Telecom ICs

Fujitsu Semiconductor Device
DATA BOOK

INDEX

Preface

Thank you for your interests in Fujitsu semiconductor products.

This document collects all data sheets relating to Telecom ICs within the ASSP (Application Specific Standard Product : Special Application ICs) product range as part of the "1996 Edition Fujitsu Semiconductor Device Data Books".

Please use this document together with the following data books for ASSP related products.

- ASSP and Linear ICs (DB04-00961-1E)
- Communication Control and Networks ICs (DB51-01961-1E)
- Magnet Disk, Audio, Video ICs (DB52-00961-1E)

If you have any questions regarding the specifications or descriptions in this document, please contact the Fujitsu sales department or Fujitsu agent.

Fujitsu Limited
Electronic Devices

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4. The products contained in this document are not intened for use with equipments which require extremely high reliability such as aerospace equipments, undersea repeaters, nuclear control systems equipments for life support.

How to Use This Document

Primarily, this document collects the data sheets for each product. The following three methods are available for finding a desired data sheet. Use whichever method is appropriate.

1. Using the indexes

   Look up data sheets in the indexes for each product category. The indexes appear on right-hand pages (odd numbered pages) and the first page of each index contains a table of contents.

2. Using the product lineup and typical characteristics

   Data sheets can be found using the "Product Lineup and Typical Characteristics" section in which products are categorized by function. The "Product Lineup and Typical Characteristics" section consists of product lineups on left-hand pages and typical characteristics with references to data sheet pages on right-hand pages.

3. Using the Model Name Index

   Data sheets can be looked up in the index by their Fujitsu model name (MB number). Index entries are listed in ascending numeric and alphabetic order.

Packages

1. Correspondence between product type and package

Products are introduced with a package illustration on the first or second page of the data sheet. The code given beneath each package is the Fujitsu package code.

(Note that package illustrations are provided to show the external appearance of the package. The illustration may differ from the actual product.)

2. Package dimension drawings

The package dimension drawings for products in this data book are listed at the end of this document (Index : Packages).

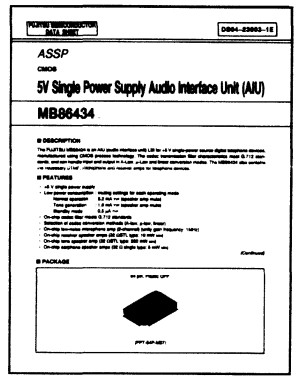
Note that the index marks denoting individual pins may differ between the actual package and the illustration or package dimension drawing.

Data Sheets

All product data sheets start from right-hand pages (odd numbered pages).

Data sheets appear in one of the following two forms.

1. Regular form


FUJITSU SEMICONDUCTOR DATA SHEET

DS04-23003-1E

ASSP

CMOS

5V Single Power Supply Audio Interface Unit (AIU)

MB86434

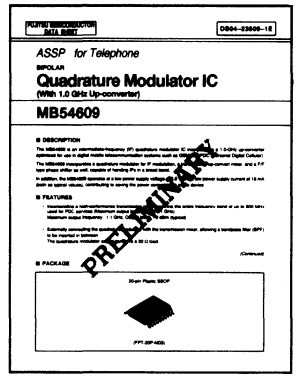
■ DESCRIPTION

■ FEATURES

■ PACKAGE

Products with data sheets in this form are in mass production.

2. Preliminary form



FUJITSU SEMICONDUCTOR DATA SHEET

DS04-23009-1E

ASSP for Telephone

BIPOLAR

Quadrature Modulator IC

(With 1.0 GHz Up-converter)

MB54609

■ DESCRIPTION

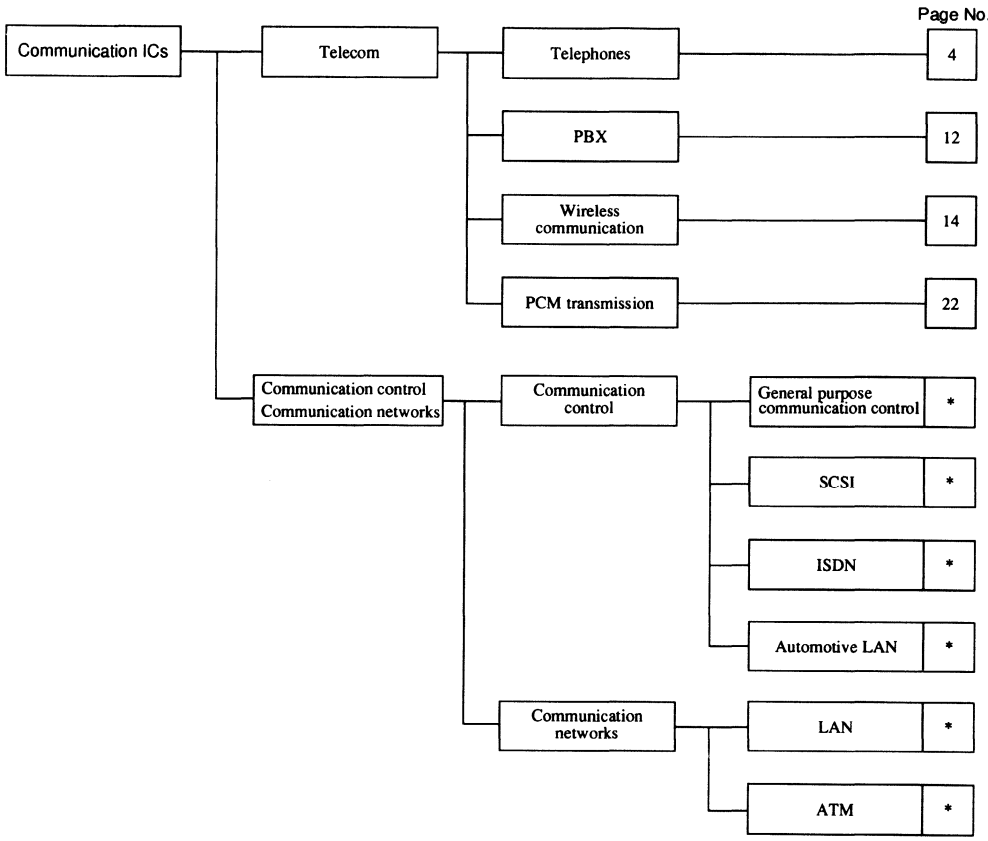
■ FEATURES

■ PACKAGE

The word "PRELIMINARY" printed on the first page indicates that the electrical ratings and other values are provisional values only. Always contact the Fujitsu marketing department or Fujitsu agent when considering the use of such products.

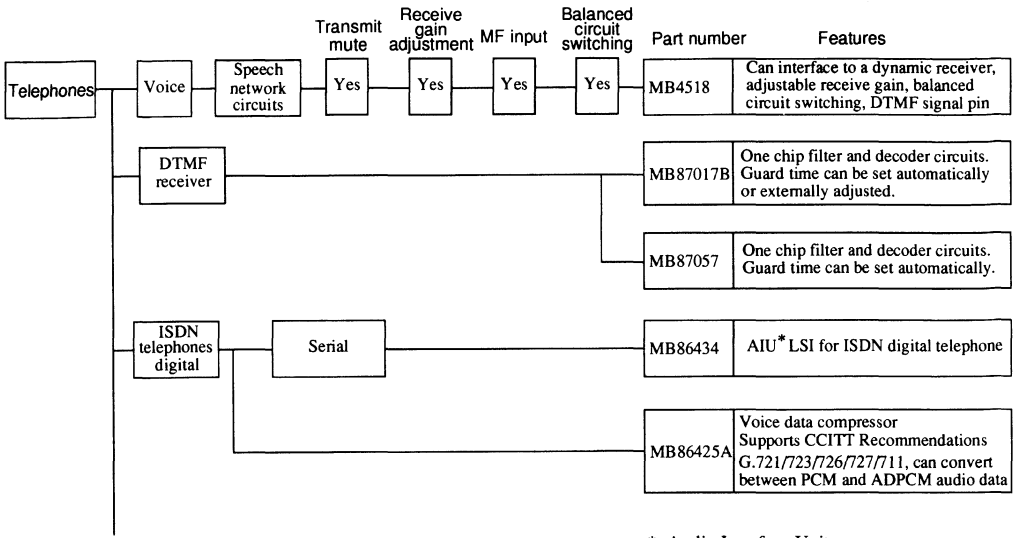
Table of Contents

1 Product Line-up and Typical Characteristics



*: See the Communication Control and Networks ICs Data Book.

Telephone Products



■ Telephone Products

Speech Network

Part number	Functions	Transmit		Receive		Dialling (MF input pin)	Balanced circuit switching	Power supply current (mA)	Power supply voltage (V) (max.)	Packages		Page No.
		Gain boost	Transmit mute	Gain adjustable externally	Gain boost					SH-DIP	SOP	
MB4518	Speech network Transmit expander circuit Speaker amplifier		●	●	6 dB	●	●	20 to 120	+12	28P	28P	39

Package: P - Plastic, C - Ceramic

DTMF Receiver

Part number	Functions	Oscillation frequency (MHz)	Signal input level (min.)	Power supply voltage (V)	Packages		Page No.
					DIP	SOP	
MB87017B	DTMF receiver	3.579	−29 dBm	+5±5%	18P	24P	53
MB87057					18P	24P	63

Package: P - Plastic, C - Ceramic

ISDN Digital Telephone LSIs

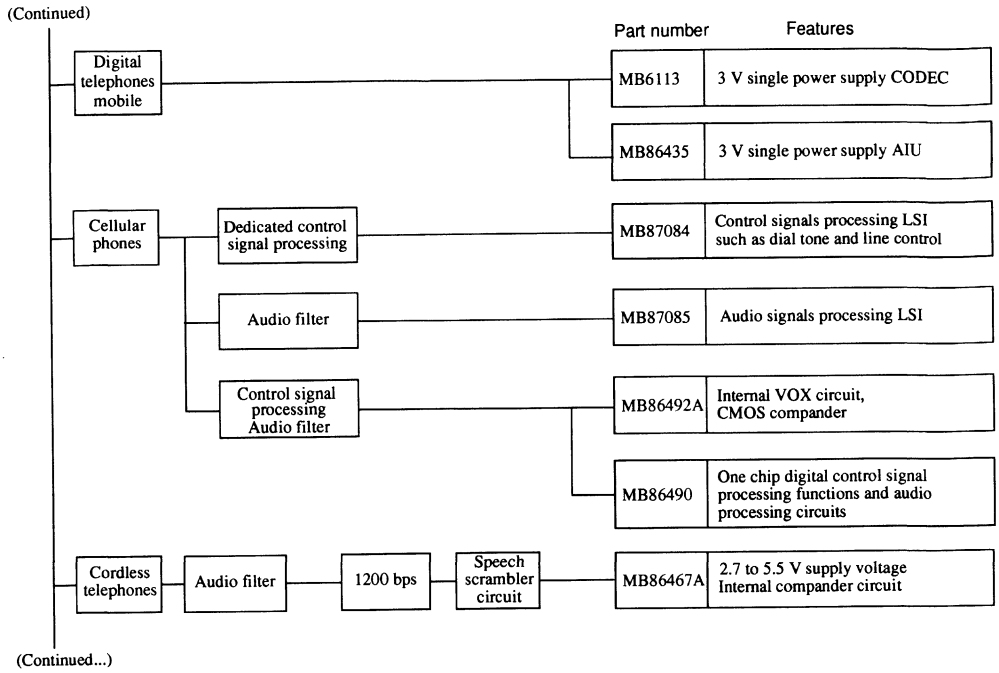
Part number	Functions	CODEC	Power supply voltage (V)	Package	Page No.
				QFP	
MB86434	AIU for ISDN digital telephones CODEC, DTMF tones, service tone Internal ringer tone	A-laW μ-laW 14-bit linear	±5±5%	64P	71

Package: P - Plastic, C - Ceramic

Voice Data Compressors for ISDN Digital Telephones

Part number	Functions	Communication standard	Power supply voltage (V)	Package	Page No.
				QFP	
MB86425A	Voice data compressor Conversion between PCM and ADPCM audio data Supports CCITT Recommendations G.721/723/726 with a 16K, 24K, 32K, and 40K bps ADPCM algorithm Either G.711 A-law or μ-law PCM data can be selected. Supports G.727 embedded ADPCM, suitable for voice mail applications PCM/ADPCM data I/O interface can be selected from either IOM-2, SLD, CODEC, or Group 1 speed backplane. Supports various test modes for equipment testing. Low power operation (5 mW, typ.)	CCITT Recommendations G.721/723/726/727/711	+5±5%	48P	—

Package: P - Plastic, C - Ceramic


(Continued)
Part number
Features
Digital telephones mobile
MB6113
3 V single power supply CODEC
MB86435
3 V single power supply AIU
Cellular phones
Dedicated control signal processing
MB87084
Control signals processing LSI such as dial tone and line control
Audio filter
MB87085
Audio signals processing LSI
Control signal processing Audio filter
MB86492A
Internal VOX circuit, CMOS compander
MB86490
One chip digital control signal processing functions and audio processing circuits
Cordless telephones
Audio filter
1200 bps
Speech scrambler circuit
MB86467A
2.7 to 5.5 V supply voltage Internal compander circuit
(Continued...)

LSIs for Digital Mobile Telephones

Part number	Functions	Compression law	Power supply voltage (V)	Packages		Page No.
				SQFP	TSOP	
MB6113	3 V single power supply CODEC	A-laW μ-laW	2.97 to 3.6	—	24P	—
MB86435	3 V single power supply AIU	A-laW μ-laW linear	2.7 to 3.6	64P	—	107

Package: P - Plastic, C - Ceramic

LSIs for Cellular Phones

Part number	Functions	Frequency bands	Power supply voltage (V)	Packages		Page No.
				QFP	SQFP	
MB87084	Dedicated control signal processing LSI	AMPS, NMT, TACS	+5±10%	48P	—	—
MB87085	Audio filter			48P	—	141
MB86492A	Internal audio filter, VOX circuit, and CMOS compander	AMPS, TACS	+3.0 to +5.5	—	80P	—
MB86490	Control signal processing functions, audio filter LSI		+5±10%	80P	100P	159

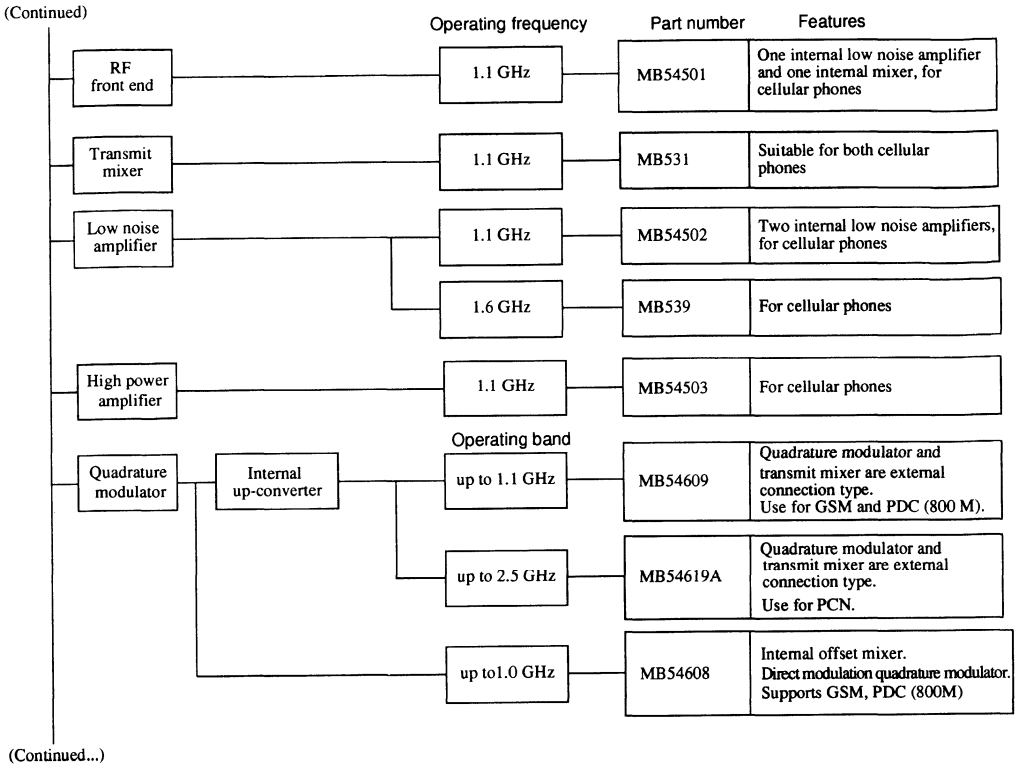
Package: P - Plastic, C - Ceramic

Audio Filters for Cordless Telephones

Part number	Internal modem*	Speech scrambler circuit	Compander	Power supply voltage (V)	Package	Page No.
					QFP	
MB86467A	1200 bps	Internal	Internal	+2.7 to +5.5	48P	—

*:MSK(Minimum Shift Keying)

Package: P - Plastic, C - Ceramic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Operating frequency
Part number
Features
RF front end
1.1 GHz
MB54501
One internal low noise amplifier and one internal mixer, for cellular phones
Transmit mixer
1.1 GHz
MB531
Suitable for both cellular phones
Low noise amplifier
1.1 GHz
MB54502
Two internal low noise amplifiers, for cellular phones
1.6 GHz
MB539
For cellular phones
High power amplifier
1.1 GHz
MB54503
For cellular phones
Operating band
Quadrature modulator
Internal up-converter
up to 1.1 GHz
MB54609
Quadrature modulator and transmit mixer are external connection type.
Use for GSM and PDC (800 M).
up to 2.5 GHz
MB54619A
Quadrature modulator and transmit mixer are external connection type.
Use for PCN.
up to1.0 GHz
MB54608
Internal offset mixer.
Direct modulation quadrature modulator.
Supports GSM, PDC (800M)
(Continued...)

RF Front End

Part number	Functions		Operating frequency (GHz)	Gain	Noise figure	1 dB compression	Power supply voltage (V)	Package SSOP	Page No.
MB54501	RF front end	(Amp.)	1.1	14 dB	2.2 dB	−1 dBm	+2.7 to +5.5	16P	191
		(Mixer)		15 dB	5 dB	—			

Package: P - Plastic, C - Ceramic

Transmit Mixer

Part number	Functions	Operating frequency (GHz)	Conversion gain (typ.)	1 dB compression point (typ.)	3rd order intercept point (typ.)	Power supply voltage (V)	Package SOP	Page No.
MB531	Transmit mixer	1.1	3.5 dB	−12 dBm	−3 dBm	+5±10%	8P	197

Package: P - Plastic, C - Ceramic

Low Noise Amplifier

Part number	Functions	Operating frequency (GHz)	Gain	Noise figure	1 dB compression (typ.)	Amplitude variation (820±50 MHz)	Power supply voltage (V)	Package SSOP	Page No.
MB54502	Low noise amplifier	1.1	14 dB	2.2 dB	−6 dBm	2.5 dB	+2.7 to +5.5	16P	203

Part number	Functions	Operating frequency (GHz)	Gain	Noise figure	Maximum output voltage	Power supply voltage (V)	Package SSOP	Page No.
MB539	Low noise amplifier	1.6	11 dB	4 dB	−7 dBm	+5±10%	8P	209

Package: P - Plastic, C - Ceramic

High Power Amplifier

Part number	Functions	Operating frequency (GHz)	Gain	Output level (For Pin = −8 dBm)	Input return loss	Output return loss	Power supply voltage (V)	Package SSOP	Page No.
MB54503	High power amplifier	1.1	25 dB	+13 dBm	14 dB	6 dB	+2.7 to +5.0	16P	215

Package: P - Plastic, C - Ceramic

Quadrature Modulator

Part number	Functions	Operating band (GHz)	Output level (dBm)	Vector error (RMS value)	Power supply current (mA)	Power supply voltage (V)	Package SSOP	Page No.
MB54609	Quadrature modulator with internal up-converter (with power-save mode)	up to 1.1	−9	1.9%*1	18	+2.7 to +3.3	20P	221
MB54619A		up to 2.5	−15	2.0%*2	23	+2.7 to +3.8	20P	—
MB54608	Direct modulation quadrature modulator (with power save mode)	up to 1.0	−8	3.0%*1	26	+2.7 to +3.8	20P	—

*1: 800 MHz PDC specification. *2: PHS specification.

Package: P - Plastic, C - Ceramic

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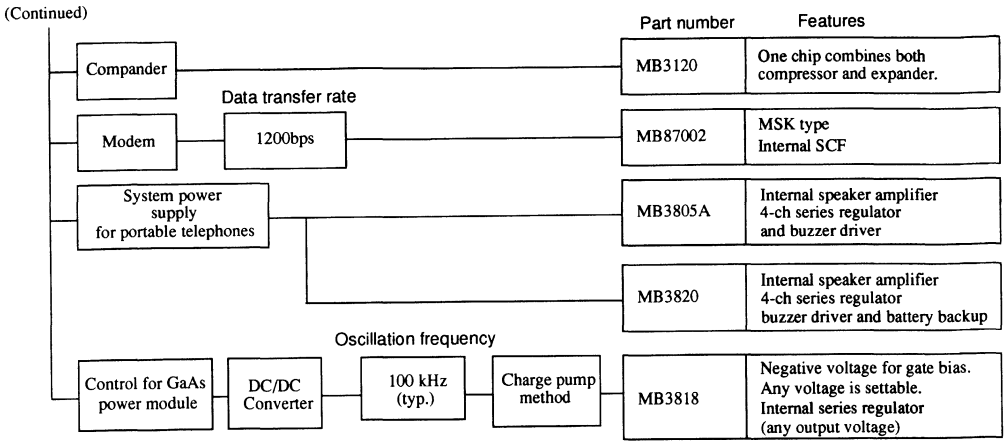

Part number
Features
Compander
MB3120
One chip combines both compressor and expander.
Data transfer rate
Modem
1200bps
MB87002
MSK type
Internal SCF
System power supply for portable telephones
MB3805A
Internal speaker amplifier
4-ch series regulator
and buzzer driver
MB3820
Internal speaker amplifier
4-ch series regulator
buzzer driver and battery backup
Oscillation frequency
Control for GaAs power module
DC/DC Converter
100 kHz (typ.)
Charge pump method
MB3818
Negative voltage for gate bias.
Any voltage is settable.
Internal series regulator
(any output voltage)

Compander

Part number	Functions	Compander section		Power supply current (typ.) (mA)	Power supply voltage (V)	Packages		Page No.
		Total harmonic distortion	Noise output voltage			SOP	ZIP	
MB3120	Compander	0.5% (typ.)	< −80 dBm	3.0	+3.2 to ±10	16P	17P	243

Package: P - Plastic, C - Ceramic

Modem

Part number	Functions	Type	Transfer rate	Packages		Page No.
				DIP	SOP	
MB87002	Modem	MSK (Minimum Shift Keying)	1200 bps	16P	16P	253

Package: P - Plastic, C - Ceramic

System Power Supply for Mobile Telephones

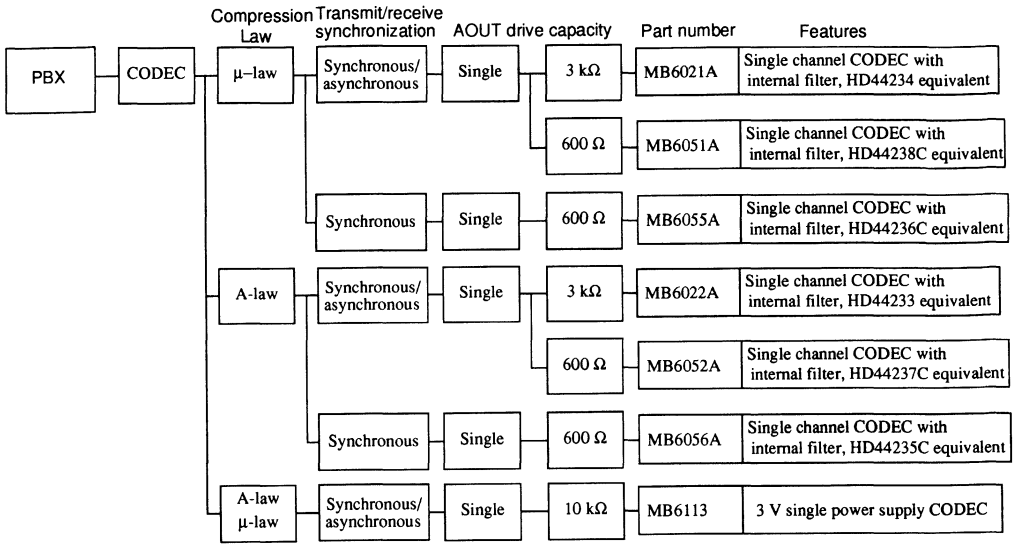
Part number	Functions	Output	Speaker amplifier output power (typ.) (mW)	Power supply voltage (V)	Package	Page No.
					SQFP	
MB3805A	System power supply for portable telephones	3.3 V x 2ch, 4.0 V x 2ch	160 (Vcc=4.8 V)	4.3 to 8	48P	—
MB3820		3.0 V x 4ch	90 (Vcc=3.6 V)	3.49 to 8	48P	—

Package: P - Plastic, C - Ceramic

GaAs Power Module Controller

Part number	Function	Gate voltage (V)	Series regulator (V)	Power supply voltage (V)	Package	Page No.
					SSOP	
MB3818	DC/DC converter for GaAs power module control	−2.4 to 4.0 (arbitrary)	2.6 to 3.6 (arbitrary)	3.6 to 6.0	24P	—

Package: P - Plastic, C - Ceramic


PBX
CODEC
Compression Law
Transmit/receive synchronization
AOUT drive capacity
Part number
Features
μ–law
Synchronous/ asynchronous
Single
3 kΩ
MB6021A
Single channel CODEC with internal filter, HD44234 equivalent
600 Ω
MB6051A
Single channel CODEC with internal filter, HD44238C equivalent
Synchronous
Single
600 Ω
MB6055A
Single channel CODEC with internal filter, HD44236C equivalent
A-law
Synchronous/ asynchronous
Single
3 kΩ
MB6022A
Single channel CODEC with internal filter, HD44233 equivalent
600 Ω
MB6052A
Single channel CODEC with internal filter, HD44237C equivalent
Synchronous
Single
600 Ω
MB6056A
Single channel CODEC with internal filter, HD44235C equivalent
A-law μ-law
Synchronous/ asynchronous
Single
10 kΩ
MB6113
3 V single power supply CODEC

■ PBX Products

CODEC (MB6020A Series)

Part number	Functions	Companding law	Transmit/receive synchronization	AOUT drive capacity	Power supply voltage (V)	Package DIP	Page No.
MB6021A	CODEC	μ-law	Synchronous/asynchronous	Single-end 3kΩ	+5±5%	16P	267
MB6022A		A-law			−5±5%	16P	267

Package: P - Plastic, C - Ceramic

CODEC (MB6050A Series)

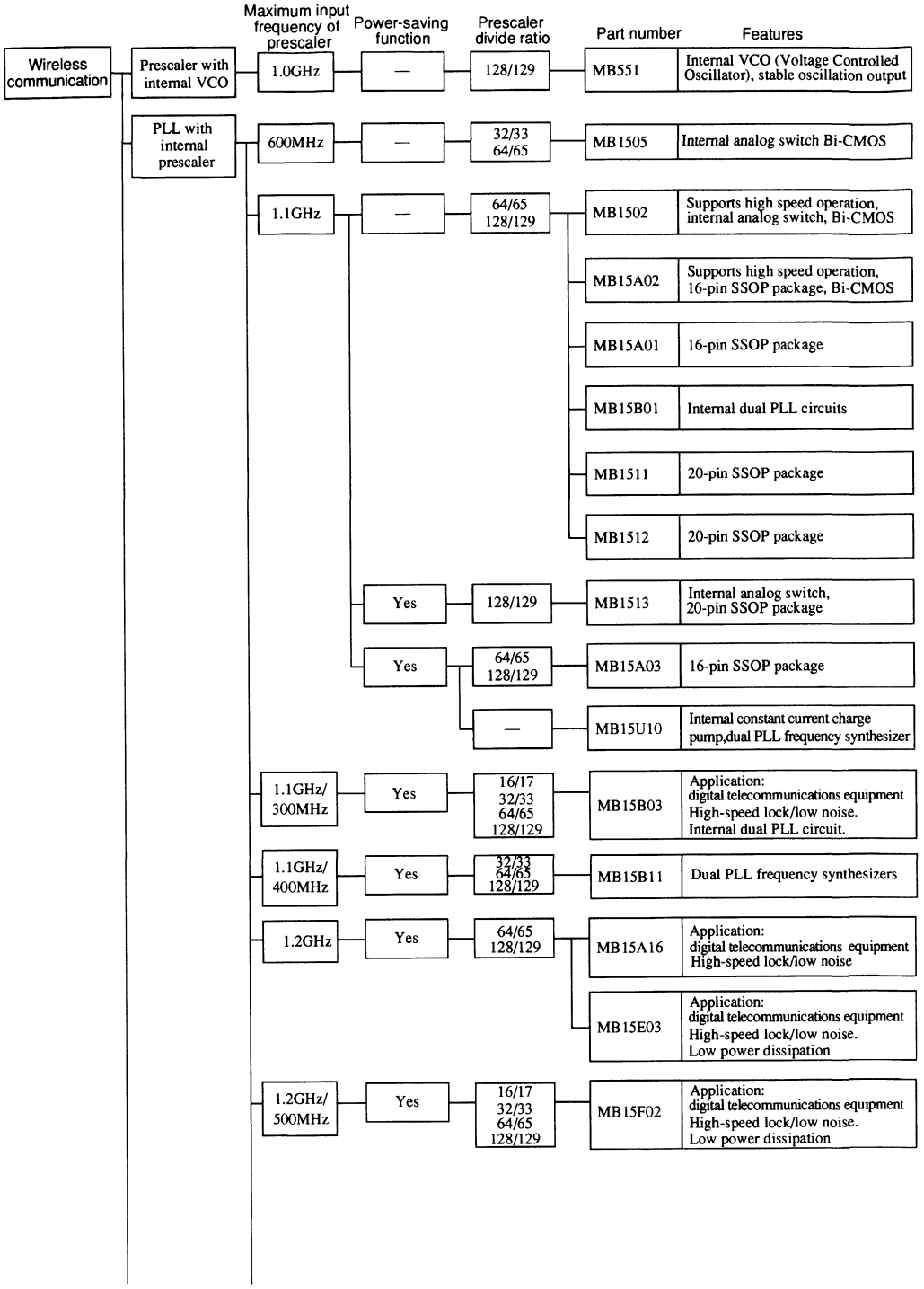
Part number	Functions	Companding law	Transmit/receive synchronization	AOUT drive capacity	Power supply voltage (V)	Package DIP	Page No.
MB6051A	CODEC	μ-law	Synchronous/asynchronous	Single-end 600Ω	+5±5% −5±5%	16P	—
MB6052A		A-law				16P	—
MB6055A		μ-law	Synchronous			16P	—
MB6056A		A-law				16P	—

Package: P - Plastic, C - Ceramic

CODEC (MB6113)

Part number	Functions	Companding law	Transmit/receive synchronization	AOUT drive capacity	Power supply voltage (V)	Package TSOP	Page No.
MB6113	CODEC	A-law / μ-law	Synchronous/asynchronous	Single-end 10kΩ	+3.3±10%	24P	—

Package: P - Plastic, C - Ceramic



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■ Wireless Communication Products

Prescaler with Internal VCO

Part number	Functions	Prescaler maximum input frequency (GHz)	Prescaler divide ratio	C/N ratio (typ.)	S/N ratio (typ.)	Power supply current (mA) (typ.)	Power supply voltage (V)	Package SOP	Page No.
MB551	Prescaler with internal VCO	1.0	128/129	65 dB	45 dB	15	+5±10%	8P	287

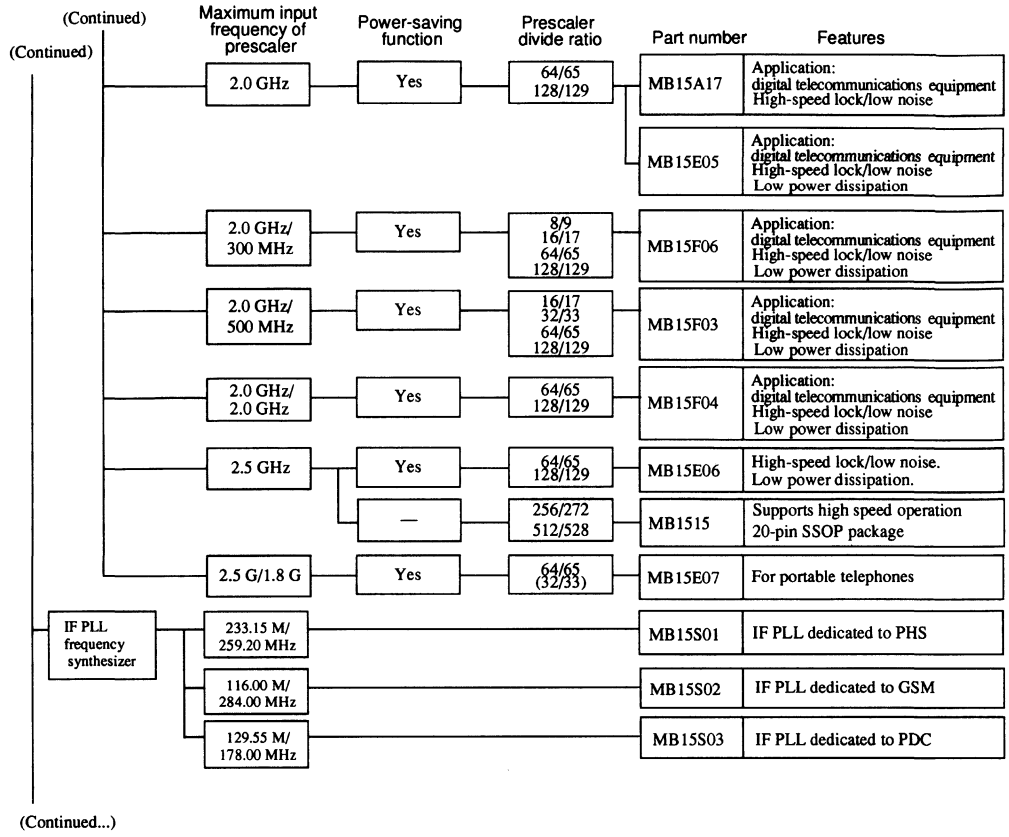
Package: P - Plastic, C - Ceramic

PLL Frequency Synthesizers with Internal Prescaler

Part number	Functions	Maximum input frequency (Hz)	Prescaler divide ratio	Program counter divide ratio	Swallow counter divide ratio	Reference counter divide ratio	Power supply current (mA)	Power supply voltage (V)	Packages DIP	Packages SOP	Packages SSOP	Page No.
MB1505	PLL frequency synthesizers with internal prescaler	600M	32/33 64/65	Binary 11-bit 16 to 2047	Binary 7-bit 0 to 127	Binary 14-bit 8 to 16383	6	+5±10%	16P	16P	—	—
MB1502		1.1 G	64/65 128/129				8	+5±10%	16P	16P	—	—
MB15A02							7		—	16P	16P, 20P	303
MB15A01†				Binary 11-bit 5 to 2047		Binary 14-bit 6 to 16383	6.5	+2.7 to +3.5	—	—	16P, 20P	321
MB15B01†				Binary 11-bit 16 to 2047		Binary 14-bit 8 to 16383	13/0.2*		—	—	20P	339
MB1511							7	+2.7 to +5.5	—	—	20P	357
MB1512							8	+5	—	—	20P	371
MB1513			128/129				8/0.1*	±10%	—	—	20P	381
MB15A03†			64/65 128/129	Binary 11-bit 5 to 2047		Binary 14-bit 6 to 16383	6.5/0.1*	+2.7 to +3.5	—	—	16P, 20P	395
MB15U10†			—	Binary 17-bit 1024 to 131071	—	Binary 12-bit 6 to 4095	7/0.01*	+2.6 to +5.5	—	—	20P	413
MB15B03†		1.1G/300M	16/17 32/33 64/65 128/129	Binary 11-bit 5 to 2047	Binary 7-bit 0 to 127	Binary 14-bit 6 to 16383	10/0.2*	+2.7 to +3.6	—	—	16P	431
MB15B11†		1.1G/400M	64/65 128/129 32/33 64/65	Binary 11-bit 16 to 2047		Binary 14-bit 8 to 16383	9.5/0.2*	+2.7 to +3.5	—	—	20P	449
MB15A16†		1.2G	64/65 128/129	Binary 11-bit 5 to 2047		Binary 14-bit 6 to 1683	7/0.1*	+2.7 to +3.6	—	—	16P	473
MB15E03						Binary 14-bit 5 to 16383	3.5/0.01		—	—	16P	491
MB15F02		1.2G/500M	16/17 32/33 64/65 128/129				6.0/0.02		—	—	16P	509

*: In power-saving mode
†: New product

Package: P - Plastic, C - Ceramic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Maximum input frequency of prescaler
Power-saving function
Prescaler divide ratio
Part number
Features
2.0 GHz
Yes
64/65
128/129
MB15A17
Application:
digital telecommunications equipment
High-speed lock/low noise
MB15E05
Application:
digital telecommunications equipment
High-speed lock/low noise
Low power dissipation
2.0 GHz/
300 MHz
Yes
8/9
16/17
64/65
128/129
MB15F06
Application:
digital telecommunications equipment
High-speed lock/low noise
Low power dissipation
2.0 GHz/
500 MHz
Yes
16/17
32/33
64/65
128/129
MB15F03
Application:
digital telecommunications equipment
High-speed lock/low noise
Low power dissipation
2.0 GHz/
2.0 GHz
Yes
64/65
128/129
MB15F04
Application:
digital telecommunications equipment
High-speed lock/low noise
Low power dissipation
2.5 GHz
Yes
64/65
128/129
MB15E06
High-speed lock/low noise.
Low power dissipation.
—
256/272
512/528
MB1515
Supports high speed operation
20-pin SSOP package
2.5 G/1.8 G
Yes
64/65
(32/33)
MB15E07
For portable telephones
IF PLL
frequency
synthesizer
233.15 M/
259.20 MHz
MB15S01
IF PLL dedicated to PHS
116.00 M/
284.00 MHz
MB15S02
IF PLL dedicated to GSM
129.55 M/
178.00 MHz
MB15S03
IF PLL dedicated to PDC
(Continued...)

PLL Frequency Synthesizers with Internal Prescaler

Part number	Functions	Maximum input frequency (Hz)	Prescaler divide ratio	Program counter divide ratio	Swallow counter divide ratio	Reference counter divide ratio	Power supply current (mA)	Power supply voltage (V)	Packages			Page No.
									DIP	SOP	SSOP	
MB15A17	PLL frequency synthesizers with internal prescaler	2.0G	64/65 128/129	Binary 11-bit 5 to 2047	Binary 7-bit 0 to 127	Binary 14-bit 6 to 16383	14/0.2*	+2.7 to +3.6	—	—	16P	531
MB15E05†						Binary 14-bit 5 to 16383	6/0.01*		—	—	16P	549
MB15F06†		2.0G/300M	8/9 16/17 64/65 128/129				9/0.02		—	—	16P	—
MB15F03†		2.0G/500M	16/17 32/33 64/65 128/129						—	—	16P	567
MB15E06†		2.5G	64/65 128/129				7/0.01		—	—	16P	587
MB1515			256/272 512/528	Binary 12-bit 32 to 4095	Binary 5-bit 0 to 31	256, 512, 1024, 2048	16	+5±10%	—	—	20P	605
MB15E07†		2.5G/ (1.8G)	64/65 (32/33)	Binary 11-bit 5 to 2047	Binary 7-bit 0 to 127	Binary 14-bit 5 to 16383	8/0.01	+2.7 to +3.6	—	—	16P	—

†: New product

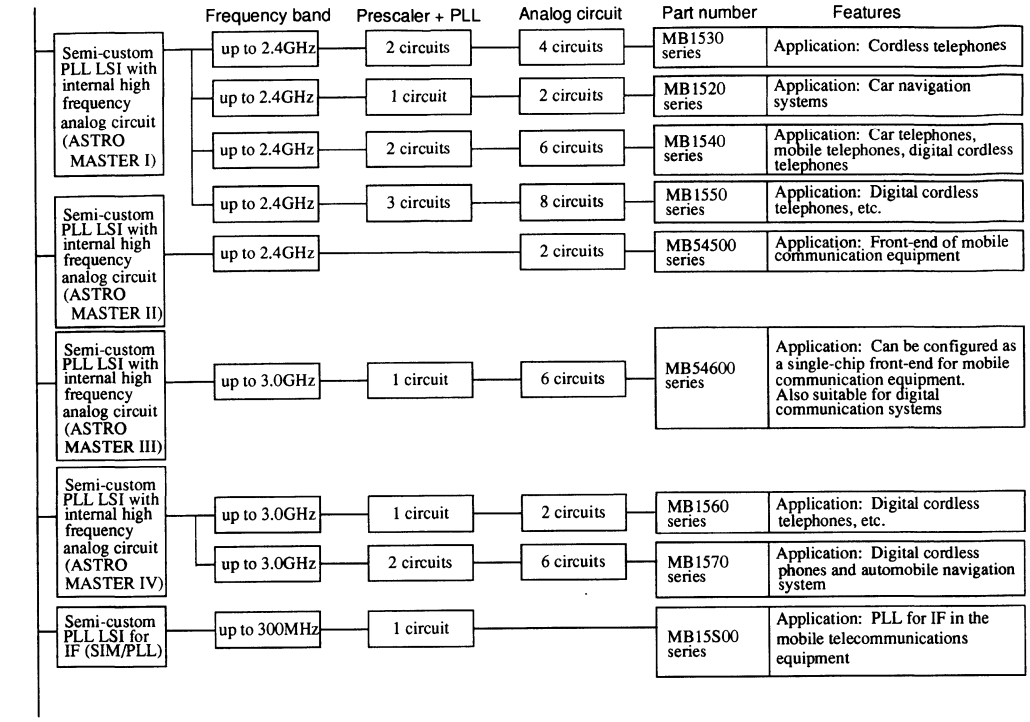
*:In power-saving mode

IF PLL Frequency Synthesizer

Part number	Application	Frequency (MHz)	Power supply current (mA)	Power supply voltage (V)	Package	Page No.
					SSOP	
MB15S01†	PHS	259.20	3.5	+2.7 to +3.6	8P	619
MB15S02†	GSM	116.00			8P	633
MB15S03†	PDC	129.55			8P	645

†: New product

(Continued...)



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Semi-Custom PLL LSI with Internal High Frequency Analog Circuit (ASTRO MASTER I)

Part number (Series name)	Frequency band (GHz)	Prescaler + PLL number of circuits	Analog circuits*1	Power supply voltage (V)	Packages			Page No.
					SSOP	QFP	SQFP	
MB1530 series	up to 2.4	2	4	+5/+3	34P	—	—	659
MB1520 series		1	2		20P	—	—	659
MB1540 series		2	6		—	48P	48P	659
MB1550 series		3*2	8		—	48P	64P	659

*1: The analog circuit structure consists of an RF amplifier, VCO oscillator circuit, mixer, and IF amplifier. Package: P - Plastic, C - Ceramic
*2: Includes the single divider PLL1 circuit.

Semi-Custom LSI with Internal High Frequency Analog Circuit (ASTRO MASTER II)

Part number (Series name)	Frequency band (GHz)	Number of prescaler circuits	Analog circuits	Power supply voltage	Packages		Page No.
					SOP	SSOP	
MB54500 series	up to 2.0	—	2	+5/+3	8P, 14P	8P, 16P	681

Package: P - Plastic, C - Ceramic

Semi-Custom LSI with Internal High Frequency Analog Circuit (ASTRO MASTER III)

Part number (Series name)	Frequency band (GHz)	Number of prescaler circuits	Analog circuits	Power supply voltage	Package	Page No.
					SSOP	
MB54600 series	up to 3.0	1	6	+3/+2.2	20P, 34P	693

Package: P - Plastic, C - Ceramic

Semi-Custom LSI with Internal High Frequency Analog Circuit (ASTRO MASTER IV)

Part number (Series name)	Frequency band (GHz)	Number of prescaler circuits	Analog circuits	Power supply voltage (V)	Packages			Page No.
					SSOP	QFP	SQFP	
MB1560 series†	up to 3.0	1	2	+3	20P,34P	—	—	705
MB1570 series		2	6		—	48P	48P,64P	—

†:New product

Package: P - Plastic, C - Ceramic

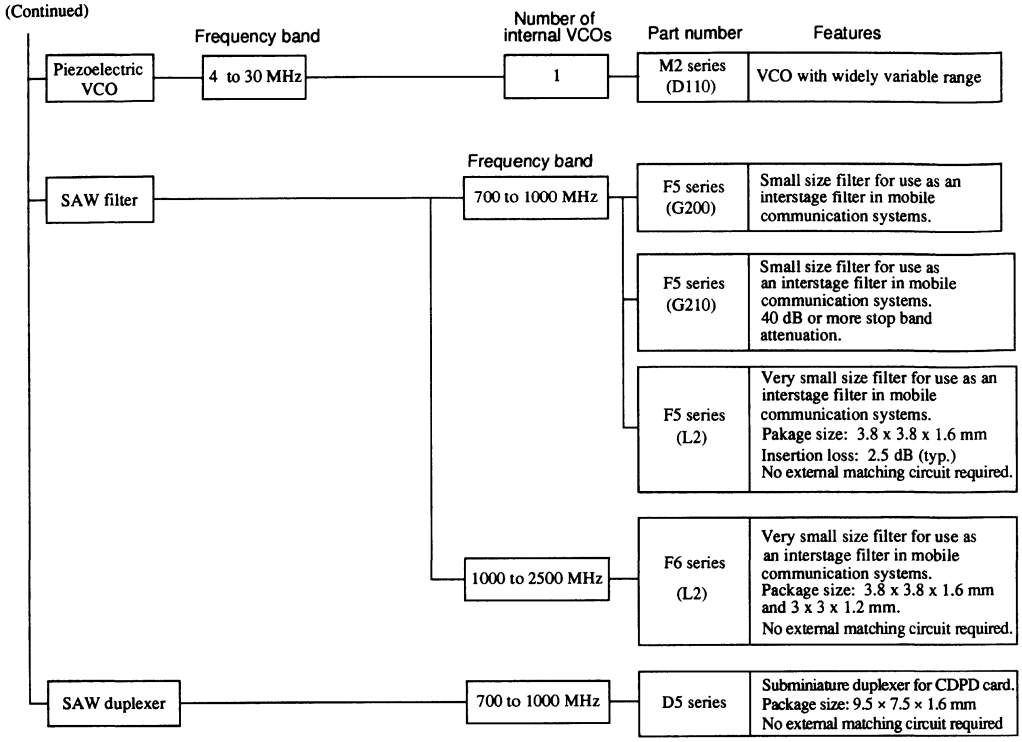
IF PLL frequency synthesizer semi-custom LSI (SIM/PLL)

Part number (Series name)	Frequency band (MHz)	Number of prescaler circuits	Analog circuits	Power supply voltage (V)	Packages		Page No.
					SOP	SSOP	
MB15S00 series†	up to 300	1	—	+2.7 to +3.3	—	8P	721

†:New product

Package: P - Plastic, C - Ceramic

(Continued)


Frequency band
Number of internal VCOs
Part number
Features
Piezoelectric VCO
4 to 30 MHz
1
M2 series (D110)
VCO with widely variable range
SAW filter
Frequency band
700 to 1000 MHz
F5 series (G200)
Small size filter for use as an interstage filter in mobile communication systems.
F5 series (G210)
Small size filter for use as an interstage filter in mobile communication systems. 40 dB or more stop band attenuation.
F5 series (L2)
Very small size filter for use as an interstage filter in mobile communication systems. Pakage size: 3.8 x 3.8 x 1.6 mm Insertion loss: 2.5 dB (typ.) No external matching circuit required.
1000 to 2500 MHz
F6 series (L2)
Very small size filter for use as an interstage filter in mobile communication systems. Package size: 3.8 x 3.8 x 1.6 mm and 3 x 3 x 1.2 mm. No external matching circuit required.
SAW duplexer
700 to 1000 MHz
D5 series
Subminiature duplexer for CDPD card. Package size: 9.5 × 7.5 × 1.6 mm No external matching circuit required

Piezoelectric VCO

Part number	Functions	Output frequency (MHz)	Frequency variation range	Control voltage (V)	Output level	Temperature characteristics	Operating temperature (°C)	Supply voltage (V)	Page No.
M2 series (D110)	Voltage controlled oscillator	4 to 30	±0.2% or more	0 to 5	CMOS level	−0.03 to +0.05%	−10 to +70	+5±5%	737

SAW Filter for Car or Mobile Telephones

Part number	Functions	Frequency range (MHz)	Bandwidth (MHz)	Operating temperature (°C)	Applicable types	Page No.
F5 series (G200)	Filter	700 to 1000	12 to 41*	−30 to +85	AMPS, NTT, ETACS, NMT, NTACS, GSM	743
F5 series (G210)	Filter stop band attenuation is 40 dB or more				AMPS, ETACS, NMT, GSM	767
F5 series (L2)	Filter insertion loss is 2.5 dB (typ.)				AMPS, NTT, ETACS, NMT, NTACS, PDC800, GSM, etc.	781

*: Depends on type and frequency band

SAW Filter for Digital Mobile Communication Systems

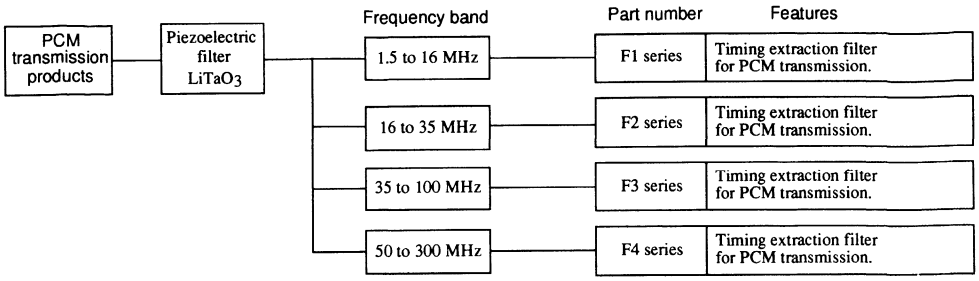
Part number	Functions	Frequency range (MHz)	Bandwidth (MHz)	Operating temperature (°C)	Applicable types	Page No.
F6 series (L2)	Filter insertion loss is 3.0 dB (typ.)	1000 to 2500	24 to 100	−30 to +85	PDC1.5G, Wireless LAN, DCS1800, PCS	809

SAW Duplexer for CDPD Cards

Part number	Functions	Frequency (MHz)	Bandwidth (MHz)	Insertion loss (dB)	Stopband attenuation (dB)	Applicable types	Page No.
D5 series†	Antenna duplexer	836 (Tx side)	25	3	30	AMPS	—
		881 (Rx side)		4	40		

†: Under development

PCM Transmission Products



■ PCM Transmission Products

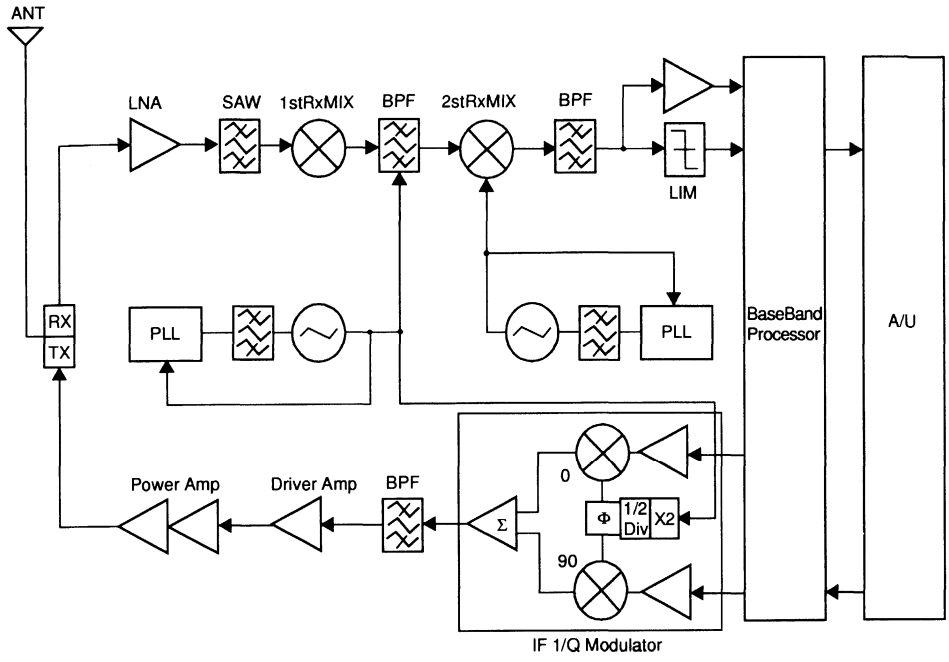
Piezo-electric Filter $LiTaO_3$

Part number	Function	Frequency range f_0 (MHz)	Proportional Bandwidth $\Delta f > f_0$	Insertion loss IL	Stop band attenuation at $2f_0$	Temperature characteristics (−10 to +60°C)	Page No.
F1 series	Timing extraction filter	1.5 to 16	0.1 to 2.5%	6 dB or less	20 dB or more	400ppm or less	833
F2 series		16 to 35					833
F3 series		35 to 100	0.5 to 2%			−30ppm/°C	833
F4 series		50 to 300	0.3 to 1.0%		15 dB or more ($f_0 \pm 10$ MHz)	200ppm or less	841

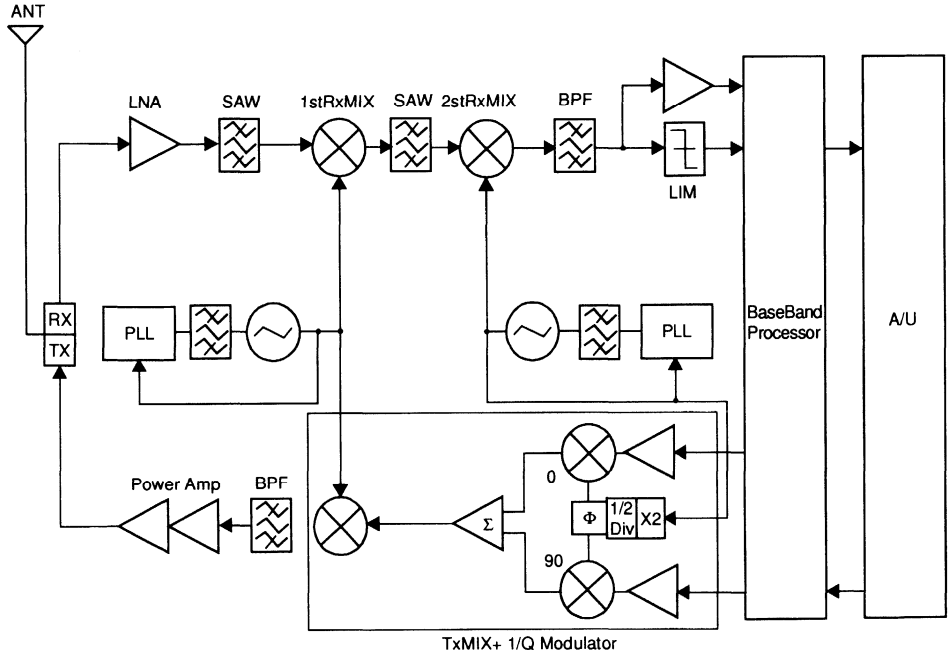
Communication Equipment

1. Telephones

System Configuration of a Digital Cellular Phone



System Configuration of a Digital Cordless Phone



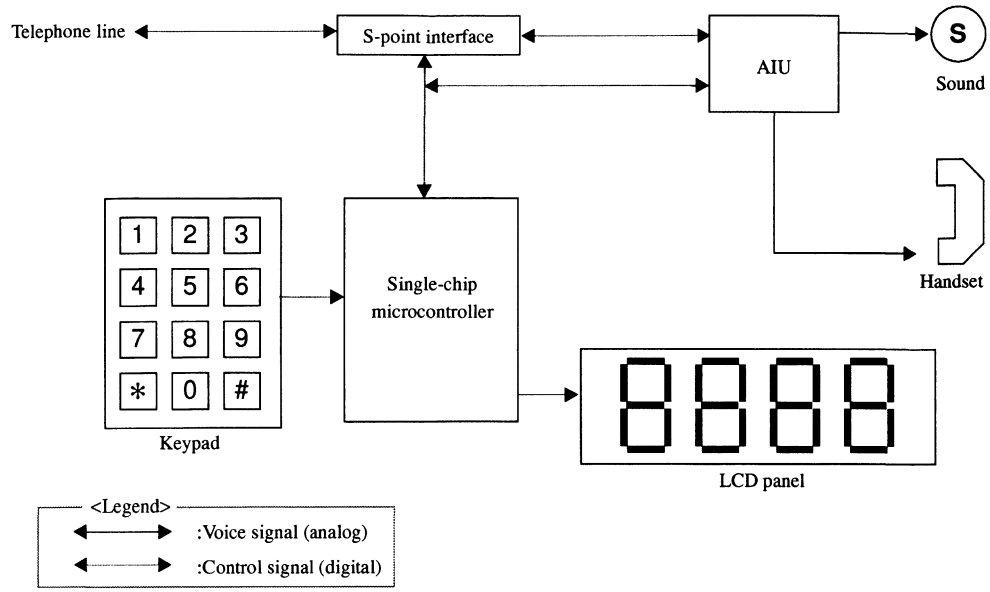
Recommended Semiconductor Products [Digital Cellular]

Part number	Functions
MB15A16	PLL frequency synthesizer with an internal prescaler
MB15A17	
MB15E03	
MB15E04	
MB15E05	
MB15F02	
MB15F03	
MB154x, MB155x	Semicustom PLLLSI (ASTRO I) with internal high frequency analog circuit.
MB156x, MB157x	Semicustom PLLLSI (ASTRO V) with internal high frequency analog circuit.
MB545xx	Semicustom LSI (ASTRO II) with internal high frequency analog circuit.
MB546xx	Semicustom LSI (ASTRO III) with internal high frequency analog circuit.
MB15Sxx	IFPLL frequency synthesizer semicustom LSI (SIM/PLL)
MB15S02	IFPLL frequency synthesizer
MB15S03	
MB54608	Quadrature modulator
MB54609	
MB86434	Audio interface unit (AIU)
MB86435	

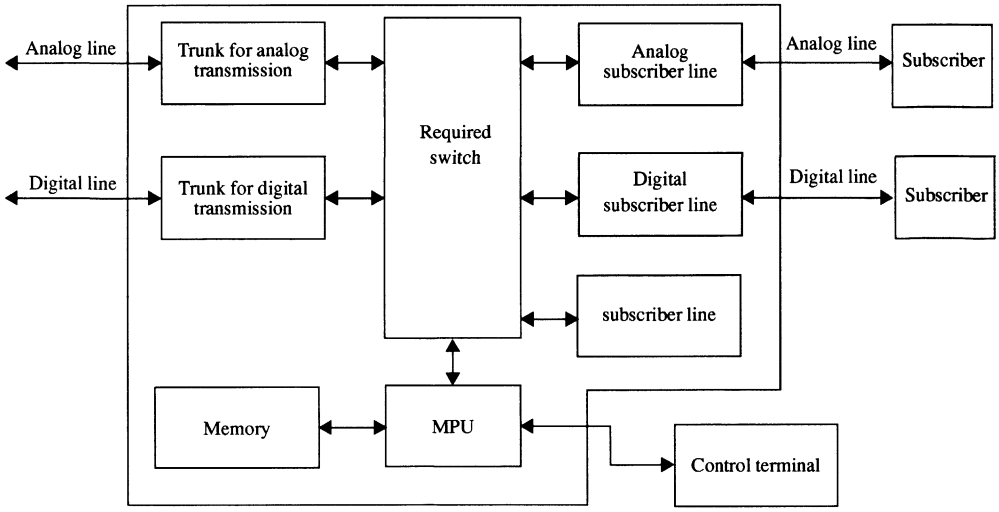
Recommended Semiconductor Products [Digital Cordless]

Part number	Functions
MB15A17	PLL frequency synthesizer with an internal prescaler
MB15E04	
MB15E05	
MB15F03	
MB15F05	
MB154x, MB155x	Semicustom PLLLSI (ASTRO I) with internal high frequency analog circuit.
MB156x, MB157x	Semicustom PLLLSI (ASTRO V) with internal high frequency analog circuit.
MB545xx	Semicustom LSI (ASTRO II) with internal high frequency analog circuit.
MB546xx	Semicustom LSI (ASTRO III) with internal high frequency analog circuit.
MB15Sxx	IFPLL frequency synthesizer semicustom LSI (SIM/PLL)
MB15S01	IFPLL frequency synthesizer
MB54619A	Quadrature modulator
MB86434	Audio interface unit (AIU)
MB86435	

System Configuration of an ISDN Digital Telephone



2. System Configuration of a Telephone Switch



Recommended Semiconductor Products [ISDN Digital Telephone]

Part number	Functions
MB86434	Audio interface unit (AIU)
MB86435	
MB86405A	ISDN S-point interface controller (internal driver/receiver)

Recommended Semiconductor Products [PBX]

Part number	Functions
MB87017B	DTMF receiver
MB6021A	CODEC
MB6022A	
MB6051A	
MB6052A	
MB6055A	
MB6056A	
MB6113	

MEMO

Handling of Semiconductor Devices

Handling of Semiconductor Devices

1. About Absolute Maximum Ratings

(1) Absolute Maximum Ratings

The principal factors limiting the operation of semiconductor devices are voltage, current, allowable dissipation and temperature. Failure to observe any one of these elements can be a cause of damage to or destruction of semiconductor devices.

To prevent damage or destruction, certain maximum values called absolute maximum ratings (maximum ratings) are established.

Absolute maximum ratings are values which if exceeded even instantaneously will result in damage or destruction.

Therefore, users of semiconductor devices must take care that the maximum ratings for each devices are not exceeded under any condition.

The factors that determine maximum ratings are closely interrelated. Users should not therefore assume that satisfying the voltage and current ratings is sufficient, and that power dissipation limits can safely be exceeded.

The following definition of absolute maximum ratings is extracted from JISC7030 (Transistor Testing Methods) .

> Absolute maximum ratings are limiting values governing operating and environmental conditions for all transistors, and are established in the form of published standards for each transistor. These limiting values are not to be exceeded under any worst-case circumstances. The values are determined by the transistor manufacturer, who warrants that the device is able to fully perform its functions as long as it is used within these limits.

Maximum ratings represent the limits of use of a device and are generally established for voltage, current, allowable dissipation and temperature.

(2) Maximum Voltage Ratings

Maximum voltage ratings are established for supply voltage, input voltage, output voltage, and otherwise as necessary. Supply voltage is the maximum voltage that may be applied at the power supply terminal. Input and output voltages are the maximum voltages that may be applied at the input and output terminals, and are defined according to the voltage ratings of each input or output transistor.

Users should also aware that reverse connection of supply terminals can lead to forward bias current at separation and connection, which can damage the device.

(3) Maximum Current Ratings

Maximum current ratings are determined by the allowable current level of internal bonding wires, as well as the current level at which the allowable dissipation levels of the device are exceeded.

(4) Allowable Dissipation

Dissipation within the device is the source of increases in junction temperature (Tj) as power is converted into thermal energy, which causes a dramatic decline in the performance of the device. The relation between internal dissipation and junction temperature is given by the following formula :

$$Tj = P_D \times \theta + T_A$$

where P_D : dissipation
θ : thermal resistance
T_A : ambient temperature

Here thermal resistant is a constant for each device and assuming that junction temperature does not vary, if the ambient temperature is held constant then the level of dissipation within the device is necessarily limited. This factor is also affected by the material in which the device is sealed.

(5) Maximum Temperature Ratings

a. Junction Temperature

Semiconductor devices are sensitive to temperature, because as temperature increases the thermal agitation of the crystal becomes intense creating greater numbers of electron-hole pairs and making normal operation more difficult to achieve.

Junction temperature in silicon devices is between 150° and 175℃, but with epoxy resin sealing is limited to 150℃ or less.

b. Storage Temperature

Storage temperature is the temperature level at which the device can be stored. Although devices are not normally operated at this temperature, it is generally determined to be the same as junction temperature.

c. Operating Temperature

Operating temperature is the range of temperature at which the circuits of the device function normally. Device characteristics, however, may impose requirements other than those of the standard values.

2. Transportation of Devices

(1) During transportation, care must be taken to minimize mechanical vibration and shock.

(2) Placing devices upside down or on edge during transportation may cause breakage due to excess force. Be sure that devices are correctly positioned.

(3) Do not throw or drop devices.

(4) Do not expose devices to moisture.

3. Storage of Devices

(1) Temperature and humidity in the storage location should be within normal limits (5 to 30℃, 40 to 70%RH or less) , and extrem temperature and humidity should be avoided.

(2) Do not expose devices to corrosive gases or dusty circumstance.

(3) Exposure to rapid changes in temperature may cause moisture to condense into frost on devices, so that it is best to store devices in a location where there is little variation in temperature.

(4) Do not expose devices to excess loads.

(5) Containers should be made of antistatic material.

(6) Storing devices for long periods of time may cause leads to lose solderability or to become corroded, so that it is best to store devices in unprocessed state.

4. Mounting of Devices

(1) Lead Processing

The boundary between the external lead and the package greatly affect the moisture-resistance of the epoxy resin seal. Therefore considerable care should be taken not to subject this area to externally excess stress when forming external leads.

a. In particular when forming external leads by bending, etc. To avoid placing stress on the package, firmly hold the base of the lead in place before bending. Also avoid bending the base of the lead itself.

b. Take care not to apply stress to the base of the lead whenever the device is inserted into or removed from a circuit board.

(2) Soldering

When mounting a semiconductor device by soldering, it normally happens that temperatures exceeding the absolute maximum ratings are applied to the lead areas. Quality assurance with relation to thermal stability during soldering is subject to the following rules. Care must be taken not to exceed these conditions.

a. Solder temperature and immersion time : 260℃, 10 seconds or less.

b. Lead immersion position : 1 to 1.5mm from package body

c. When mounting devices using solder flow techniques, avoid immersing the package body in liquid solder.

d. When using flux, avoid the use of chlorine based fluxes, using resin-based fluxes instead.

(3) Cleaning

d. Normal Cleaning

After semiconductor devices are soldered onto circuit boards, when cleaning processes are used to remove flux and other residue, sufficient care must be taken in the selection of a cleaning solvent.

Cleaning solvent must not be flammable, poisonous or corrosive, and should have good cleaning properties. Also, because many solvents with strong cleaning properties also cause the marking to separate from the package surface, care should be taken to avoid rubbing the marking side of the package until the solvent has completely dried.

d. Ultrasound Cleaning

Avoid ultrasound cleaning at resonance points. (For structural and dimensional reasons the mechanical resonance point of internal devices is near the frequency on the order of tens of kHz point.) Also, because extended immersion in cleaning liquids can lower resistance to humidity, cleaning time should be limited to the shortest possible time.

5. Anti-Static Measures

(1) Normal Static Electricity Precautions

Anti-static measures include reducing the potential for generation of static electricity, as well as providing immediate discharge for any static electricity that does occur.

a. Prevention of static electricity in the working environment requires attention to eliminating materials likely to generate static electricity, as well as such measures as adding moisture through circulation systems in order to avoid dry air conditions.

b. In the working environment all insulating materials likely to attract charges (synthetic chemical fibers, plastics, etc.) should be avoided in favor of electro-conductive materials. Also, semiconductor devices should only be stored or transported in materials treated to prevent static electricity, or in electro-conductive containers.

(2) Static Electricity Precautions During Working Operations

a. Equipment and Machinery

All equipment used for measurement and testing, as well as conveyors, work stands, solder vessels and soldering irons should be fully grounded. Working surfaces should be covered with copper plates or other highly conductive metal, and grounded.

b. Personnel

Workers should be grounded through arm or leg bracelets. (Protective measures for personnel will be discussed later) . In addition, gloves should be worn so that devices are never touched with bare hands. The use of electrically sensitive materials in gloves and work clothes should be avoided. Shoes or sandals should provide between 100 k Ω and 100 M Ω of resistance.

c. Working Procedures

Soldering irons should be specially designed for use with semiconductors (12 to 24 volts) , and the tips should be grounded (to approximately 1 M Ω) . Handling procedures should be designed to minimize the length of time that any one device is handled.

(3) Precautions After Mounting

a. Storage

When storing or transporting printed circuit boards, use electro-conductive bags or containers. Circuit board connections should also be shorted using aluminum foil or similar material.

b. Body Grounding

Workers handling circuit boards after mounting for inspection and testing should observe the same grounding precautions as workers handling individual devices before mounting.

c. Handling

Printed circuit boards should never be touched by bare hands, and workers should wear gloves. Also, power should always be switched off whenever inserting or removing connectors.

(4) Physical Protection

The same body grounding that protects against damage from static electricity can also be a source of additional physical danger in the event that a worker receives an electrical shock. Body grounding therefore must give full consideration both to anti-static protection and protection of workers. For this reason, resistance is usually placed between the worker's body and the ground. At present, 250 k Ω to 1 M Ω is considered sufficient resistance for this purpose.

6. Thermal Design

As explained earlier in relation to maximum ratings,

dissipation within a device is closely related to its characteristics. Allowable levels of dissipation are established for each device in order to protect its operating capability, and usage in excess of these conditions is likely to cause damage or destruction to the device and reduce reliability.
Therefore it is necessary that sufficient safety margins in thermal design be provided to allow the device to be used with assurance that its function will not be impaired.

Figure 1 shows the allowable dissipation characteristics of the MB3759 switching regulator controller.
Most integrated circuit devices have characteristics such as those shown in Figure 1. This demonstrates the maximum dissipation and operating range (limited by the thermal characteristics of devices including transistors and resistors), in which reliability considerations impose limits on operating temperature. These characteristics should be borne in mind when preparing thermal designs.
Also, in devices such as power ICs that use heat relief plates, heat relief design should be used for both the the thermal resistance between the IC junction and case ($\theta_{j\text{-}c}$) and a level of thermal resistance in the relief plate that is appropriate for the operating range of the device. Power ICs in particular are often viewed in terms of thermal resistance, and this value determines the level of allowable dissipation in the device.
Specifically, the allowable dissipation in devices such as power ICs is determined by the ambient temperature and head relief plate.

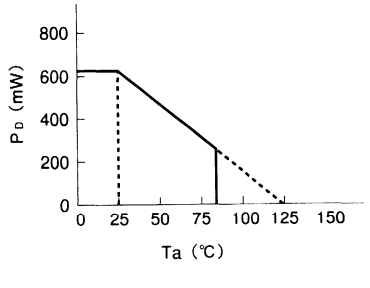


Figure 1. MB3759PF P_D Characteristics (flat package)

Figure 2 shows example characteristics for allowable dissipation. In this case $P_D$max is limited to the level of 18W, and with the ideal heat relief plate (where $T_C=T_A$), the thermal resistance (in which thermal resistance of the relief plate $\theta_f=0$) is given by

$$\theta_{j\text{-}c} = \frac{150℃ - 96℃}{18W} = 3℃/W$$

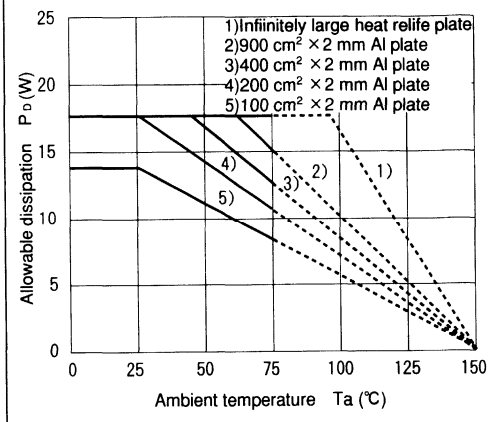


Figure 2. Example Characteristics : Allowable Dissipation

Here the thermal resistance required under the conditions in Figure 3, to operate at T_A=60℃, P_D=15W, is

$$\theta_{j\text{-}a} = \frac{150℃ - 60℃}{15W} = 6℃/W$$

$$\theta_f = \theta_{j\text{-}a} - \theta_{j\text{-}c}$$
$$= 6℃/W - 3℃/W$$
$$= 3℃/W$$

and therefore the area of the heat relief plate is 400cm².

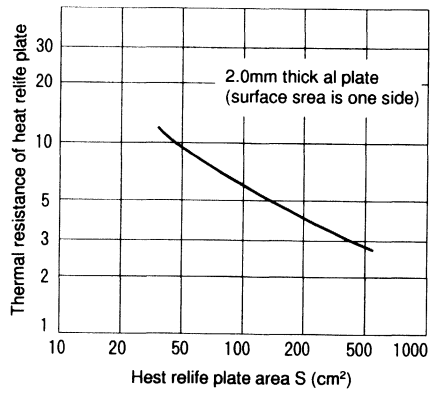


Figure 3. Heat Relief Plate Thermal Resistance Characteristics

7. External Components

ASSP products use external capacitors to determine oscillation frequency, operating time constants, and other variables, and in some cases the use of capacitors with large leak current levels can lead to unwanted variability in timing settings which cause entire systems to operate improperly. Sufficient care must be taken whenever using capacitors that produce large leak currents or external stress levels.

8. Using Power ICs

(1) Precautions for Installation

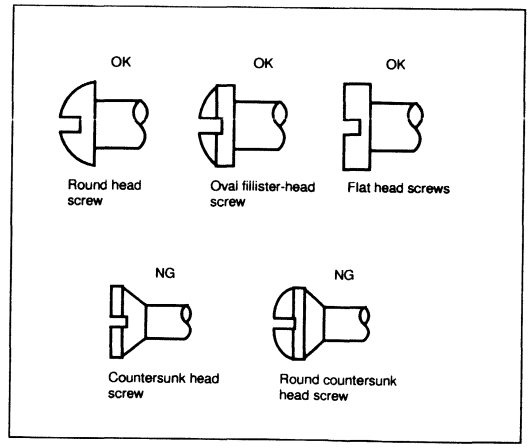
a. When installing a power IC on a heat relief plate, use a torque setting of 4 to 6kg/cm². Levels or 8kg/cm² or higher increase the likelihood of cracking the chip or external package, and conversely the use of too little force may increase thermal resistance and prevent the achievement of desired characteristics. (package with heatsink relief)

b. To realize full heat relief effects the following precautions should be observed in the use of heat relief plates.

- There should be no protrusions, indentations or twisting. Abnormal stress is likely to be a cause of trouble.
- Contact surfaces with heat relief fins should be ground flat.
- Take care that no foreign substances are captured within the contact surfaces.
- All holes for mounting screws must be chamfered.
- Remove surface painting so that tabs can contact the GND circuit.

c. Avoid the use of countersunk head screws or round countersunk head screws. Use screws on which the underside of the head provides a flat surface for contact with the plate, including round head screws, oval fillister-head screws, or flat head screws.

d. Screw hole spacing should match the screw hole spacing on the IC.



(2) Always be sure that external circuit constants agree with the recommended constant values.

External components on the input side require particular attention because they frequently affect device characteristics.

(3) Observe any designated instructions provided with external components

Oscillation damper capacitors should be the non-inductive type.

(4) Refer to recommended patterns for wiring, and use them in design.

Grounding points for input and output GND lines, components, etc. require particular attention because they frequently affect device characteristics.

(5) About Oscillation Damper Capacitors

Use capacitors providing effective capacity of $0.15\,\mu F\,^{+100}_{-20}$ (%) and ESR=0.5 to $2\,\Omega$ at 1 to 10MHz. It is recommended that mylar capacitors have $0.1\,\mu F$ and $1\,\Omega$ series connections.

Also at 10MHz and higher frequencies, the use of low-resonance capacitors is recommended.

(6) Tabs

Heat relief fans must always be grounded.

2 Telephones Products

FUJITSU SEMICONDUCTOR
DATA SHEET

DS04–23203–1E

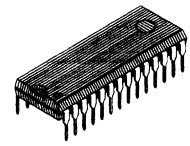
ASSP

TELECOMMUNICATION CIRCUIT

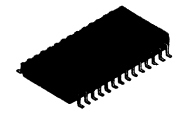
MB4518

The MB4518 provides many of the major speech circuit functions of the telephone handset. Additional features include a level expander circuit to minimize ambient acoustic noise interference and an on-chip amplifier with speaker-drive capability. Combined with general-purpose dialer and tone-ringer ICs, the MB4518 provides all of the basic handset functions.
The MB4518 easily interfaces with microprocessors designed for telephone handset control to provide microprocessor-controlled speaker level, transmitter muting, and side-tone level adjustments. The sidetone level adjustment circuit detects loop current levels and switches between two balance networks for proper sidetone level.

- On-chip power amplifier drives an 8 Ω speaker
- Transmit level expander
- Simple receive level boost
- Balanced transmitter input for improved noise rejection
- Drives low-impedance receiver (dynamic receiver)
- Switchable balance network for optimum side-tone level
- Loop-current monitoring automatic gain control (automatic pad function)
- Low loop current drain ($I_L \fallingdotseq 5$ mA)
- Superior branching properties
- Gain and frequency characteristics adjustable by external resistor and capacitor.
- Simple telephone microcomputer interface
- Available in 28-pin shrink dip and flat packages



PLASTIC PACKAGE
(DIP-28P-M03)



PLASTIC PACKAGE
(FPT-28P-M01)

ABSOLUTE MAXIMUM RATINGS (See NOTE)

(T_A = +25°C)

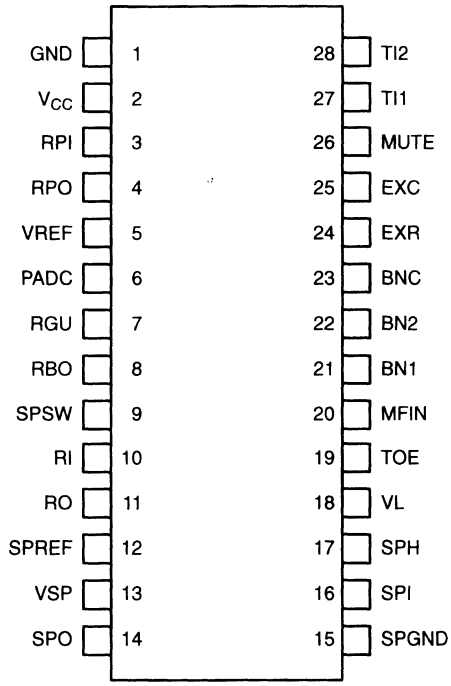
Rating	Symbol	Value	Unit
Supply voltage	V_L	18	V
Supply current	I_L	120	mA
Operating temperature range	Top	–30 to +60	°C
Storage temperature range	Tstg	–55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

PIN ASSIGNMENT

(TOP VIEW)

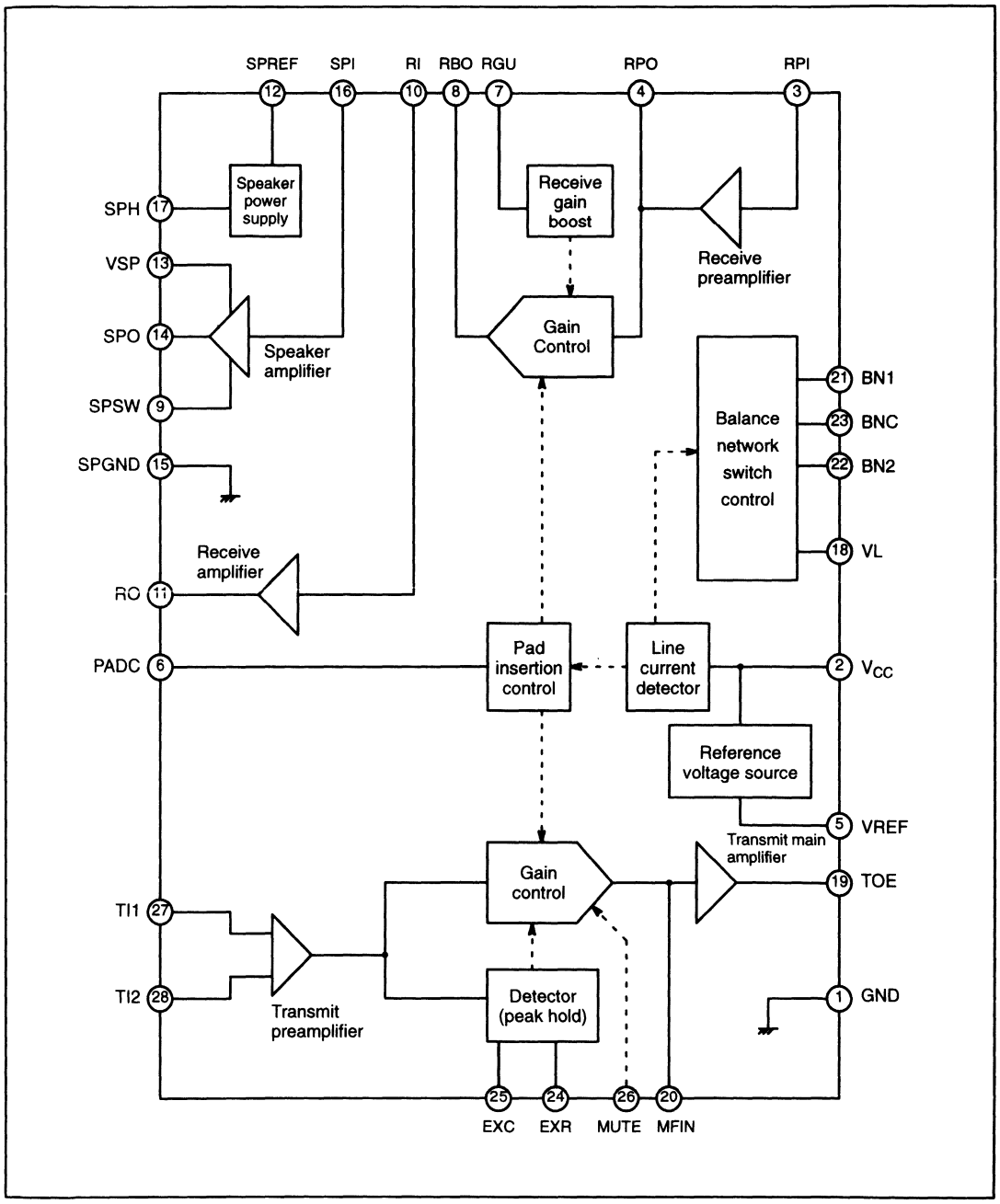


PIN FUNCTIONS

Pin No.	Symbol	I/O	Description
1	GND	–	Chip ground. Connected to the (–) side of an external diode bridge connected to the subscriber loop.
2	V_{CC}	–	Power supply pin. Supplies power to the chip circuits. Coupled from the loop (AC-grounded) by an external capacitor.
3	RPI	I	Receive preamplifier input. Connected to the receive input through an external coupling capacitor.
4	RPO	O	Receive preamplifier output. The receive preamplifier gain and frequency compensation are externally adjusted with a resistor and capacitor connected between this pin and the RPI pin.
5	VREF	–	Reference voltage pin. Connected to the internal reference voltage and AC-grounded through an external capacitor.
6	PADC	–	Pad insertion control. Start-up current for the pad insertion control is adjusted by connecting an external resistor to this pin.
7	RGU	I	Simple receive gain control. Grounding this pin increases the receive preamplifier gain by about 6 dB. Normally left open.
8	RBO	O	Receive buffer output. Connected to the RI and SPI pins through external coupling capacitors.
9	SPSW	I	Speaker defeat switch. When this pin is open, the speaker is connected; when grounded, the speaker is disconnected.
10	RI	I	Receive main amplifier input. The receive signal is coupled to this pin from the RBO pin by an external capacitor.
11	RO	O	Receive main amplifier output. Connected to a low-impedance receiver by an external coupling capacitor. Some receivers may require a shunt capacitor to prevent oscillation.
12	SPREF	–	Speaker circuit reference voltage pin. Reference voltage pin for the speaker and receive output circuit. AC-grounded through an external capacitor.
13	VSP	–	Speaker amplifier power supply pin. The speaker amplifier receives power from this pin. The speaker power supply can be coupled at this point by an external capacitors.
14	SPO	O	Speaker output. Connected to an 8 Ω speaker through an external capacitor. Some applications may require a speaker shunt capacitor to prevent oscillation.

Pin No.	Symbol	I/O	Description
15	SPGND	–	Speaker amplifier ground. This pin must be connected to the circuit network ground.
16	SPI	I	Speaker amplifier input. Connected to the RBO pin through an external capacitor and resistor for adjustment of speaker amplifier gain and frequency compensation.
17	SPH	–	Speaker circuit power control. The speaker power supply circuit is connected to the speaker amplifier input (VSP) through an external network which can be adjusted to control chip power consumption.
18	VL	I	Line input. Connected to the (+) side of an external diode bridge connected to the subscriber loop.
19	TOE	O	Transmit main amplifier output. Connected to the emitter of the transmit transistor.
20	MFIN	I	DTMF signal input. Connected to the base of the transmit output transistor. The input impedance is about 24 kΩ. During voice transmission this pin must be open.
21, 22	BN1, BN2	–	Balance network pins. Used for connection of external balance networks. BN1: Short loop, BN2: Long loop
23	BNC	–	Balance network switching control. An external resistor is connected between this pin and V_{CC} or ground to adjust the BN1 and BN2 switching current.
24	EXR	–	Level expander reference voltage pin. Reference voltage pin for the control of the level expander. Connecting an external capacitor holds the positive peak voltage level.
25	EXC	–	Level expander control. Control pin for the level expander. Connecting an external capacitor holds the negative peak voltage level. When grounded, this pin disables the expander function.
26	MUTE	–	Muting. Grounding this pin suppresses output to the loop. During communication this pin must be left open.
27, 28	TI1, TI2	I	Transmit preamplifier input. Connected to the transmitter through external coupling capacitors. The input is balanced. TI1 is the noninverting input and TI2 is the inverting input.

BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

(T_A = +25°C)

Parameter	Symbol	Value	Unit
Supply voltage	V_L	12	V
Supply current	I_L	20 to 120	mA

ELECTRICAL CHARACTERISTICS

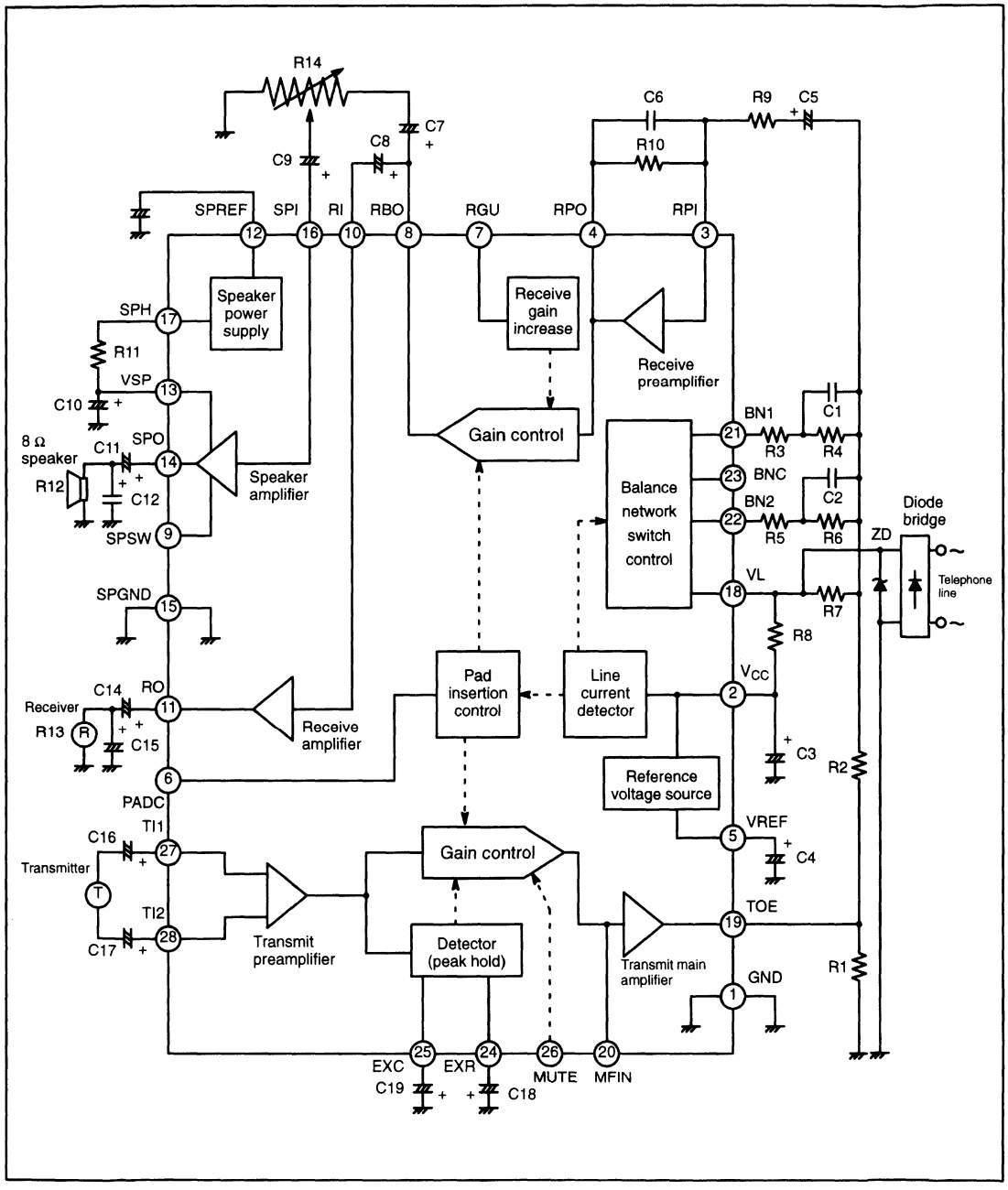
(T_A = +25°C)

Parameter	Symbol	Measurement conditions (f = 1 kHz)	IL (mA)	Value Min	Value Typ	Value Max	Unit
Handset DC voltage	V_{L1}	–	20	2.9	3.2	3.5	V
	V_{L2}		90	6.0	6.5	7.0	V
Supply voltage	V_{CC}	–	20	1.3	1.6	1.9	V
Handset AC impedance	Z_{TEL1}	–	30	500	600	700	Ω
	Z_{TEL2}		90	500	600	700	Ω
Transmit circuit gain	G_{TV1}	V_{IN} = –50 dBV	30	38.0	41.0	44.0	dB
	G_{TV2}	V_{IN} = –50 dBV	90	36.5	39.5	42.5	dB
	ΔG_{TV}	$\Delta G_{TV} = G_{TV}$ (V_{IN} = –50 dBV) – G_{TV} (V_{IN} = –65 dBV)	30	4.0	7.0	10.0	dB
Transmit circuit dynamic range	D_{T1}	Distortion attenuation: ≥ 20 dB	30	–0.5	2.5	–	dBV
	D_{T2}		90	4.5	7.5	–	dBV
Transmit circuit residual noise	NT *	–	–	–	–	–56	dBV
Receive circuit gain	G_{RV1}	V_{IN} = –30 dBV	30	–8.0	–5.0	–2.0	dB
	G_{RV2}	V_{IN} = –30 dBV	90	–13.0	–10.0	–7.0	dB
Receive circuit gain increase	G_{RUP}	V_{IN} = –30 dBV	30	4.0	6.0	8.0	dB
Receive circuit dynamic range	D_{R1}	Distortion attenuation: ≥ 20 dB	30	–15.0	–12.0	–	dBV
	D_{R2}		90	–10.5	–7.5	–	dBV
Speaker circuit gain	G_{SV1}	V_{IN} = –30 dBV	30	4.0	7.0	10.0	dB
	G_{SV2}	V_{IN} = –30 dBV	90	0.0	3.0	6.0	dB
Speaker circuit dynamic range	D_{S1}	Distortion attenuation: ≥ 20 dB	30	–22.0	–19.0	–	dBV
	D_{S2}		90	–11.5	–8.5	–	dBV
Balance network switching	I_{FN}	Far near	–	43.0	55.0	70.0	mA
	I_{NF}	Near far	–	32.5	42.5	52.5	mA
	I_H	Hysteresis width	–	9.0	12.5	27.5	mA

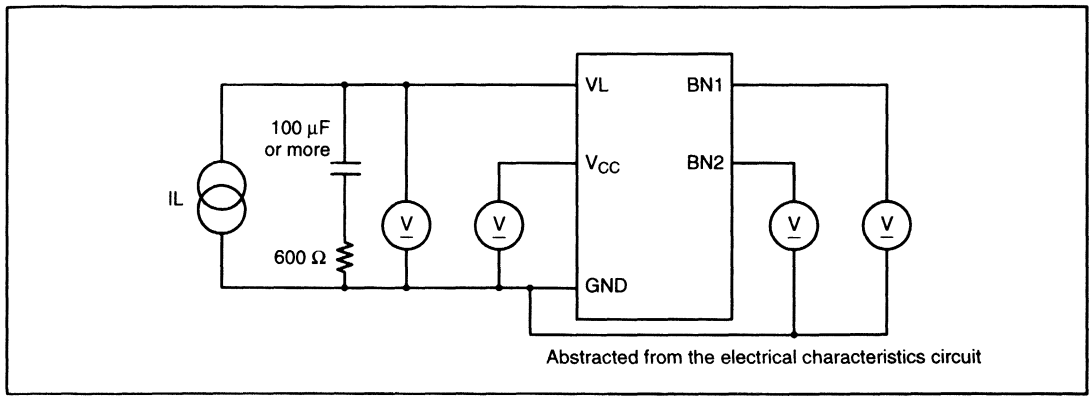
* : Design guaranteed

TEST CIRCUITS

- **Test circuit**



- **DC characteristics test circuit**



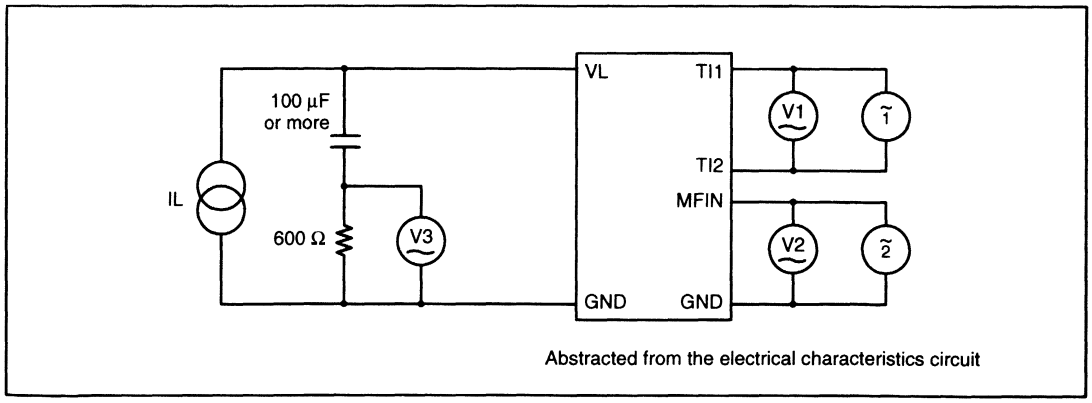
IL : Current source (AC impedance ≥ 60 kΩ, 1 kHz, 30 mA)

Ⓥ : DC voltmeter

- Balance network switching I_{FN} : When IL increases from 30 mA to 70 mA
  IL (mA) for which VBN2 increases from 1.5 V to 3.5 V or more
  I_{NF} : When IL decreases from 70 mA to 30 mA
  IL (mA) for which VBN1 decreases from 3.5 V to 1.5 V or less

Note: The tolerance of the load impedance for each pin shall be ±1%. (All test circuits)

- **Transmission characteristics test circuit**



Ⓒ : Oscillator (Output impedance and DC resistance ≤ 4 Ω at 1 kHz)

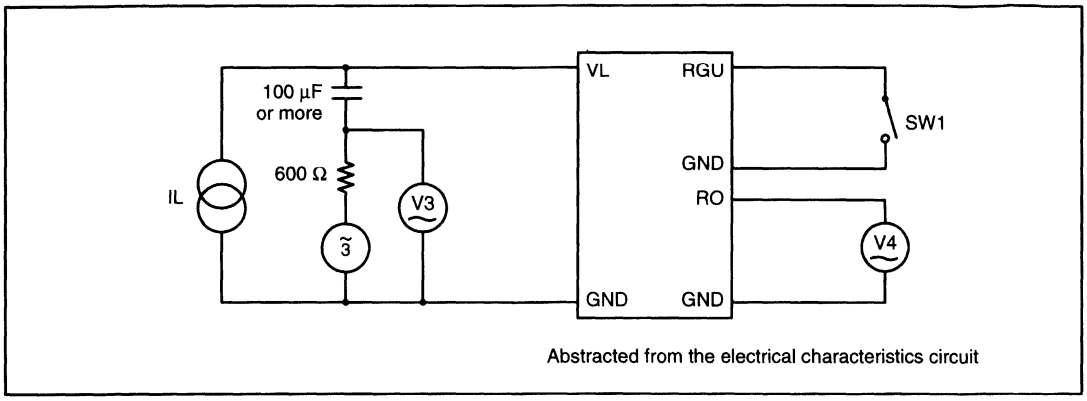
IL : Current source (AC impedance ≥ 60 kΩ, 1 kHz, 30 mA)

Ⓥ : AC voltmeter

Transmit circuit gain: G_{TV} (dB) = 20 Log V3/V1 (oscillator 1)
G_{MFV} (dB) = 20 Log V3/V2 (oscillator 2)

- Dynamic range : The distortion attenuation with the output signal level fixed is at least 20 dB.
- Residual noise : Measure the transmit output signal level with no transmit input signal.

- **Receive characteristics test circuit**

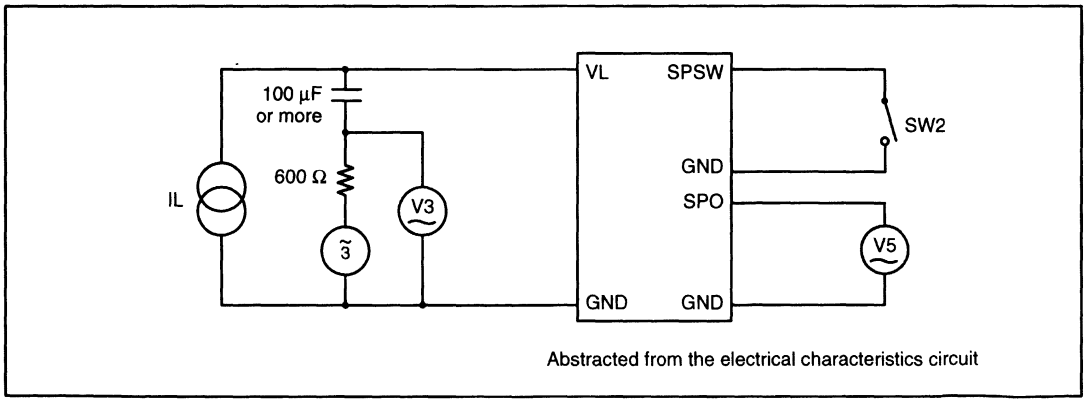


Abstracted from the electrical characteristics circuit

(~) : Oscillator (Output impedance and DC resistance ≤ 4 Ω, f = 1 kHz)
IL : Current source (AC impedance ≥ 60 kΩ, 1 kHz, 30 mA)
(V) : AC voltmeter
Receive circuit gain: G_{RV} (dB) = 20 Log V4/V3

- Gain boost : Measure the V3 AC signal level boost when SW1 is closed.
- Dynamic range : The distortion attenuation with the output signal level fixed is at least 20 dB.

- **Speaker characteristics test circuit**



Abstracted from the electrical characteristics circuit

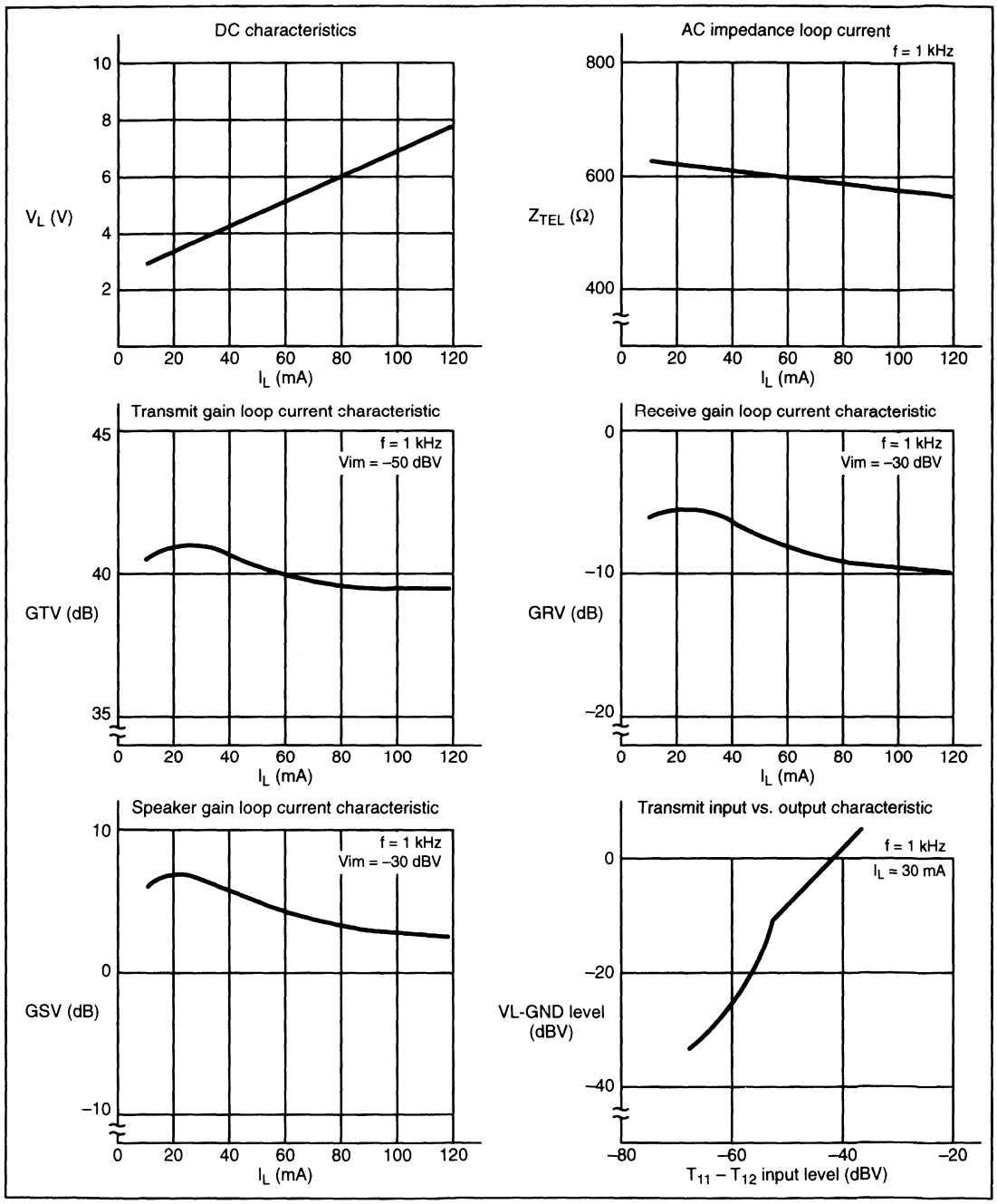
(~) : Oscillator (Output impedance and DC resistance ≤ 4 Ω, f = 1 kHz)
IL : Current source (AC impedance ≥ 60 kΩ, 1 kHz, 30 mA)
(V) : AC voltmeter
Speaker system gain: G_{SV} (dB) = 20 Log V5/V3 (SW2 open)

- Dynamic range : The distortion attenuation with the output signal level fixed is at least 20 dB.

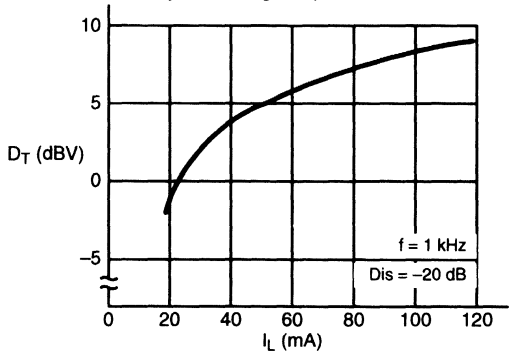
- **Test circuit components**

Reference Designation	Component	Values	Remarks
R1	Resistor	82 Ω F, 1/8 W or more	
R2	Resistor	820 Ω F, 1/16 W or more	
R3	Resistor	2.4 kΩ F, 1/16 W or more	
R4	Resistor	8.2 kΩ F, 1/16 W or more	
R5	Resistor	1.5 kΩ F, 1/16 W or more	
R6	Resistor	6.2 kΩ F, 1/16 W or more	
R7	Resistor	5.6 kΩ F, 1/16 W or more	
R8	Resistor	680 Ω F, 1/16 W or more	
R9	Resistor	5.6 kΩ F, 1/16 W or more	
R10	Resistor	27 kΩ F, 1/16 W or more	
R11	Resistor	10 Ω F, 1/8 W or more	
R12	Resistor	8 Ω F, 1/8 W or more	Speaker
R13	Resistor	150 Ω F, 1/16 W or more	Receiver
R14	Resistor	20 kΩ or more F, 1/16 W or more	
C1	Capacitor	0.027 µF, 16 V or more, ±1%	
C2	Capacitor	0.015 µF, 16 V or more, ±1%	
C3	Capacitor	220 µF, 5 V or more, ±5%	
C4	Capacitor	100 µF, 3 V or more, ±5%	
C5	Capacitor	2.2 µF, 3 V or more, ±1%	
C6	Capacitor	2000 PF, 3 V or more, ±1%	
C7	Capacitor	2.2 µF, 5 V or more, ±5%	
C8	Capacitor	2.2 µF, 5 V or more, ±5%	
C9	Capacitor	2.2 µF, 5 V or more, ±5%	
C10	Capacitor	1000 µF, 5 V or more, ±5%	
C11	Capacitor	220 µF, 3 V or more, ±5%	
C12	Capacitor	2.2 µF, 3 V or more, ±5%	
C13	Capacitor	100 µF, 3 V or more, ±5%	
C14	Capacitor	100 µF, 3 V or more, ±5%	
C15	Capacitor	0.47 µF, 3 V or more, ±5%	
C16	Capacitor	2.2 µF, 3 V or more, ±1%	
C17	Capacitor	2.2 µF, 3 V or more, ±1%	
C18	Capacitor	2.2 µF, 5 V or more, ±1%	
C19	Capacitor	2.2 µF, 5 V or more, ±1%	

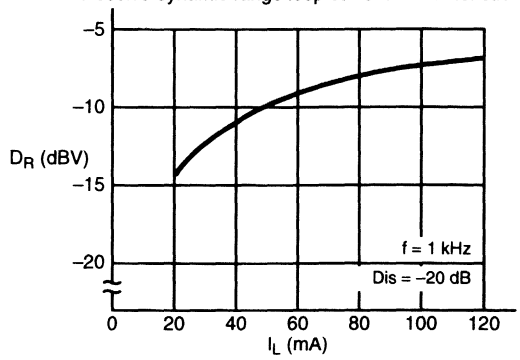
TYPICAL CHARACTERISTIC CURVES



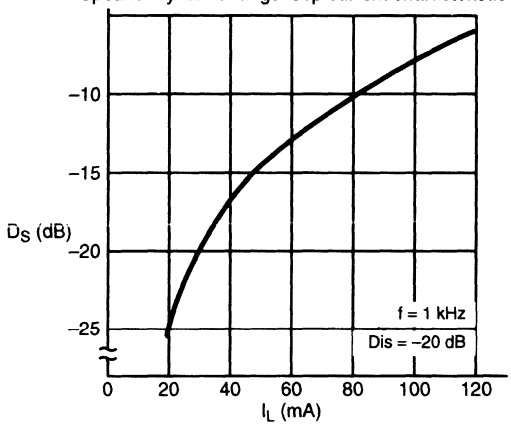
Transmit dynamic range loop current characteristic



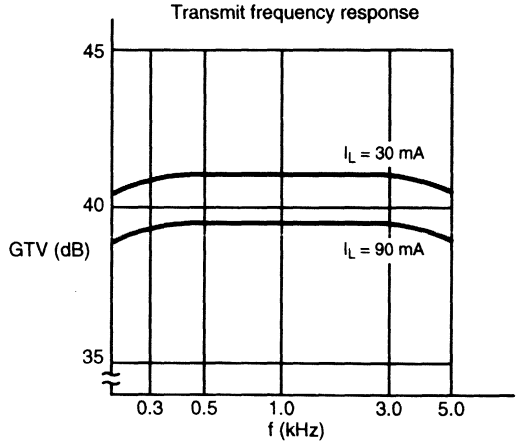
Receive dynamic range loop current characteristic



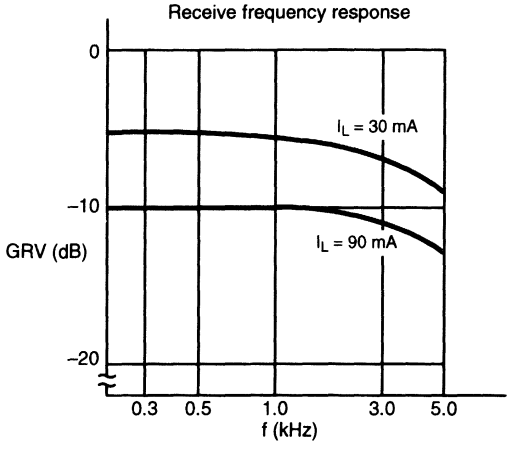
Speaker dynamic range loop current characteristic



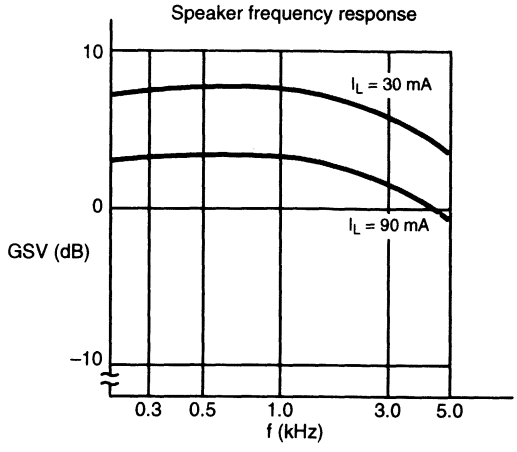
Transmit frequency response



Receive frequency response



Speaker frequency response



MEMO

FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-23002-2E

ASSP

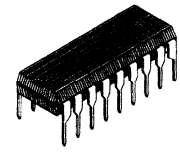
DTMF RECEIVER

MB87017B

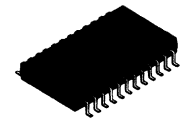
DUAL TONE MULTI FREQUENCY RECEIVER

The MB87017B is a one chip DTMF receiver with an input amplifier gain adjuster and low power consumption, integrating filter and decoder circuits. The MB87017B can select either automatic guard time setting mode or adjustable external guard time setting mode.
This circuit consists of SCFs (Switched Capacitor Filters) and decoders which convert 16 types of DTMF tone pairs into hexadecimal four-bit codes.

- All DTMF receiver functions are integrated on one chip.
- Low power consumption
- Built-in input amplifier gain adjustment circuit
- Selectable automatic or adjustable external guard time setting modes



PLASTIC PACKAGE
(DIP-18P-M02)



PLASTIC PACKAGE
(FPT-24P-M02)

ABSOLUTE MAXIMUM RATINGS (See NOTE)

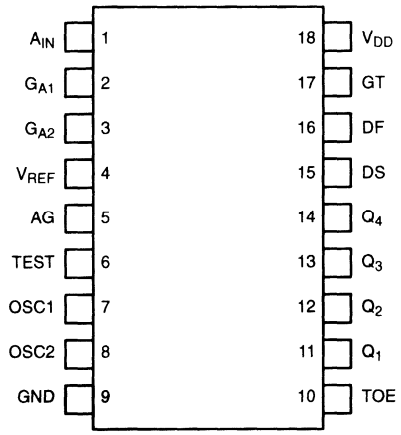
Ratings	Symbol	Value	Unit
Supply Voltage	V_{DD}	+6.0	V
Analog Input Voltage	V_{AIN}	−0.3 to V_{DD} + 0.3	V
Digital Input Voltage	V_{DIN}	−0.3 to V_{DD} + 0.3	V
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{STG}	−55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

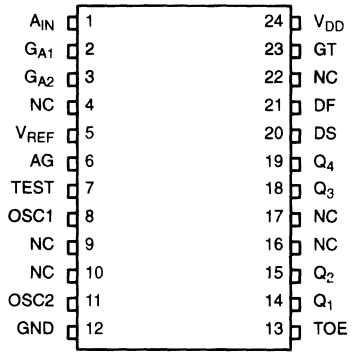
PIN ASSIGNMENT

PIN ASSIGNMENT
(TOP VIEW)



(DIP-18P-M02)

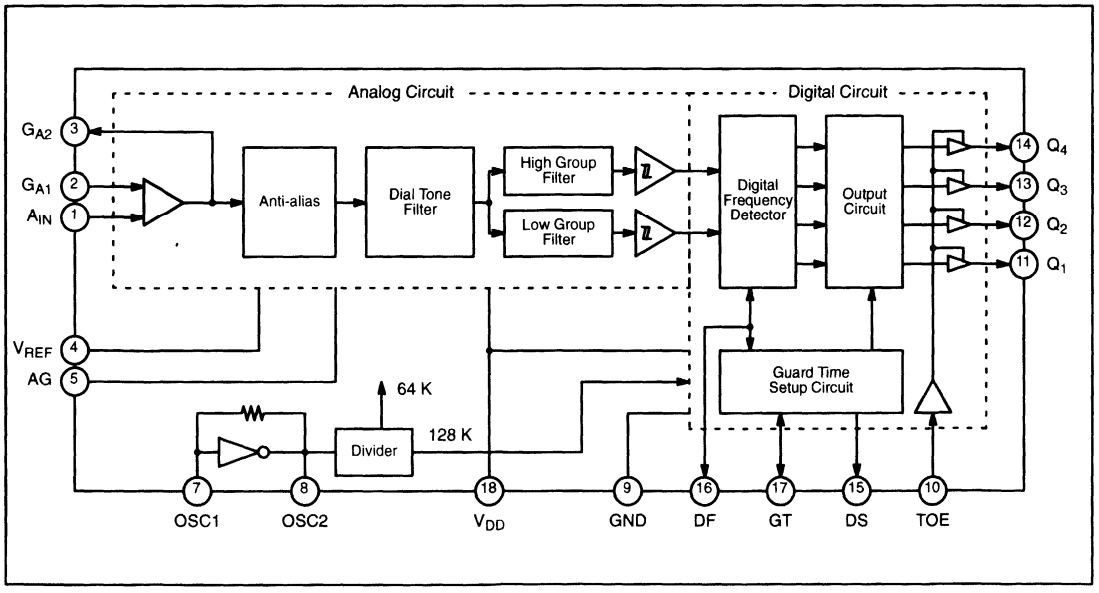
PIN ASSIGNMENT
(TOP VIEW)



(FPT-24P-M02)

BLOCK DIAGRAM

(DIP PACKAGE)



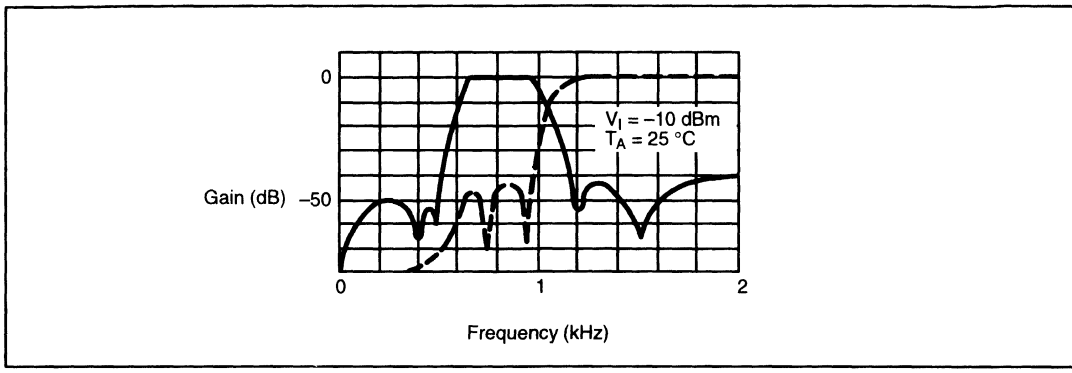
PIN DESCRIPTIONS

Pin Number		Symbol	I/O	Description
DIP	FPT			
1	1	A_{IN}	I	Analog input pin (non-inverted operational amplifier input)
2	2	G_{A1}	I	Operational amplifier gain adjustment pin 1 (inverted operand amplifier input). Operational amplifier gain adjustment pin 2 (operand amplifier output pin). * These pins are provided for operational amplifier gain adjustment. The polarity of G_{A1} is opposite to that of G_{A2}.
3	3	G_{A2}	O	
4	5	V_{REF}	O	Reference voltage output pin. (1/2 V_{DD})
5	6	AG	–	Analog ground pin
6	7	TEST	–	Test pin. Usually set to ground level.
7	8	OSC1	I	Clock input pin. Clock output pin. * Connect a 3.5795 MHz crystal between OSC1 and OSC2 pins.
8	11	OSC2	O	
9	12	GND	–	Ground pin
10	13	TOE	I	Three-state output enable pin. * Data from Q_1 to Q_4 may be output when this pin is set to "High".
11 to 14	14, 15 18, 19	Q_1 to Q_4	O	Three-state data output pin.
15	20	DS	O	Signal detection pin. * This pin goes to "High" when an valid tone pair is received and decoded, and the data in the output data-bus is updated.
16	21	DF	O	Frequency detection pin. * This pin goes to "High" when a received tone pair is acknowledged as the valid DTMF signal frequency.
17	23	GT	O	Guard time mode select pin. * When GT pin is clamped to V_{DD}, automatic guard time setting circuit is selected; Guard Time Present (GTP) and Guard Time Absent (GTA) are set to 20 milliseconds. * See functional descriptions on page 5. * When GT pin exceeds 1/2V_{DD}, DS pin outputs high level. When GT pin is less than 1/2V_{DD}, DS pin outputs low level.
18	24	V_{DD}	–	Positive supply voltage pin. * The voltage must be +5 V ±5%.
–	4, 9 10, 16 17, 22	NC	–	No connection

FUNCTIONAL DESCRIPTIONS

FILTER

The filters consist of 3 sixth-order SCFs. The dial tone removal filter (including the 60 Hz filter) output is connected to the individual hysteresis comparators through the low group and high group filters.
In the figure below, the solid line shows the characteristics of the low group filter while the broken line shows the characteristics of the high group filter. At a frequency of 770 Hz it is assumed that 0 dB are lost, therefore this point is used for reference.



DECODER

1. Digital Frequency-detecting Circuit

The DF (Detect Frequency) pin goes to "High" when the detector circuit acknowledges the output signals from the two comparators as valid DTMF signal frequencies in the digital frequency detecting block.

2. Guard Time Setting Circuit

Automatic or adjustable external guard time setting modes are provided. Guard time has two types: GTP (Guard Time Present) and GTA (Guard Time Absent).

2.1 Automatic Guard Time Setting Circuit

When GT pin is clamped to V_{DD}, automatic guard time setting circuit is selected; t_{GTP} and t_{GTA} are set to 20 milliseconds. The output signal from the filters may be acknowledged as a DTMF signal if:

① A signal with valid DTMF frequency lasts more than 40 milliseconds. This signal is decoded into a DTMF signal. These pulses correspond to the input signal enable period and disable period for alternative current characteristics.

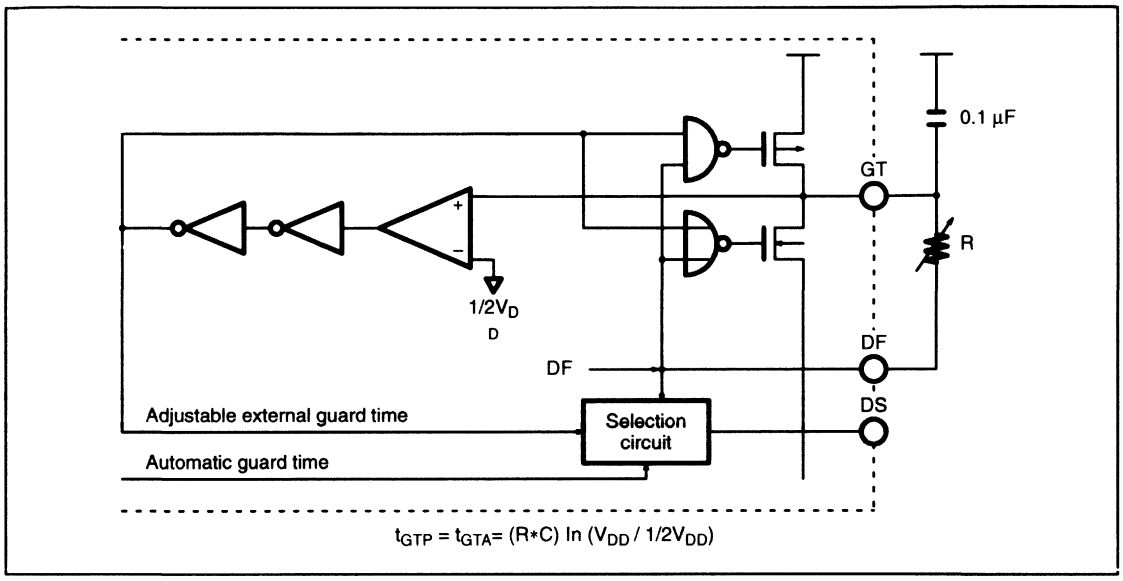
② A period of more than 40 milliseconds exists between DTMF signals n and (n + 1). If this is not the case the DTMF signal (n + 1) is disabled.
These pulses correspond to the inter-digit pauses for acceptance and rejection for alternative current characteristics.

In ①, it takes the DS (Detect Signal) pin GTP to acknowledge that the input signal is a DTMF signal after DF switches to "High". The DS pin switches to "High" when the input signal is acknowledged as a DTMF signal.
In ②, it takes the DS pin GTA to disable DTMF signal n after DF switches to "Low". The DS pin switches to "Low" when the signal is disabled. (See Page 10 for the timing chart.)

$$t_{SDA} > t_{GTP} + t_{PDF}$$
$$t_{IDA} > t_{ADF} + t_{GTA}$$

2.2 Adjustable External Guard Time Setting Circuit

The simplified adjustable external guard time setting circuit shown below enables any guard time present (GTP) or guard time absent (GTA) setting.
The guard time is adjusted by selecting external register R when the external capacitor is 0.1 µF.



2.3 Automatic Guard-time/Adjustable External Guard-time Setting Mode Selection Circuit

- Adjustable external guard time setting mode
  Adjustable external guard time setting mode (GT pin is set low) is selected on the rising edge of the detected frequency (DF).
- Automatic guard time setting mode
  The automatic guard time setting mode (GT pin is set high) is selected the power-on reset signal and on the rising edges of the DF.

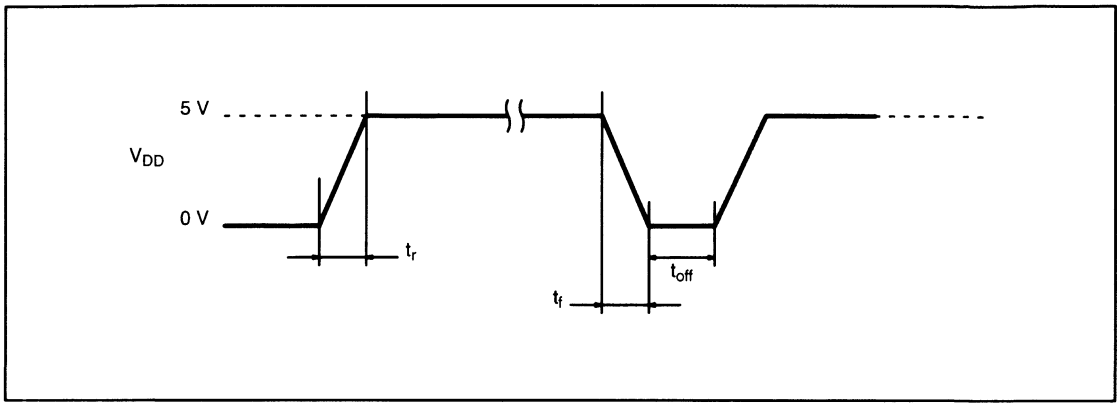
2.4 Power-on Reset Circuit

The power-on reset circuit generates a reset signal to initialize the automatic guard time or adjustable guard time setting circuit when power is applied.
The power-on reset circuit specifications and timing diagram are shown below.

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Remarks
Power supply rise time Power supply fall time	t_r t_f	0.1	–	50	ms	Power-on reset operation conditions
Power-off time	t_{off}	100	–	–	ms	

FUNCTIONAL DESCRIPTIONS

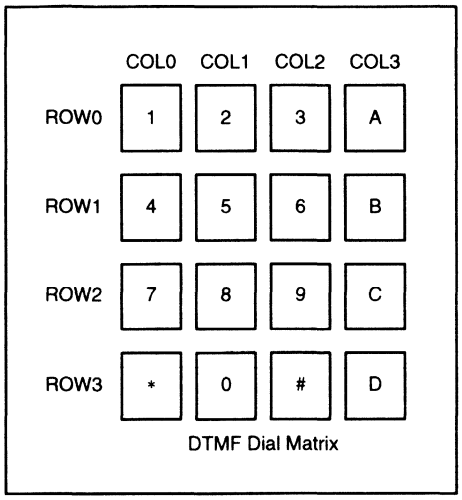
- Power-on reset timing diagram



NOTE: If the values of power supply rise time, fall time, and power off time shown in the table are not satisfied, the power-on reset signal will not be generated and the automatic guard time setting circuit may not recover from malfunction (receive disabled).
The adjustable external guard time setting circuit will not enter malfunction even if the power-on reset signal is not generated.
Therefore, if power supply conditions disable the power-on reset circuit, the adjustable external guard setting circuit can be used.

OUTPUT CIRCUIT

When the signal detector pin (DS) switches to "High", a received tone pair is stored in the output circuit register. The output latch status may be output on the output bus by setting the three state control input (TOE) to "High".

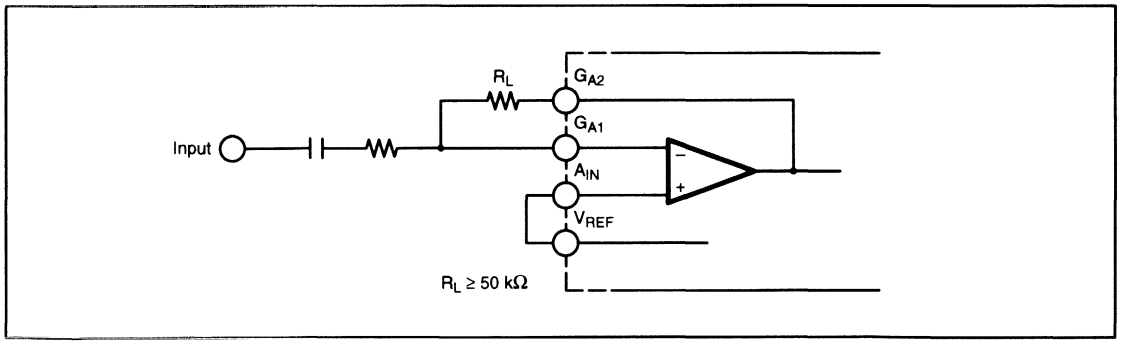


DTMF Dial Matrix

Dial	A_{IN} Input		Input	Output			
	Low group: fo	High group: fo	TOE	Q_4	Q_3	Q_2	Q_1
1	697	1209	1	0	0	0	1
2	697	1336	1	0	0	1	0
3	697	1477	1	0	0	1	1
4	770	1209	1	0	1	0	0
5	770	1336	1	0	1	0	1
6	770	1477	1	0	1	1	0
7	852	1209	1	0	1	1	1
8	852	1336	1	1	0	0	0
9	852	1477	1	1	0	0	1
0	941	1336	1	1	0	1	0
*	941	1209	1	1	0	1	1
#	941	1477	1	1	1	0	0
A	697	1633	1	1	1	0	1
B	770	1633	1	1	1	1	0
C	852	1633	1	1	1	1	1
D	941	1633	1	0	0	0	0

SAMPLE DIFFERENCE INPUT CONFIGURATION

The MB87017B uses a difference input amplifier and provides for a bias power source (V_{REF}) to apply a bias voltage to the input signal. This also allows a pin to connect a gain adjustment resistor to the amplifier output.



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Rating			Unit
		Minimum	Typical	Maximum	
Supply Voltage	V_{DD}	4.75	5.0	5.25	V
Input Voltage	V_I	0	–	V_{DD}	V
Oscillation Frequency	f_{OSC}	3.5759	3.5795	3.5831	MHz
OSC1 Pin Load Capacitance	C_{LDI}	10.0	–	50.0	pF
OSC2 Pin Load Capacitance	C_{LDO}	10.0	–	50.0	pF
GA2 Pin Load Resistance	R_{LA}	50	–	–	kΩ
GA2 Pin Load Capacitance	C_{LA}	–	–	100	pF
Operating temperature	T_A	0	–	70	°C

DC CHARACTERISTICS

V_{DD} = 5 V ±5%, T_A = 0°C to 70°C

Parameter	Symbol	Condition	Rating			Unit
			Minimum	Typical	Maximum	
Power Consumption	P_D	f = 3.58 MHz, V_{DD} = 5 V	–	25	37	mW
Low Level Input Voltage	V_{IL}		0	–	0.8	V
High Level Input Voltage	V_{IH}		2.0	–	V_{DD}	V
Low Level Input Leak Current	I_{IL}	V_I = GND	–10	–	10	μA
High Level Input Leak Current	I_{IH}	V_I = V_{DD}	–10	–	10	μA
Low Level Output Voltage	V_{OL}	I_{OL} = 2 mA	0	–	0.4	V
High Level Output Voltage	V_{OH}	I_{OH} = –0.4 mA	2.4	–	V_{DD}	V
V_{REF} Output Voltage	V_{REF}		–	2.5	–	V

AC CHARACTERISTICS

V_{DD} = 5 V ±5%, T_A = 0°C to 70°C

Parameter	Symbol	Condition	Rating			Unit
			Minimum	Typical	Maximum	
Signal Input Level *1		T_A = 25°C, V_{DD} = 5 V	−29	−10	−1	dBm
TWIST *2			−	±10	−	dB
Allowable Frequency Deviation			±1.5 ±2 Hz	−	−	%
Prohibited Frequency Deviation			±3.5	−	−	%
Allowable Noise Level *3			−	−12	−	dB
Allowable Dial Tone Level *4			−	22	−	dB
Input Signal Detection Timing (Present) *5	t_{PDF}		5	11	14	ms
Input Signal Detection Timing (Absent) *5	t_{ADF}		0.5	4	8.5	ms
Input Signal Enable Period (Accept) *5, 6	t_{SDA}		−	−	40	ms
Input Signal Enable Period (Reject) *5, 6	t_{SDR}		20	−	−	ms
Inter-digit Pause (Accept) *5, 6	t_{IPA}		−	−	40	ms
Inter-digit Pause (Reject) *5, 6	t_{IPR}		9	−	−	ms
Input Clock Frequency	f_{IN}		3.5759	3.5795	3.5831	MHz
Clock Rise Time	tr		−	−	110	ns
Clock Fall Time	tf		−	−	110	ns
Clock Duty	DR		−	50	−	%

*1 dBm: 600 ohm reference

*2 TWIST = High group tone voltage/Low group tone voltage

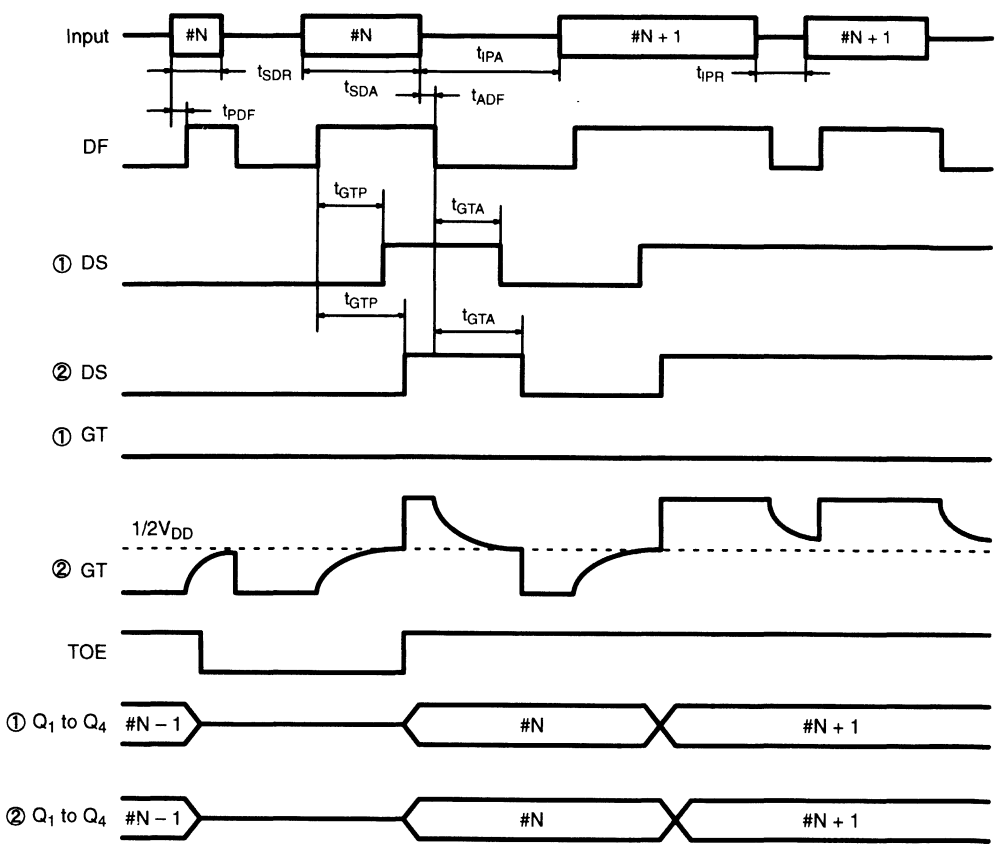
*3 Allowable noise = Total allowable noise within the range 300 Hz to 3.4 kHz/Minimum amplitude tone level in valid tone pairs

*4 Allowable dial tone level = Total allowable normal dial tone volume/Minimum amplitude tone in valid tone pairs

*5 See Timing Chart.

*6 Specified values are referenced to the automatic guard time setting mode.
See page 5 for t_{GTP} and t_{GTA} in the adjustable external guard time setting mode.

TIMING CHART



NOTE: ① Automatic guard time setting mode (GT pin is clamped to V_{DD})
② Adjustable external guard time setting mode (See circuit on page 5)

FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-23001-4E

ASSP

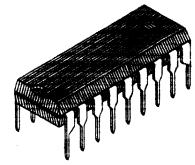
DTMF RECEIVER

MB87057

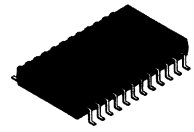
DUAL TONE MULTI FREQUENCY RECEIVER

The MB87057 is a one chip DTMF receiver with an input amplifier gain adjuster and low power consumption, integrating filter and decoder circuits. The MB87057 can automatically set guard times.
This circuit consists of SCFs (Switched Capacitor Filters) and decoders which convert 16 types of DTMF tone pairs into hexadecimal four-bit codes.

- All DTMF receiver functions are integrated on one chip.
- Low power consumption
- Built-in input amplifier gain adjustment circuit
- Automatic guard time setup



PLASTIC PACKAGE
(DIP-18P-M02)



PLASTIC PACKAGE
(FPT-24P-M02)

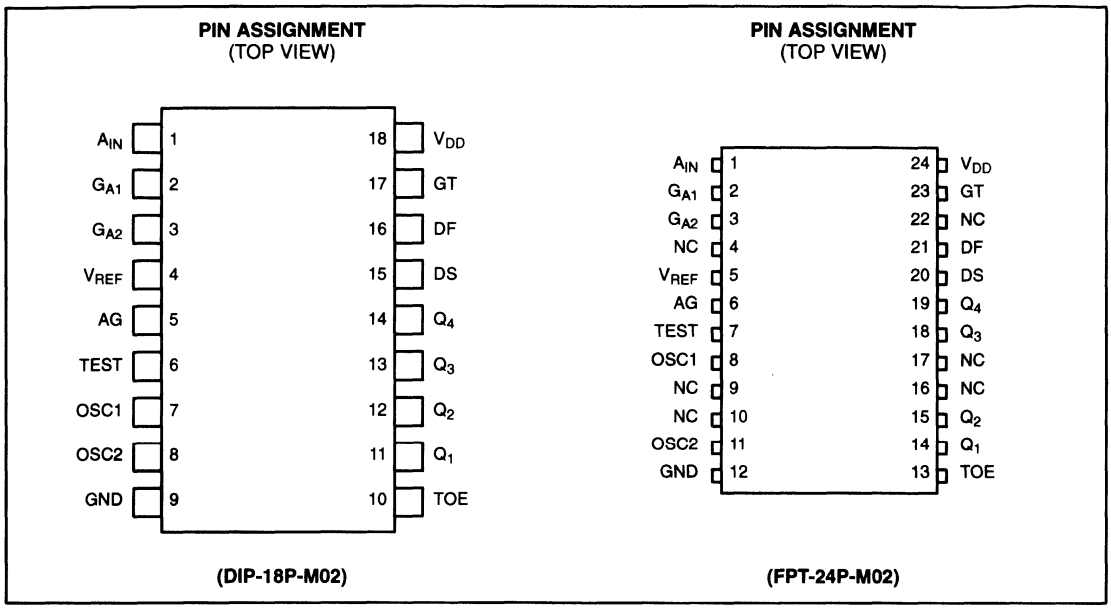
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Ratings	Symbol	Value	Unit
Supply Voltage	V_{DD}	+6.0	V
Analog Input Voltage	V_{AIN}	−0.3 to V_{DD} + 0.3	V
Digital Input Voltage	V_{DIN}	−0.3 to V_{DD} + 0.3	V
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

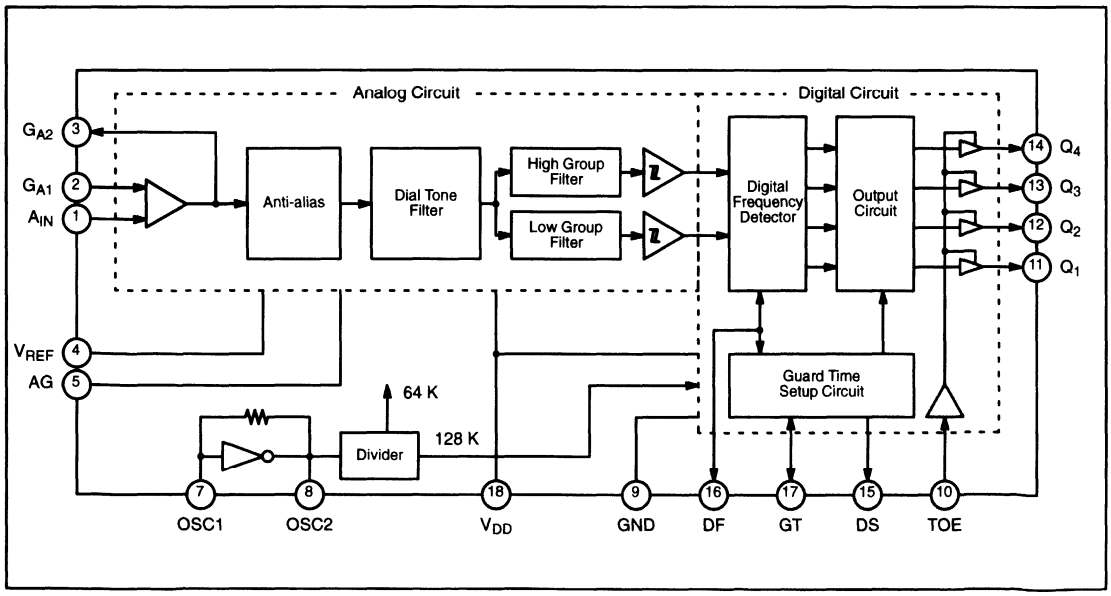
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

PIN ASSIGNMENT



BLOCK DIAGRAM

(DIP PACKAGE)



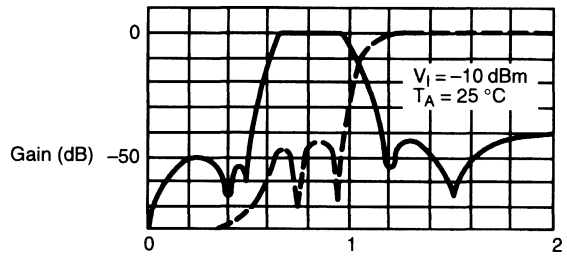
PIN DESCRIPTIONS

Pin Number		Symbol	I/O	Description
DIP	FPT			
1	1	A_{IN}	I	Analog input pin (non-inverted operational amplifier input)
2	2	G_{A1}	I	Operational amplifier gain adjustment pin 1 (inverted operand amplifier input). Operational amplifier gain adjustment pin 2 (operand amplifier output pin). * These pins are provided for operational amplifier gain adjustment. The polarity of G_{A1} is opposite to that of G_{A2}.
3	3	G_{A2}	O	
4	5	V_{REF}	O	Reference voltage output pin. (1/2 V_{DD})
5	6	AG	–	Analog ground pin
6	7	TEST	–	Test pin. Usually set to ground level.
7	8	OSC1	I	Clock input pin. Clock output pin. * Connect a 3.5795 MHz crystal between OSC1 and OSC2 pins.
8	11	OSC2	O	
9	12	GND	–	Ground pin
10	13	TOE	I	Three-state output enable pin. * Data from Q_1 to Q_4 may be output when this pin is set to "High".
11 to 14	14, 15 18, 19	Q_1 to Q_4	O	Three-state data output pin.
15	20	DS	O	Signal detection pin. * This pin goes to "High" when an available tone pair is received and decoded, and the data in the output data-bus is updated.
16	21	DF	O	Frequency detection pin. * This pin goes to "High" when a received tone pair is acknowledged as the valid DTMF signal frequency.
17	23	GT	O	Since "H" has been output, secure the pin in the "Open" or V_{DD} position.
18	24	V_{DD}	–	Positive supply voltage pin. * The voltage must be +5 V ±5%.
–	4, 9 10, 16 17, 22	NC	–	No connection

FUNCTIONAL DESCRIPTIONS

1. FILTER

The filters consist of 3 sixth-order SCFs. The dial tone removal filter (including the 60 Hz filter). Output is connected to the individual hysteresis comparators through the low group and high group filters.
In the figure below, the solid line shows the characteristics of the low group filter while the broken line shows the characteristics of the high group filter. At a frequency of 770 Hz it is assumed that 0 dB are lost, therefore this point is used for reference.



2. DECODER

2.1 Digital Frequency-detecting Circuit

The DF (Detect Frequency) pin goes to "High" when the detector circuit acknowledges the output signals from the two comparators as valid DTMF signal frequencies in the digital frequency detecting block.

2.2 Guard Time Setup Circuit

The automatic setup mode is provided for guard time setup. Guard time has two types: GTP (Guard Time Present) and GTA (Guard Time Absent).

2.2.1 Automatic guard-time setup circuit

The automatic guard time setup circuit sets both t_{GTP} and t_{GTA} to 20 ms. The output signal from the filters may be acknowledged as a DTMF signal if:

① A signal with valid DTMF frequency lasts more than 40 ms. This signal is decoded into a DTMF signal. These pulses correspond to the input signal enable period and disable period for alternative current characteristics.

② A period of more than 40 ms exists between DTMF signals n and (n + 1). If this is not the case the DTMF signal (n + 1) is disabled.
These pulses correspond to the inter-digit pauses for acceptance and rejection for alternative current characteristics.

In ①, it takes the DS (Detect Signal) pin GTP to acknowledge that the input signal is a DTMF signal after DF switches to "High". The DS pin switches to "High" when the input signal is acknowledged as a DTMF signal.

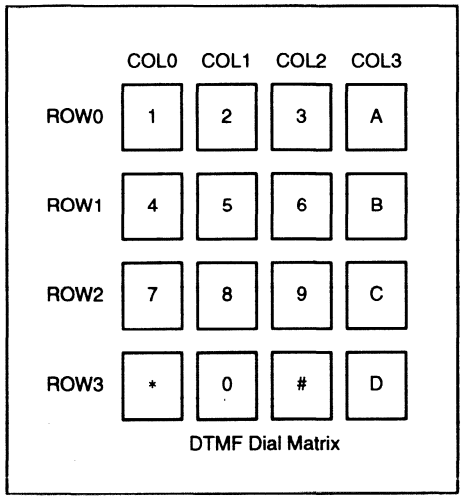
In ②, it takes the DS pin GTA to disable DTMF signal n after DF switches to "Low". The DS pin switches to "Low" when the signal is disabled. (See Page 8 for the timing chart.)

$$t_{SDA} > t_{GTP} + t_{PDF}$$
$$t_{IDA} > t_{ADF} + t_{GTA}$$

FUNCTIONAL DESCRIPTIONS

3. OUTPUT CIRCUIT

When the signal detector pin (DS) switches to "High", a received tone pair is stored in the output circuit register. The output latch status may be output on the output bus by setting the three state control input (TOE) to "High".

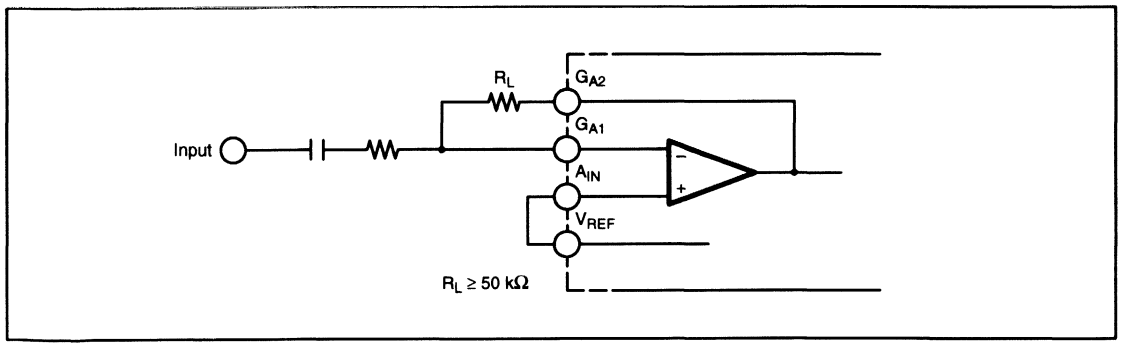


DTMF Dial Matrix

Dial	A_{IN} Input		Input	Output			
	Low group: fo	High group: fo	TOE	Q_4	Q_3	Q_2	Q_1
1	697	1209	1	0	0	0	1
2	697	1336	1	0	0	1	0
3	697	1477	1	0	0	1	1
4	770	1209	1	0	1	0	0
5	770	1336	1	0	1	0	1
6	770	1477	1	0	1	1	0
7	852	1209	1	0	1	1	1
8	852	1336	1	1	0	0	0
9	852	1477	1	1	0	0	1
0	941	1336	1	1	0	1	0
*	941	1209	1	1	0	1	1
#	941	1477	1	1	1	0	0
A	697	1633	1	1	1	0	1
B	770	1633	1	1	1	1	0
C	852	1633	1	1	1	1	1
D	941	1633	1	0	0	0	0

4. SAMPLE DIFFERENCE INPUT CONFIGURATION

The MB87057 uses a difference input amplifier and provides for a bias power source (V_{REF}) to apply a bias voltage to the input signal. This also allows a pin to connect a gain adjustment resistor to the amplifier output.



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Rating			Unit
		Minimum	Typical	Maximum	
Supply Voltage	V_{DD}	4.75	5.0	5.25	V
Input Voltage	V_I	0	–	V_{DD}	V
Oscillation Frequency	f_{OSC}	3.5759	3.5795	3.5831	MHz
OSC1 Pin Load Capacitance	C_{LDI}	10.0	–	50.0	pF
OSC2 Pin Load Capacitance	C_{LDO}	10.0	–	50.0	pF
GA2 Pin Load Resistance	R_{LA}	50	–	–	kΩ
GA2 Pin Load Capacitance	C_{LA}	–	–	100	pF
Operating temperature	T_A	0	–	70	°C

DC CHARACTERISTICS

V_{DD} = 5 V ±5%, T_A = 0°C to 70°C

Parameter	Symbol	Condition	Rating			Unit
			Minimum	Typical	Maximum	
Supply Voltage	V_{DD}		4.75	5.0	5.25	V
Power Consumption	P_D	f = 3.58 MHz, V_{DD} = 5 V	–	25	37	mW
Low Level Input Voltage	V_{IL}		0	–	0.8	V
High Level Input Voltage	V_{IH}		2.0	–	V_{DD}	V
Low Level Input Leak Current	I_{IL}	V_I = GND	–10	–	10	µA
High Level Input Leak Current	I_{IH}	$V_I = V_{DD}$	–10	–	10	µA
Low Level Output Voltage	V_{OL}	I_{OL} = 2 mA	0	–	0.4	V
High Level Output Voltage	V_{OH}	I_{OH} = –0.4 mA	2.4	–	V_{DD}	V
V_{REF} Output Voltage	V_{REF}		–	2.5	–	V

AC CHARACTERISTICS

V_{DD} = 5 V ±5%, T_A = 0°C to 70°C

Parameter	Symbol	Condition	Rating			Unit
			Minimum	Typical	Maximum	
Signal Input Level *1		T_A = 25°C, V_{DD} = 5 V	−29	−10	−1	dBm
TWIST *2			−	±10	−	dB
Allowable Frequency Deviation			±1.5 ±2 Hz	−	−	%
Prohibited Frequency Deviation			±3.5	−	−	%
Allowable Noise Level *3			−	−12	−	dB
Allowable Dial Tone Level *4			−	22	−	dB
Input Signal Detection Timing (Present) *5	t_{PDF}		5	11	14	ms
Input Signal Detection Timing (Absent) *5	t_{ADF}		0.5	4	8.5	ms
Input Signal Enable Period (Accept) *5	t_{SDA}		−	−	40	ms
Input Signal Enable Period (Reject) *5	t_{SDR}		20	−	−	ms
Inter-digit Pause (Accept) *5	t_{IPA}		−	−	40	ms
Inter-digit Pause (Reject) *5	t_{IPR}		9	−	−	ms
Input Clock Frequency	f_{IN}		3.5759	3.5795	3.5831	MHz
Clock Rise Time	tr		−	−	110	ns
Clock Fall Time	tf		−	−	110	ns
Clock Duty	DR		−	50	−	%

*1 dBm: 600 ohm reference

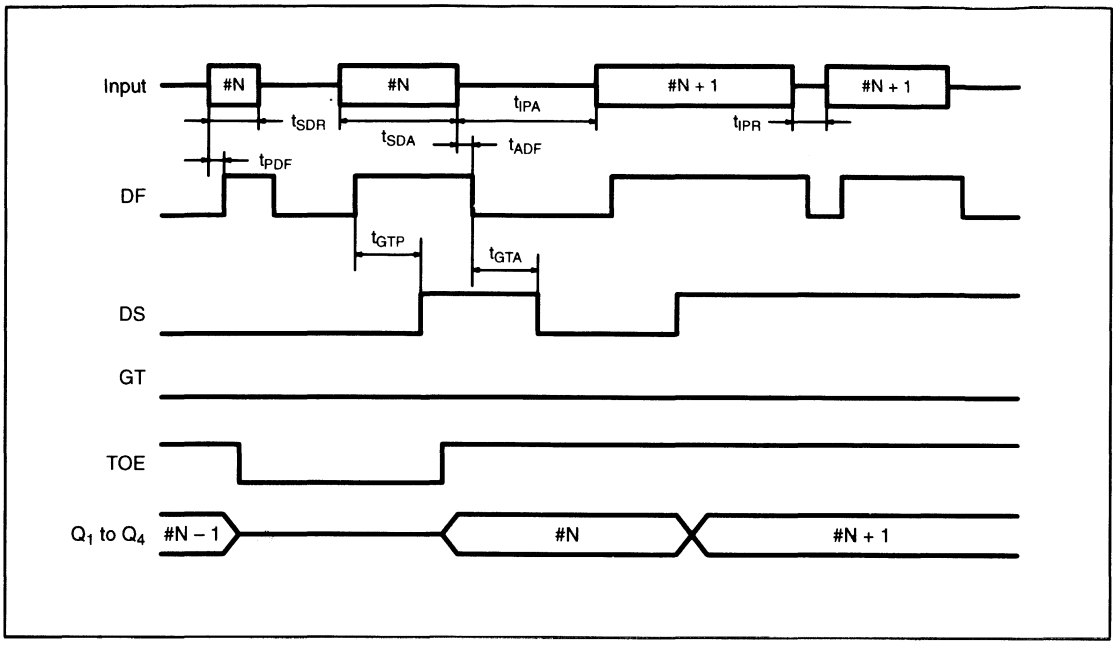
*2 TWIST = High group tone voltage/Low group tone voltage

*3 Allowable noise = Total allowable noise within the range 300 Hz to 3.4 kHz/Minimum amplitude tone level in valid tone pairs

*4 Allowable dial tone level = Total allowable normal dial tone volume/Minimum amplitude tone in valid tone pairs

*5 See Timing Chart.

TIMING CHART



FUJITSU SEMICONDUCTOR
DATA SHEET

DS04–23003–1E

ASSP

CMOS

5V Single Power Supply Audio Interface Unit (AIU)

MB86434

■ DESCRIPTION

The FUJITSU MB86434 is an AIU (audio interface unit) LSI for +5 V single-power source digital telephone devices, manufactured using CMOS process technology. The codec transmission filter characteristics meet G.712 standards, and can handle input and output in A-Law, μ-Law and linear conversion modes. The MB86434 also contains the necessary DTMF, microphone and receiver amps for telephone devices.

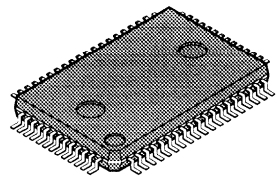
■ FEATURES

- +5 V single power supply
- Low power consumption : muting settings for each operating mode
  - Normal operation : 8.2 mA TYP (speaker amp mute)
  - Tone generation : 1.8 mA TYP (speaker amp mute)
  - Standby mode : 0.5 μA TYP
- On-chip codec filter meets G.712 standards
- Selection of codec conversion methods (A-law, μ-law, linear)
- On-chip low-noise microphone amp (2-channel) (unity gain frequency: 1MHz)
- On-chip receiver speaker amps (32 ΩBTL type: 10 mW MIN)
- On-chip tone speaker amp (32 ΩBTL type: 200 mW MIN)
- On-chip earphone speaker amps (32 Ω single type: 5 mW MIN)

(Continued)

■ PACKAGE

64 pin, Plastic QFP

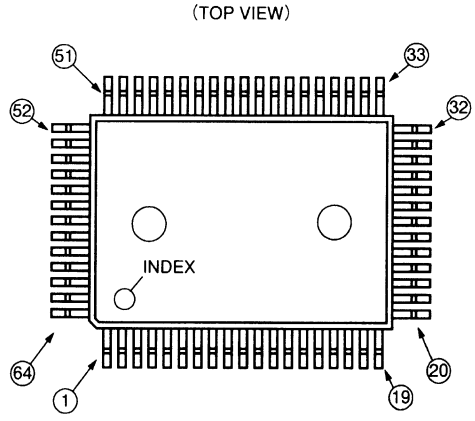


(FPT-64P-M07)

(Continued)

- On-chip electronic volume gain adjustments (sending, receiving, tone)
- On-chip accessory output circuits
- DTMF generator function
- Service tone generation
- CMOS compatible input/output

■ PIN ASSIGNMENT



(FPT-64P-M07)

■ PIN DESCRIPTION

Pin No.	Symbol	I/O	A/D	Description
1	CAG	G	A	Analog ground pin for codec block. To be set to 0 V.
2	VRH	O	A	Bypass capacitor connector pin for the A/D D/A reference voltage generator circuit. Place capacitor between VRH and CAG pins.
3	SGC	O	A	Bypass capacitor connector pin for the signal ground potential generator circuit. Place capacitor between SGC and CAG pins.
4	VDDAC	P	A	Analog power supply pin for codec block. To be set within range 4.75 to 5.25 V.
5	N.C.	—	—	Not connected. To be left open.
6	N.C.	—	—	Not connected. To be left open.
7	SYNC	I	D	PCM codec send/receive synchronization signal input pin. Operating clock frequencies 8 kHz. CMOS interface. Other frequencies may cause codec block to power-down.
8	CLK	I	D	Send/receive PCM signal series bit rate setting input pin. Data rate for μ-law, A-law modes may be set to any level in the range 64 k to 3.152 MHz, and for linear mode in the range 256 k to 3.152 MHz. Constant H or L level signal will cause part of codec block to power-down. CMOS interface.
9	DIN	I	D	PCM signal input pin. This signal is picked up internally at the fall of the CLK signal. CMOS interface.
10	DOUT	O	D	PCM signal output pin. Data is output in sync with the rise of the CLK signal. After data output, loses PLL synchronization, and at power-down this signal is fixed at H level. CMOS interface.
11	VDD	P	D	Digital power supply pin. To be set within range 4.75 to 5.25 V.
12	DG	G	D	Digital ground pin. To be set to 0V.
13	PSC0	I	D	Power-down control signal input pin. CMOS interface. Used with PSC1,2 pins for power-down settings.
14	PSC1	I	D	Power-down control signal input pin. CMOS interface. Used with PSC0,2 pins for power-down settings.
15	PSC2	I	D	Power-down control signal input pin. CMOS interface. Used with PSC0,1 pins for power-down settings.
16	SRD	I	D	9-bit serial data input pin. CMOS interface. Data is written at the rise of the signal from this pin.
17	SRC	I	D	Clock input pin for 9-bit serial data writing. CMOS interface. Data is written at the rise of this pin.
18	STB	I	D	Serial data latch strobe signal. Data is latched by the L level signal. CMOS interface. On-chip pull-down resistance.
19	XPRST	I	D	Digital reset signal input pin. CMOS interface. L level: internal latch initialization H level: normal operation

PSC 2 1 0
0 0 0 Full power-down
1 0 0 V_{REF} operating
— 1 0 Tone operating
— — 1 All operations available
(—: value not determined)

(Continued)

(Continued)

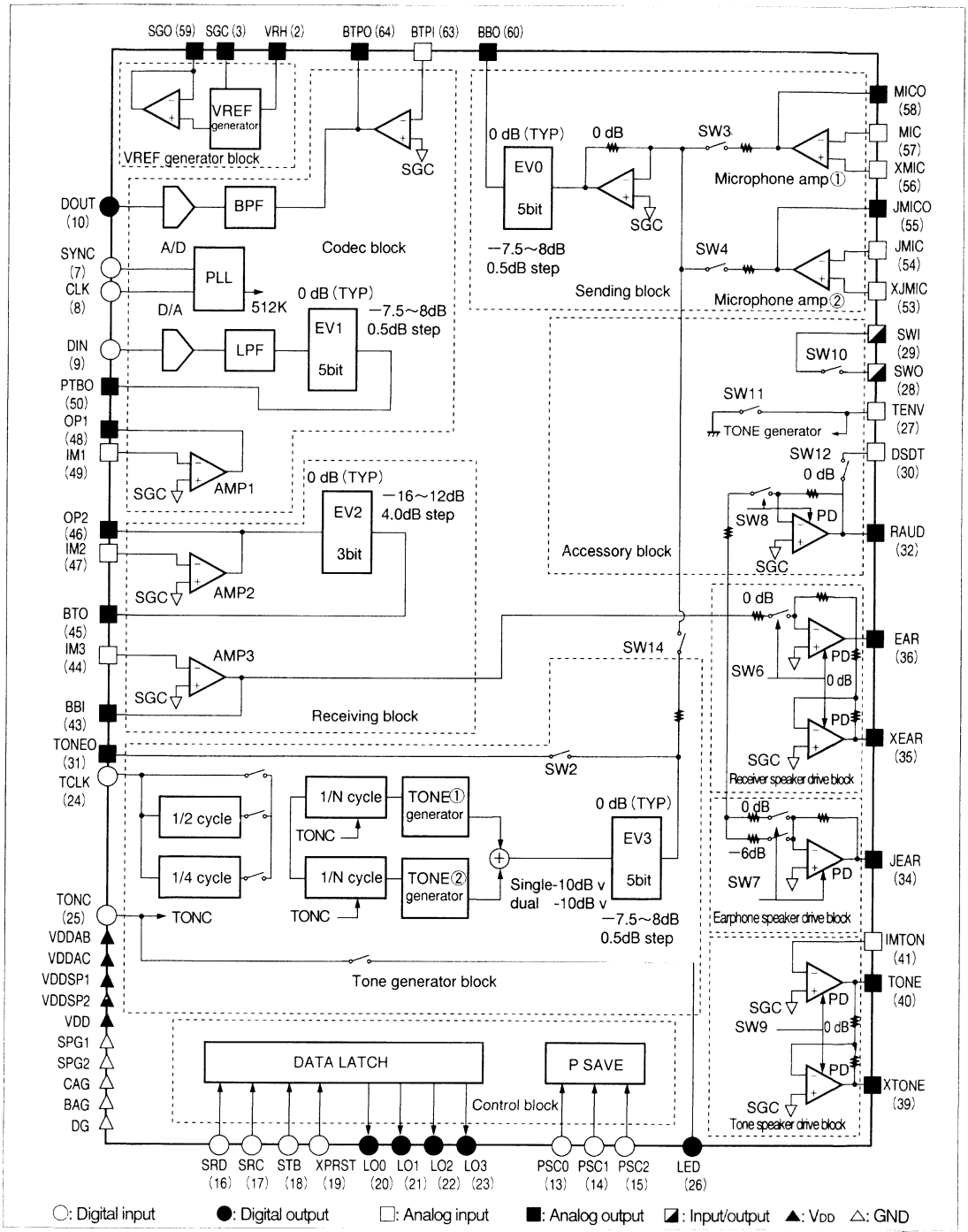
Pin No.	Symbol	I/O	A/D	Description
20	LO0	O	D	External control latch output pin. Outputs value D_0 of address 1000. CMOS interface.
21	LO1	O	D	External control latch output pin. Outputs value D_1 of address 1000. CMOS interface.
22	LO2	O	D	External control latch output pin. Outputs value D_2 of address 1000. CMOS interface.
23	LO3	O	D	External control latch output pin. Outputs value D_3 of address 1000. CMOS interface.
24	TCLK	I	D	Tone generator clock input pin. Can be used as a tone CLK signal by using address 1110 D4D3 to subdivide the internal clock signal by factors of 1/1, 1/2, 1/4. CMOS interface.
25	TONC	I	D	Tone generator cycle control input pin. CMOS interface. Hlevel signal outputs tone.
26	LED	O	D	Ring LED control output pin. CMOS interface.
27	TENV	I	A	Can be used to generate tone envelope, by placing capacitor between grounds and turning SW11 on/off.
28	SWO	I/O	A	Analog switch 10 input/output pin. Controls address 0111 D_0.
29	SWI	I/O	A	Analog switch 10 input/output pin.
30	DSDT	I	A	Accessory input. Can be connected to RAUD by switching paths.
31	TONEO	O	A	Tone signal output pin.
32	RAUD	O	A	Output pin for external speaker, or audio test signal. Can be connected to DSDT by switching paths.
33	VDDSP1	P	A	Speaker amp power supply pin. To be set within range 4.75 to 5.25 V.
34	JEAR	O	A	Earphone speaker amp output pin. Capable of 5 mW output at 32 Ω load.
35	XEAR	O	A	Receiver speaker amp output pin. Internally connected to EAR and BTL. Maximum output of 10 mW can be obtained at 32 Ω load by connecting speaker between EAR and XEAR.
36	EAR	O	A	Receiver speaker amp output pin. Connected to XEAR and BTL.
37	SPG1	G	A	Speaker amp ground pin. To be set to 0 V.
38	SPG2	G	A	Speaker amp ground pin. To be set to 0 V.
39	XTONE	O	A	Speaker amp tone output pin. Internally connected to TONE and BLT. Maximum output of 10 mW can be obtained at 32 Ω load by connecting speaker between TONE and XTONE.
40	TONE	O	A	Speaker amp tone output pin. When speaker amp is not used for tone, TONE should be shorted to IMTON.
41	IMTON	I	A	Speaker drive inverted (–) signal input pin. Can be used to adjust gain by connecting resistance to TONE and IMTON.
42	VDDSP 2	P	A	Speaker amp power supply pin. To be set within range 4.75 to 5.25 V.

(Continued)

(Continued)

Pin No.	Symbol	I/O	A/D	Description
43	BBI	O	A	AMP3 output pin. Should be included in HPF together with IM3, to prevent DC offset from entering speakers.
44	IM3	I	A	AMP3 inverted (–) signal input pin.
45	BTO	O	A	Receiving volume adjustment circuit output pin.
46	OP2	O	A	AMP2 output pin. If AMP2 is not used, IM2 should be shorted to OP2.
47	IM2	I	A	AMP2 inverted (–) signal input pin. Can form a circuit with OP2 to add sidetone or tone. Melody circuits, if used, can also be connected here.
48	OP1	O	A	AMP1 output pin. Can form a circuit with IM1 to include LPF or HPF in receiving block. If AMP1 is not used, IM1 should be shorted to OP1.
49	IM1	I	A	AMP1 inverted (–) signal input pin.
50	PTBO	O	A	PCM receiver output pin.
51	BAG	G	A	Analog ground pin for sending, receiving blocks. To be set to 0 V.
52	VDDAB	P	A	Analog power supply pin for sending, receiving blocks. To be set within range 4.75 to 5.25 V.
53	XJMIC	I	A	Microphone amp (2) non-inverted (+) signal input pin.
54	JMIC	I	A	Microphone amp (2) inverted (–) signal input pin.
55	JMICO	O	A	Microphone amp (2) output pin.
56	XMIC	I	A	Microphone amp (1) non-inverted (+) signal input pin.
57	MIC	I	A	Microphone amp (1) inverted (–) signal input pin.
58	MICO	O	A	Microphone amp (1) output pin.
59	SGO	O	A	Sending block signal ground potential output pin. Buffers SGC voltage.
60	BBO	O	A	Sending analog signal output pin.
61	N.C.	—	—	Not connected. To be left open.
62	N.C.	—	—	Not connected. To be left open.
63	BTPI	I	A	PCM ENCODE block input OP amp negative input pin.
64	BTPO	O	A	PCM ENCODE block input OP amp output pin.

■ BLOCK DIAGRAM



■ FUNCTIONAL DESCRIPTION

1. Register Settings

The MB86434 IC chip controls all electronic volume, switching, tone generator circuits and power-down control circuits by means of the SRD, STB and SRC data input signals.

The MB86434 uses a 9-bit serial data format consisting of a 4-bit address followed by 5 data bits. Data is picked up at the rise of the SRC signal, and latched by the STB L-level signal. The 9-bits of serial data preceding the STB signal are considered valid. These register settings are not reset at power-down. They can be reset when data is initialized by an XPRST L-level signal.

(1) Mode Settings

Control segment	Address	Data bit	Setting description	Initial data bit setting (at reset)	Remarks
	A_3 A_2 A_1 A_0	$D_4D_3D_2D_1D_0$		$D_4D_3D_2D_1D_0$	
EV0	0 0 0 1	$D_4D_3D_2D_1D_0$	Sending audio level adjustment. Adjusts EV0 gain.	0 1 1 1 1	*1
EV1	0 0 1 0	$D_4D_3D_2D_1D_0$	Sending audio level adjustment. Adjusts EV1 gain.	0 1 1 1 1	
EV2	0 0 1 1	** $D_2D_1D_0$	Sending audio level adjustment. Adjusts EV2 gain.	** 1 0 0	
TX-MUTE	0 1 0 0	D_4*** D_0	D_0: Sending audio mute SW 3, 4 on/off control. Mute: 1, Unmute: 0	0 * * * 0	*2, *3
RX-MUTE			D_4: Receiving audio mute SW 6, 7, 8, 9 on/off control. Mute: 1, Unmute: 0		*3, *4
SW4	0 1 0 1	D_4* $D_2D_1D_0$	D_1: JMIC mute SW 4 on/off control. Mute: 1, Unmute: 0	0 * 0 0 0	*2
SW3			D_2: MIC mute SW 3 on/off control. Mute: 1, Unmute: 0		
SW8			D_4: RAUD mute SW 8 on/off control. Mute: 1, Unmute: 0		*3, *4, *5
SW6	0 1 1 0	D_4* $D_2D_1D_0$	D_0: EAR, XEAR mute SW 6 on/off control. Mute: 1, Unmute: 0	0 * 0 0 0	*4
SW9			D_1: TONE, XTONE mute SW 9 on/off control. Mute: 1, Unmute: 0		
SW7			D_2: JEAR mute SW 7 on/off control. Mute: 1, Unmute: 0		
ATT			D_4: JEAR attenuation level switch. 0: 0.0 dB, 1: -6.0 dB.		
SW10	0 1 1 1	$D_4D_3D_2D_1D_0$	D_0: SWI-SWO switch SW 10 on/off control. On: 1, Off: 0	0 0 0 0 0	*3, *6
SW12			D_1: DSDT pin selection SW 12 on/off control. On: 1, Off: 0		*3, *5
SW11			D_2: Envelope generator generate envelope (SW11 Off): 1 no envelope (SW11 On): 0		*3, *7
SW2			D_3: TONEO mute SW 2 on/off control. Mute: 1, Unmute: 0		*8
SW14			D_4: TONE sending add SW 14 on/off control. On: 1, Off: 0		

(Continued)

(Continued)

Control segment		Address				Data bit					Setting description	Initial data bit setting (at reset)					Remarks
		A_3	A_2	A_1	A_0	D_4	D_3	D_2	D_1	D_0		D_4	D_3	D_2	D_1	D_0	
Serial / parallel converter		1	0	0	0	*	D_3	D_2	D_1	D_0	Parallel output D_3=LO3, D_2=LO2, D_1=LO1, D_0=LO0	*	0	0	0	0	*9
EV3		1	0	0	1	D_4	D_3	D_2	D_1	D_0	Tone level adjustment. Adjusts EV3 gain.	0	1	1	1	1	*1
TONE control	Frequency control	1	0	1	0	X_8	X_7	X_6	X_5	X_4	Tone (1) frequency control, set by 8-bit value X_7 to X_0. X_8 = 1 to output trapezoidal wave, X_8 = 0 to output sine wave.	0	0	0	0	0	*10, *11
		1	0	1	1	*	X_3	X_2	X_1	X_0		*	0	0	1	0	
		1	1	0	0	Y_8	Y_7	Y_6	Y_5	Y_4	Tone (2) frequency control, set by 8-bit value Y_7 to Y_0. Y_8 = 1 to output trapezoidal wave, Y8 = 0 to output sine wave.	0	0	0	0	0	
		1	1	0	1	*	Y_3	Y_2	Y_1	Y_0		*	0	0	1	0	
	Output control	1	1	1	0	D_4	D_3	D_2	D_1	D_0	Tone generator control D_0: tone (2) on/off control. On: 1, off: 0 D_1: tone (1) on/off control. On: 1, off: 0 D_2: LED output on/off control. On: 1, off: 0	0	0	1	1	1	*7, *8, *12
	Master clock control										Tone CLK D_4, D_3 0 0 : TCLK1/1 frequency selected 0 1 : TCLK1/2 frequency selected 1 0 : TCLK1/4 frequency selected 1 1 : Prohibited						*10
PCM		1	1	1	1	*	*	*	D_1	D_0	PCM control D_1, D_0 0 0 : μ-law mode selected 1 0 : A-law mode selected 0 1 : linear mode selected	*	*	*	0	0	*13, *14
TEST		0	0	0	0	D_4	D_3	D_2	D_1	D_0	Do not write in test mode.	0	0	0	0	0	

*1: See (4) Electronic Volume Controls
*2: See (2) Sending Audio Mute Setting
*3: See 5. Power Saving Modes
*4: See (3) Receiving Audio Mute Settings
*5: See 3. Analog Output (2) Accessory Output
*6: See 2. Analog Input (2) Accessory Input
*7: See (5) Tone Generator Circuit • Tone Output Controls
*8: See (5) Tone Generator Circuit • Tone Generator Control Output Level
*9: See (7) Parallel Output
*10: See (5) Tone Generator Circuit • Tone Frequency Control Registers
*11: See (5) Tone Generator Circuit • Tone Output Waveforms
*12: See (5) Tone Generator Circuit • LED Output Controls
*13: See (6) Codec Input/Output
*14: See (7) The Codec SYNC Pin

(2) Sending Audio Mute Settings

Switches SW 3 to SW 4 have the following functions. Address 0100 signals have priority.

Address	Setting		Switching setting		Remarks
	$A_3A_2A_1A_0$	$A_3A_2A_1A_0$			
	0 1 0 0	0 1 0 1			
Data bit	$D_4D_3D_2D_1D_0$	$D_4D_3D_2D_1D_0$	SW3	SW4	
	— * * * 1	— * — — *	○	○	
	— * * * 0	— * — 1 *	—	○	
	— * * * 0	— * 1 — *	○	—	
	— * * * 0	— * — 0 *	—	×	
	— * * * 0	— * 0 — *	×	—	

○: muted, ×: unmuted, —: not determined

(3) Receiving Audio Mute Settings

Switches SW 6 to SW 9 have the following functions. Address 0100 signals have priority.

Address	Setting			Switching setting				Remarks
	$A_3A_2A_1A_0$	$A_3A_2A_1A_0$	$A_3A_2A_1A_0$					
	0 1 0 0	0 1 0 1	0 1 1 0					
Data bit	$D_4D_3D_2D_1D_0$	$D_4D_3D_2D_1D_0$	$D_4D_3D_2D_1D_0$	SW8	SW7	SW9	SW6	
	1 * * * —	— * — — *	— * — — —	○	○	○	○	
	0 * * * —	— * — — *	— * — — 1	—	—	—	○	
	0 * * * —	— * — — *	— * — 1 —	—	—	○	—	
	0 * * * —	— * — — *	— * 1 — —	—	○	—	—	
	0 * * * —	1 * — — *	— * — — —	○	—	—	—	
	0 * * * —	— * — — *	— * — — 0	—	—	—	×	
	0 * * * —	— * — — *	— * — 0 —	—	—	×	—	
	0 * * * —	— * — — *	— * 0 — —	—	×	—	—	
	0 * * * —	0 * — — *	— * — — —	×	—	—	—	

○: muted, ×: unmuted, —: not determined

(4) Electronic Volume Controls

There are four different electronic volume controls, EV0 through EV3, with the following specifications. Electronic volume control settings are made by the SRD, SRC and STB signals, and setting values are reset by the XPRST signal. However, settings are not reset by PSC0, PSC1, PSC2 power-down mode operations.

Table 1 Relation of Volume Control Data bit Values to Gain

Step	Data bit value	EV0 sending gain adjustment	EV1 receiving gain adjustment	EV2 receiver volume adjustment	EV3 tone gain adjustment	Unit
	D_4 D_3 D_2 D_1 D_0	Typ.	Typ.	Typ.	Typ.	
0	0 0 0 0 0	−7.5	−7.5	−16	−7.5	
1	0 0 0 0 1	−7.0	−7.0	−12	−7.0	
2	0 0 0 1 0	−6.5	−6.5	−8	−6.5	
3	0 0 0 1 1	−6.0	−6.0	−4	−6.0	
4	0 0 1 0 0	−5.5	−5.5	0	−5.5	
5	0 0 1 0 1	−5.0	−5.0	4	−5.0	
6	0 0 1 1 0	−4.5	−4.5	8	−4.5	
7	0 0 1 1 1	−4.0	−4.0	12	−4.0	
8	0 1 0 0 0	−3.5	−3.5		−3.5	
9	0 1 0 0 1	−3.0	−3.0		−3.0	
10	0 1 0 1 0	−2.5	−2.5		−2.5	
11	0 1 0 1 1	−2.0	−2.0		−2.0	
12	0 1 1 0 0	−1.5	−1.5		−1.5	
13	0 1 1 0 1	−1.0	−1.0		−1.0	
14	0 1 1 1 0	−0.5	−0.5		−0.5	
15	0 1 1 1 1	0.0	0.0		0.0	
16	1 0 0 0 0	0.5	0.5		0.5	dB
17	1 0 0 0 1	1.0	1.0		1.0	
18	1 0 0 1 0	1.5	1.5		1.5	
19	1 0 0 1 1	2.0	2.0		2.0	
20	1 0 1 0 0	2.5	2.5		2.5	
21	1 0 1 0 1	3.0	3.0		3.0	
22	1 0 1 1 0	3.5	3.5		3.5	
23	1 0 1 1 1	4.0	4.0		4.0	
24	1 1 0 0 0	4.5	4.5		4.5	
25	1 1 0 0 1	5.0	5.0		5.0	
26	1 1 0 1 0	5.5	5.5		5.5	
27	1 1 0 1 1	6.0	6.0		6.0	
28	1 1 1 0 0	6.5	6.5		6.5	
29	1 1 1 0 1	7.0	7.0		7.0	
30	1 1 1 1 0	7.5	7.5		7.5	
31	1 1 1 1 1	8.0	8.0		8.0	

Note: Each setting value is determined in relation to the initial setting value.
Returns to initial value at reset (—— parts)
EV2 data bits D_4, D_3 are *.

Table 2 Volume Gain Deviation

Volume control No.	Condition	Min.	Typ.	Max.	Unit
EV0 EV1 EV3	Gain deviation, with respect to reference value shown in Table1	Reference value − 0.5 dB	Reference value	Reference value + 0.5 dB	dB
EV2	Input frequency = 1020 Hz Input level = − 20 dBv	Reference value − 1.0 dB	Reference value	Reference value + 1.0 dB	

(5) Tone Generator Circuit

- **Tone Frequency Control Registers**
  The tone generator uses a clock signal obtained by subdividing the TCLK clock signal input by 1/1, 1/2 or 1/4 according to the data bit in address 1110.

Table 3 Tone Clock Frequency Register Control

Address 1110		Tone generator clock signal (f_{IN})
D_4	D_3	
0	0	TCLK input clock signal
0	1	TCLK input clock signal subdivided by 1/2
1	0	TCLK input clock signal subdivided by 1/4
1	1	Prohibited

Frequency settings available through the tone frequency control register are determined by the following formula.
Frequency setting $f = f_{IN}/(12 * (1+n))$, n=1, 2, 3, ..., 255. (where f_{IN}: tone generator clock signal frequency).
Therefore the available frequency setting range when f_{IN} = 512 kHz is between f_{min} = 167 Hz and f_{max} = 21333 Hz.

Frequency settings corresponding to each DTMF rated reference frequency are shown in the following table.

Table 4 Tone Frequency Register Control

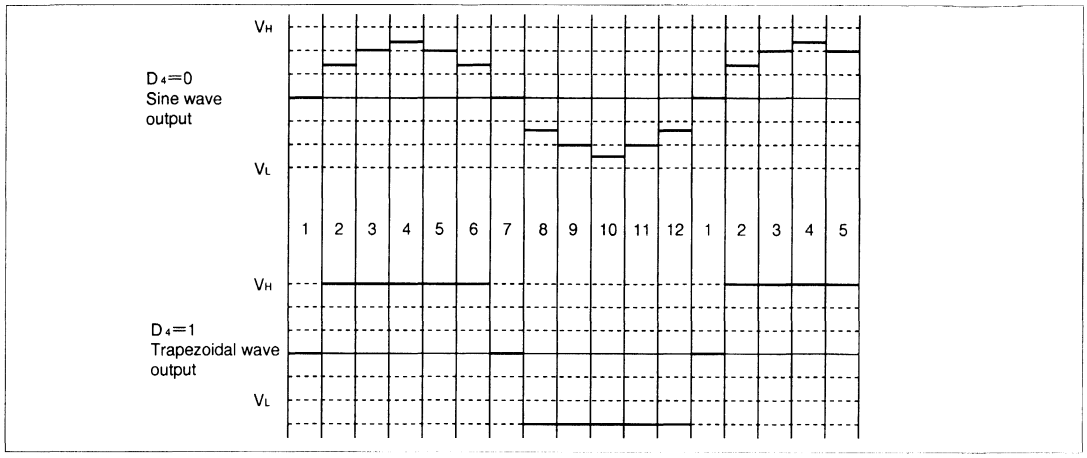
(Condition: 512 kHz)

Tone type		Rated reference frequency (generator frequency)	Frequency setting	Address 1010/1100 Data bit D_4 D_3 D_2 D_1 D_0	Address 1011/1101 Data bit D_4 D_3 D_2 D_1 D_0	n	Error
Service tone (single tone)		262 Hz	261.7 Hz	— 1 0 1 0	* 0 0 1 0	162	−0.11%
		384 Hz	384.4 Hz	— 0 1 1 0	* 1 1 1 0	110	0.10%
		400 Hz	398.7 Hz	— 0 1 1 0	* 1 0 1 0	106	−0.32%
		2000 Hz	2031.7 Hz	— 0 0 0 1	* 0 1 0 0	20	1.56%
		2600 Hz	2666.7 Hz	— 0 0 0 0	* 1 1 1 1	15	2.50%
DTMF	Low tone	697 Hz	699.4 Hz	— 0 0 1 1	* 1 1 0 0	60	0.34%
		770 Hz	775.7 Hz	— 0 0 1 1	* 0 1 1 0	54	0.74%
		852 Hz	853.3 Hz	— 0 0 1 1	* 0 0 0 1	49	0.15%
		941 Hz	948.1 Hz	— 0 0 1 0	* 1 1 0 0	44	0.75%
	High tone	1209 Hz	1219.0 Hz	— 0 0 1 0	* 0 0 1 0	34	0.82%
		1336 Hz	1333.3 Hz	— 0 0 0 1	* 1 1 1 1	31	−0.20%
		1477 Hz	1471.3 Hz	— 0 0 0 1	* 1 1 0 0	28	−0.38%
		1633 Hz	1641.0 Hz	— 0 0 0 1	* 1 0 0 1	25	0.48%

Note: • Setting values are BIN display values
• Error represents frequency setting error with respect to rated reference frequency.

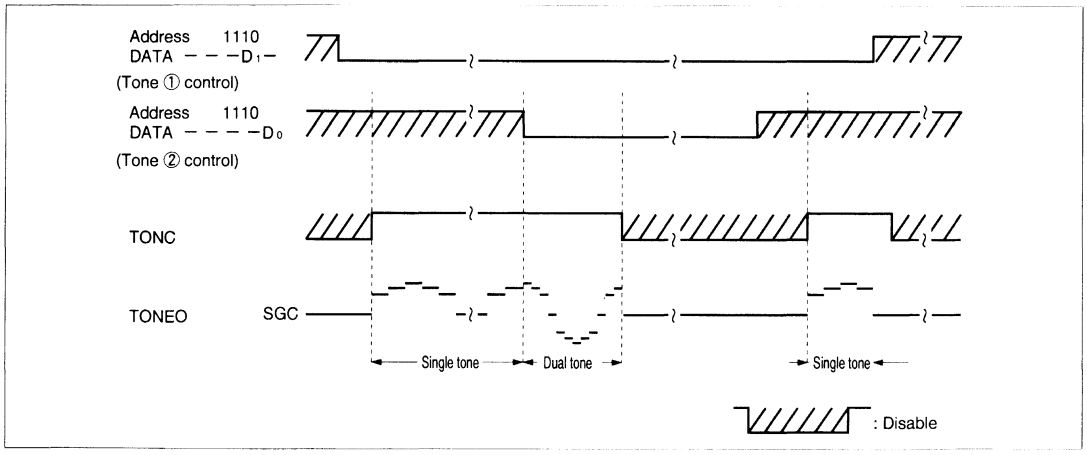
• **Tone Output Waveform**

The D_4 data bit at address 1010, 1100 may be used to select either sine-wave or trapezoidal waveforms for tone output.

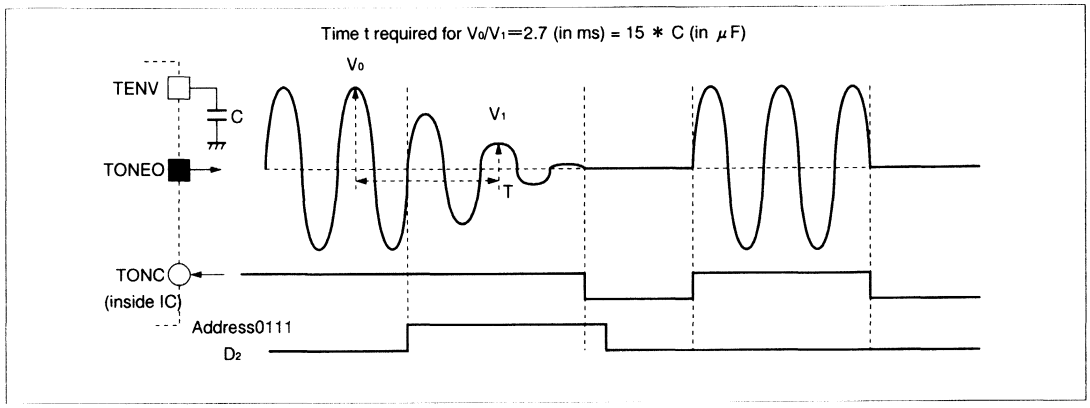


• **Tone Output Control**

Tone output may be controlled by address and through the external tone control input pin TONC. In addition, the tone control offers a choice of sine or trapezoidal waveforms.

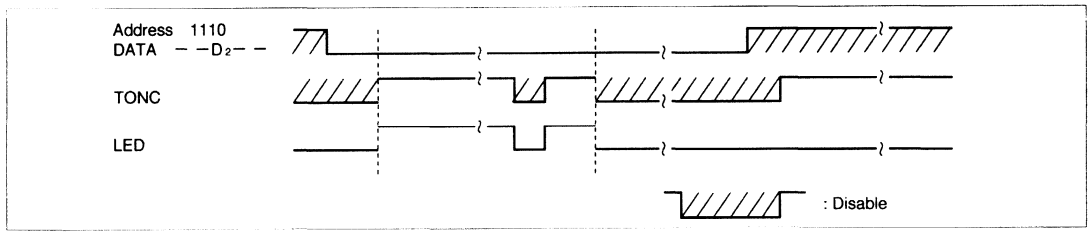


Also, by connecting a capacitor between the TENV pin and the ground, it is possible to generate an envelope for the tone waveform. Set address 0111 data bit D_2 to 1 to generate. If an envelope is generated, silencing must be applied by an L-level signal from the TONC pin. The type of envelope that can be generated can be calculated approximately from the following formula.



• LED Output Controls

Output from the LED output pins can be controlled by the TONC signal and the address 1110 data bit D_2. When the TONC signal is H-level, and the address 1110 data bit D_2 value is L-level, the output level will be high. Output levels are CMOS levels.



• **Tone Generator Control Output Level**

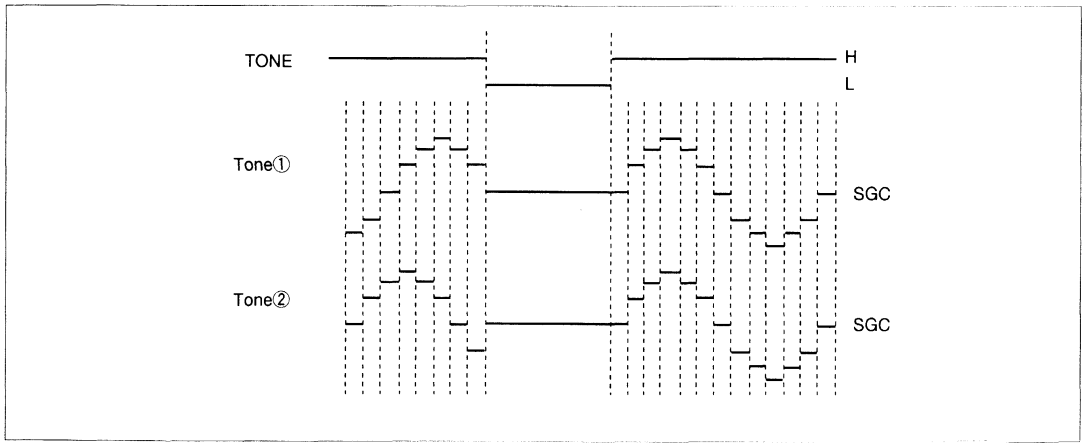
(Condition: EV3 = 0 dB)

External pins				Address 1110 data bits			Address 0111 data bits	Tone generator circuit operating mode		Output pin mode		Remarks
PSC2	PSC1	PSC0	TONC	D_2	D_1	D_0	D_3 (SW2)	Tone ①	Tone ②	LED	TONEO	
0	0	0	—	—	—	—	—	×	×	L	H-Z	
1	0	0	—	—	—	—	—	×	×	L	H-Z	
—	1 or 1		0	—	—	—	0	SGC	SGC	L	SGC	
—	1 or 1		0	—	—	—	1	SGC	SGC	L	H-Z	
—	1 or 1		1	1	—	—	—	—	—	L	—	
—	1 or 1		1	0	—	—	—	—	—	○	—	
—	1 or 1		1	—	1	1	0	SGC	SGC	—	SGC	
—	1 or 1		1	—	1	0	0	SGC	○	—	−10 dBv	Single tone output
—	1 or 1		1	—	0	1	0	○	SGC	—	−10 dBv	Single tone output
—	1 or 1		1	—	0	0	0	○	○	—	−10 dBv	Dual tone output

○ : Operational, × : Power down, H-Z : High-impedance, L : L-level fixed, SGC : SGC fixed

Note: When the TONC pin signal is L-level, the tone generator circuit counters will be reset. When a dual tone is generated at the time of reset, the initial phase settings for tone ① and tone ② will be in phase.

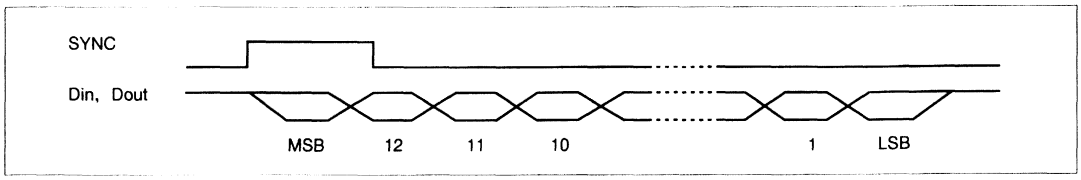
• **Example: When Tone ①, Tone ② are at the same frequency:**



(6) Codec

• Input/output

Both the μ-law and A-law coding/decoding conversion processes used by the MB86434 codec are compatible with CCITT Recommendation G.711. In addition, linear coding in the form of 14-bit two's complement code can be output starting with MSB values.



MSB	Code	LSB	PTBO reference voltage (V)
0	1 1 1 1 1 1 1 1 1 1 1 1 1		1.1766
	⟆		⟆
0	0 0 0 0 0 0 0 0 0 0 0 0 0	1	2.3986
0	0 0 0 0 0 0 0 0 0 0 0 0 0	0	2.4000
1	1 1 1 1 1 1 1 1 1 1 1 1 1	1	2.4014
	⟆		⟆
1	0 0 0 0 0 0 0 0 0 0 0 0 0	1	3.6235

• The codec SYNC pin

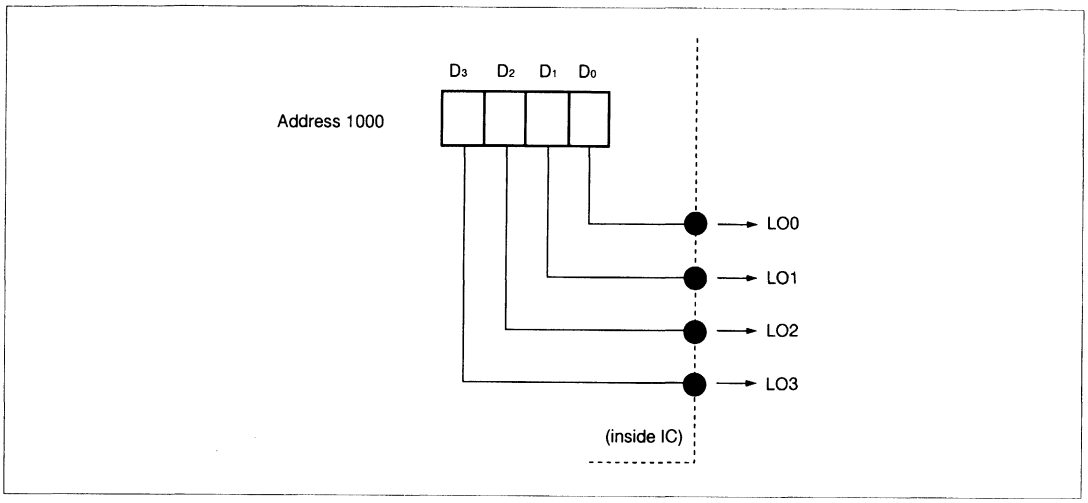
The codec block requires the input of an 8 kHz sampling clock signal at the SYNC pin, as well as a data transfer clock at the CLK pin. In order to conserve power consumption, whenever the SYNC pin or CLK pin signal is inactive, the system goes into SYNC power-down mode and stops code conversion.

Also, if either the SYNC or CLK pins encounters jitter of 5 μs or greater, the system may go into power-down mode.Table shows the status of output pins in SYNC power-down mode.

Pin symbol	Operation
SGC	Normal operation (2.4 V)
SGO	Normal operation (2.4 V)
VRH	Normal operation (4.0 V)
DOUT	H-level fixed
PTBO	SGC
BTPO	High impedance

(7) Parallel Output

The LO0 to 3 pins carry latched output for external controls. The data written to address 1000 can be output through these pins. Output is CMOS output.

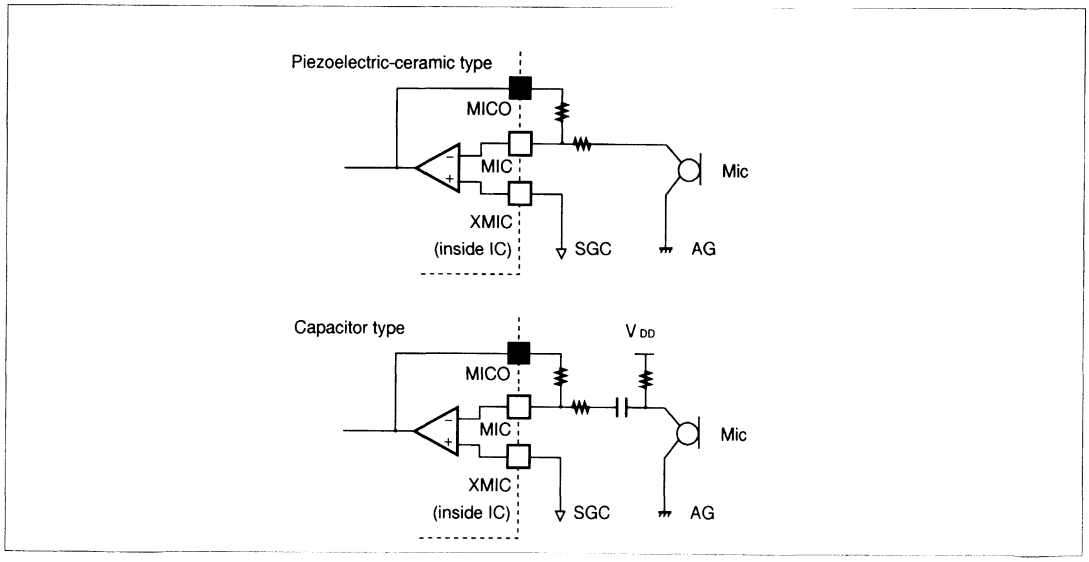


2. Analog Input

Analog input signals in the MB86434 include the two microphone inputs and the general-purpose analog switch.

(1) Microphone Amps

The microphone amps take the incoming signal from the microphones and amplify it to any desired level of gain. The microphone lines are low-noise types for use with piezoelectric-ceramic or capacitor microphones, and are capable of a wide range of amplification. All microphones and amps must be coupled with capacitors to prevent amplification of offset signals.

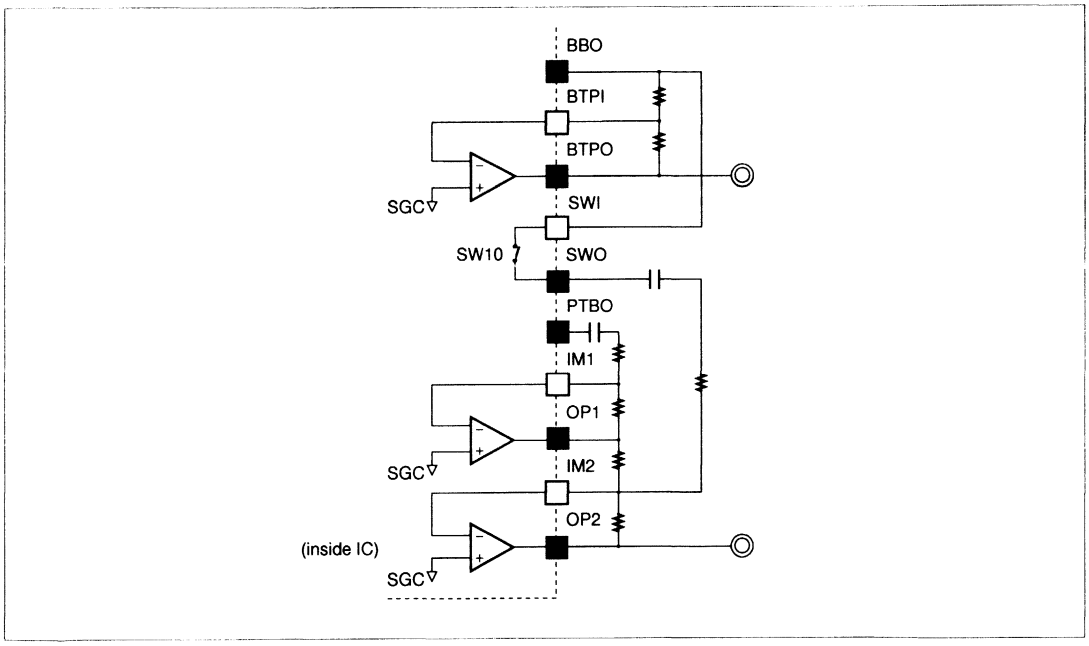


Parameter	Characteristics (typ)
Unity gain frequency	1 MHz
Input conversion noise (BW = 300 - 3400 Hz)	3.1mV
Maximum output level	1.25 - 3.75 V_{OP}
Minimum load level	50 kΩ

(2) Analog Switches

The analog switches include on-chip general-purpose switches with 1 kΩ in-resistance. Switches are controlled by writing to register address 0111 data bit D_0, using H-level to make connections.

• Sidetone addition using analog switches



• SW10 = on

Address A_3 A_2 A_1 A_0	Data bit D_4 D_3 D_2 D_1 D_0
0 1 1 1	— — — — 1

3. Analog Output

The MB86434 has a total of four analog output circuits, including the three speaker drive circuits (receiver, earphone and tone) and the accessory output.

(1) Speaker Drive Amp

The speaker drive amps include two circuits (receiver and tone) with BTL output and one system (earphone) with single output. Because the speaker amp requires relatively high levels of power, it is connected to speaker selection switches (sw6-sw9) for power-down mode selection.

Two systems (receiver and earphone) have fixed gain levels, while the other system (tone) allows gain adjustment by means of external resistors.

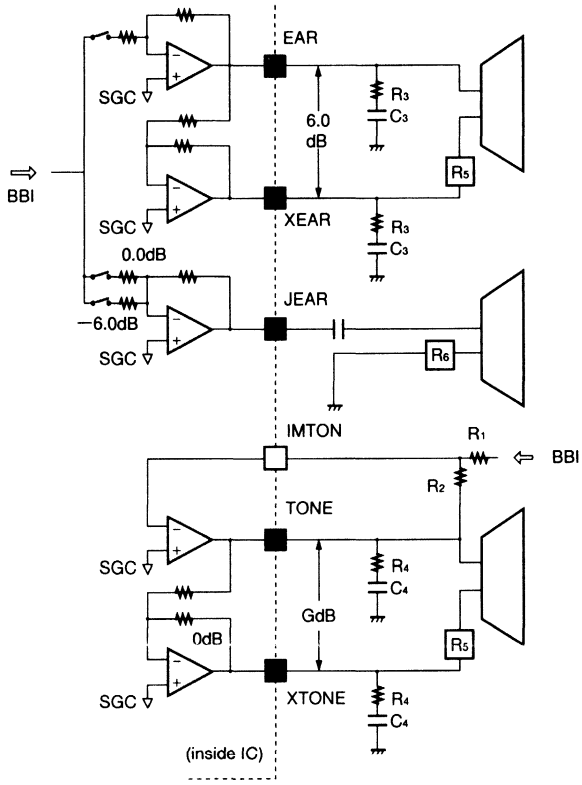
In addition, the tone speaker amp is able to use the 200 mW large-current power circuit

Table Speaker Drive Amp Output Standards

Parameter	Receiver speaker amps (EAR, XEAR)	Earphone speaker amp (JEAR)	Tone speaker amps (TONE, XTONE)
Output type	BTL	Single	BTL
Load resistance *1	32 Ω (typ)	32 Ω (typ)	32 Ω (typ)
Load resistance *2	2.8 kΩ (typ)	2.8 kΩ (typ)	2.8 kΩ (typ)
Load capacity *2	70 nF	70 nF	70 nF
Final stage gain	6.0 dB (between EAR-XEAR)	0.0 dB/−6.0 dB (JEAR)	−5 to 20 dB (between TONE-XTONE)
Maximum output power	10 mW (min)	5 mW (min)	200 mW (min)

*1: Dynamic-type speaker
*2: Piezoelectric-ceramic type speaker

• Analog Output Connection Example



Receiver speaker
Dynamic type: 32 Ω (typ)
Piezoelectric-ceramic type: 70 nF, 2.8 kΩ (typ)

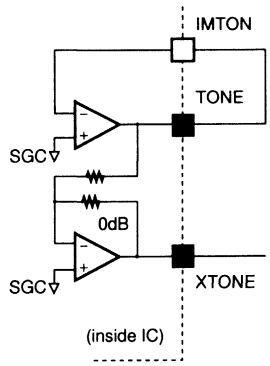
Earphone speaker
Dynamic type: 32 Ω (typ)
Piezoelectric-ceramic type: 70 nF, 2.8 kΩ (typ)

Tone speaker
Dynamic type: 32 Ω (typ)
Piezoelectric-ceramic type: 70 nF, 2.8 kΩ (typ)

G=20 LOG (2 * R_2/R_1) [dB]

Note: • R_3, C_3, R_4, C_4 should be given the respective values 80Ω, 0.01 μF in order to prevent unwanted oscillation.
• If a piezoelectric-ceramic type microphone is used, R_5, R_6 should be given the respective values 20Ω, 10Ω in order to prevent unwanted oscillation.

• Tone Speaker Amp Not Used



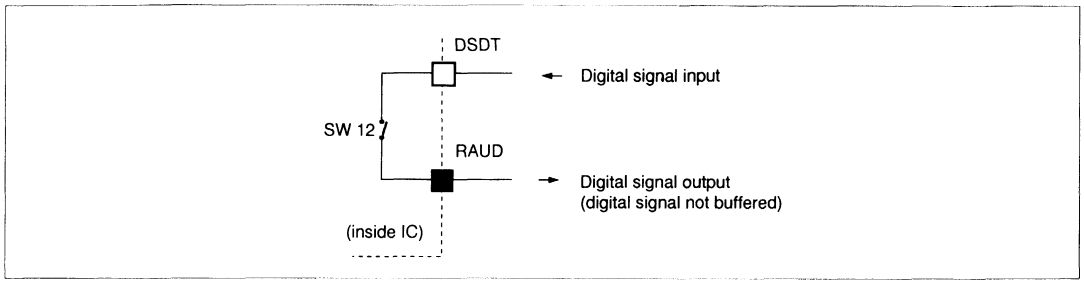
Note: When no tone speaker amp is used, the amp input IMTON and output TONE should be shorted together.

(2) Accessory Output

The accessory output (RAUD pin) can carry either digital or analog output signals, and is controlled by address 0101 data bit D_4 (SW 8), and address 0111 data bit D_1 (SW 12).

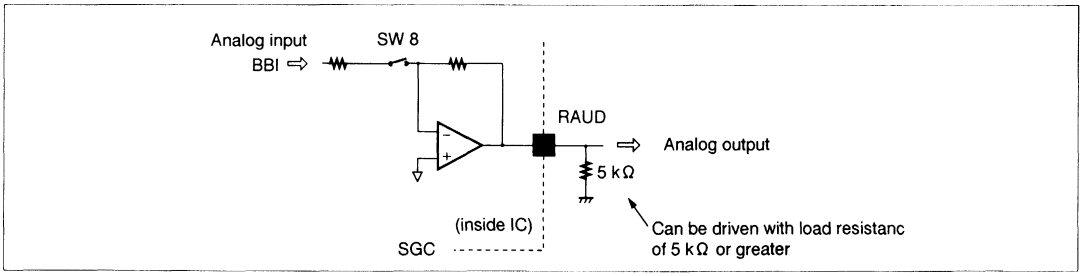
When both SW 8 and SW 12 are in off position, the accessory outputline is in H-Z (high impedance) state. Caution: never place both SW 8 and SW 12 in on position at the same time. This may cause the MB86434 to function improperly.

• SW12 in On Position



Address				Data bit				
A_3	A_2	A_2	A_1	D_4	D_3	D_2	D_1	D_0
0	1	1	1	—	—	—	1	—

• SW8 in On Position

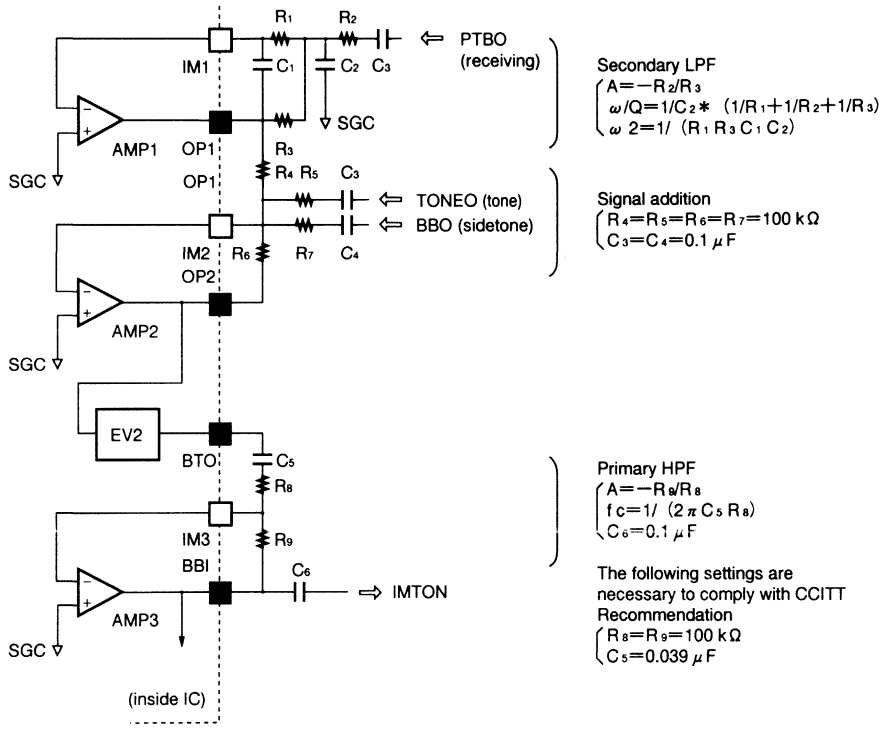


Address				Data bit				
A_3	A_2	A_2	A_1	D_4	D_3	D_2	D_1	D_0
0	1	0	0	0	*	*	*	—
0	1	0	1	0	*	—	—	—

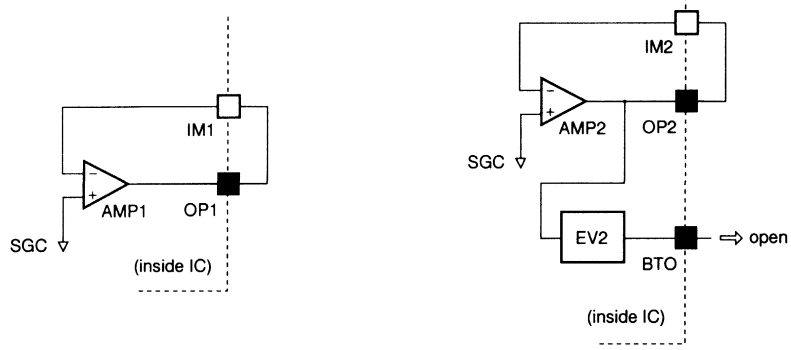
4. Receiver Connections

It is possible to add tones and adjust sidetones by using amp 1,2 and 3 and the electronic volume control. When using amp 3, however, it is necessary to include HPF to avoid interference from the speaker amp DC.

• Tone and Sidetone Addition by Inclusion of Secondary LPF and Primary HPF.

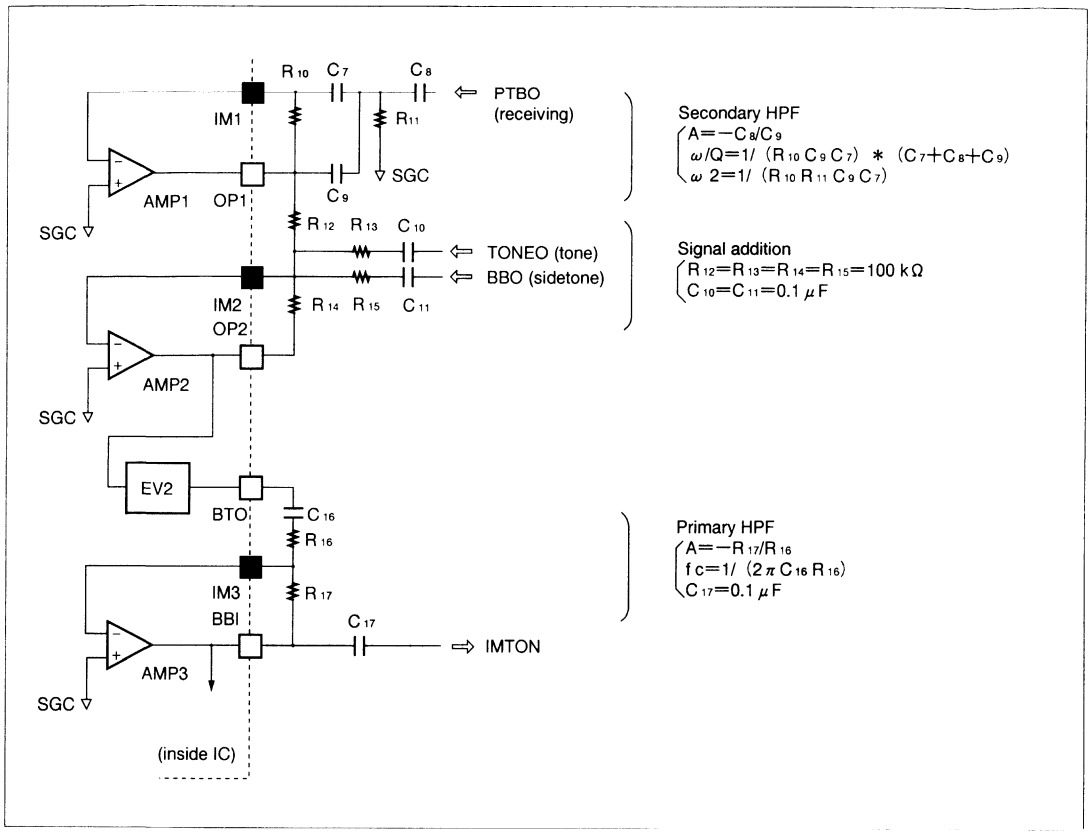


• Amp1, Amp2 not used



Note: When amps are not used, the amp input and output should be shorted together.

• **Tone and Sidetone Addition by Inclusion of Third-Order HPF**



5. Power Saving Modes

(1) Mode Selection

The MB86434 power saving modes can be controlled by using the external control signal lines (3 lines). It is also possible to apply power saving modes to the speaker amps with high power consumption levels by writing changes to register settings. Whenever the MB86434 changes directly from a power-down mode to normal operating mode, there is a possibility that speaker tones may be produced. The recommended sequence of coding changes to go into normal mode is (VREF mode) → (Tone mode) → (Normal mode).

Power Saving Modes

Mode	External pins			Address 0100		Address 0101	Address 0110			Output pin status												Operating circuit status									Power supply current (mA) (typ)
	PSC2	PSC1	PSC0	D4	D0	D	D	D	D	EAR XEAR	JEAR	TONE XTONE	RAUD	DOUT	SGC SGO	OP2 BTO	PTBO BTPO	OP1	MICO JMICO BBO VRH	BBI	CODEC	VREF generator	TONE generator	Sending	Receiving	Receiver	Earphone	Tone	Accessory		
						SW8	SW7	SW3	SW6	SW6	SW7	SW9	SW8													SW6	SW7	SW9	SW8		
All power-down	0	0	0	—	—	—	—	—	—	ZA	H-Z	ZB	H-Z	H	H-Z	ZC	H-Z	H-Z	H-Z	*	×	×	×	×	×	×	×	×	×	0.0005
VREF	1	0	0	—	—	—	—	—	—	ZA	H-Z	ZB	H-Z	H	○	ZC	H-Z	H-Z	H-Z	*	×	○	×	×	×	×	×	×	×	0.48
Tone	—	1	0	1	1	—	—	—	—	ZA	H-Z	ZB	H-Z	H	○	○	H-Z	H-Z	H-Z	○	×	○	○	×	○	×	×	×	×	1.8
	—	1	0	0	1	0	1	1	1	ZA	H-Z	ZB	○	H	○	○	H-Z	H-Z	H-Z	○	×	○	○	×	○	×	×	×	○	2.4
	—	1	0	0	1	1	0	1	1	ZA	○	ZB	H-Z	H	○	○	H-Z	H-Z	H-Z	○	×	○	○	×	○	×	○	×	×	4.5
	—	1	0	0	1	1	1	0	1	ZA	H-Z	○	H-Z	H	○	○	H-Z	H-Z	H-Z	○	×	○	○	×	○	×	×	○	×	6.8
	—	1	0	0	1	1	1	1	0	○	H-Z	ZB	H-Z	H	○	○	H-Z	H-Z	H-Z	○	×	○	○	×	○	○	×	×	×	6.8
Normal	—	—	1	0	0	0	1	1	1	ZA	H-Z	ZB	○	○	○	○	○	○	○	○	○	○	○	○	○	×	×	×	○	8.2
	—	—	1	0	0	1	0	1	1	ZA	○	ZB	H-Z	○	○	○	○	○	○	○	○	○	○	○	○	×	○	×	×	10.3
	—	—	1	0	0	1	1	0	1	ZA	H-Z	○	H-Z	○	○	○	○	○	○	○	○	○	○	○	○	×	×	○	×	12.6
	—	—	1	0	0	1	1	1	0	○	H-Z	ZB	H-Z	○	○	○	○	○	○	○	○	○	○	○	○	○	×	×	×	12.6
	—	—	1	0	0	0	0	0	0	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	20.9

Note: • ○: Operational, ×: Power-down, H-Z: High impedance, H: H-level fixed

*: High impedance may not be applied, depending on status of SW6, SW7, SW8.

ZA: EAR and XEAR are floating, however high resistance connection between EAR and XEAR.

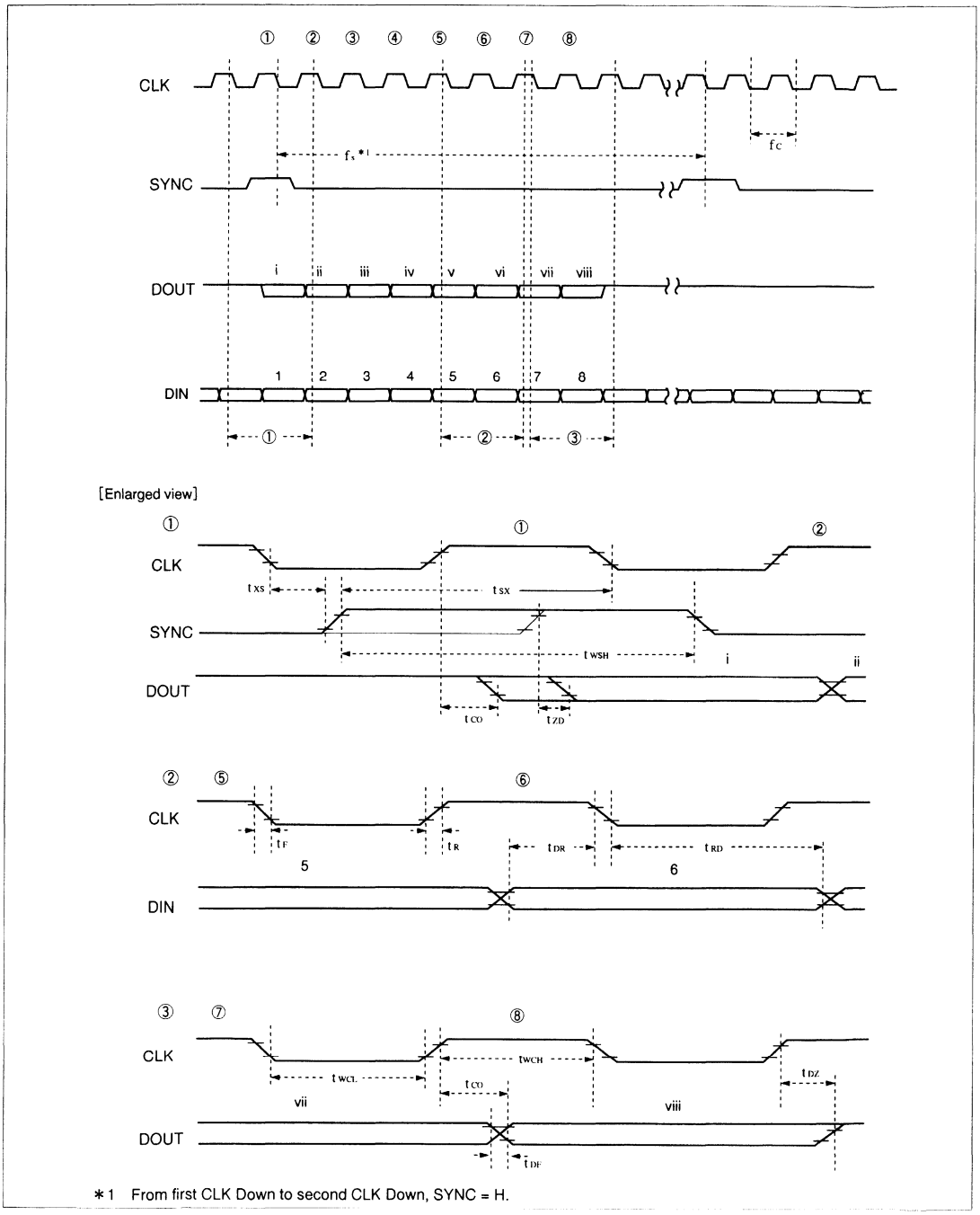
ZB: TONE and XTONE are floating, however, high resistance connection between TONE and XTONE, and between SGO and XTONE.

ZC: Floating, however high resistance connection between OP2 and BTO. Codec in [Normal] mode operates with SYNC = 8 kHz, CLK = 2048 kHz.

- When RAUD is operating, address 0111 data bit D1 value should be "0" (SW12 off).
- In tone mode, address 0111 data bit D3 should be "0" (SW2 on), and address 0111 data bit D4 should be "0" (SW14 off).
- When the SYNC and CLK pin signals are fixed at either L-level or H-level, part of the codec unit will go into power-down mode. At this time the PTBO signal will be SGC level, BTPO will be H-Z, and VRH output will be approximately 4.0 V.

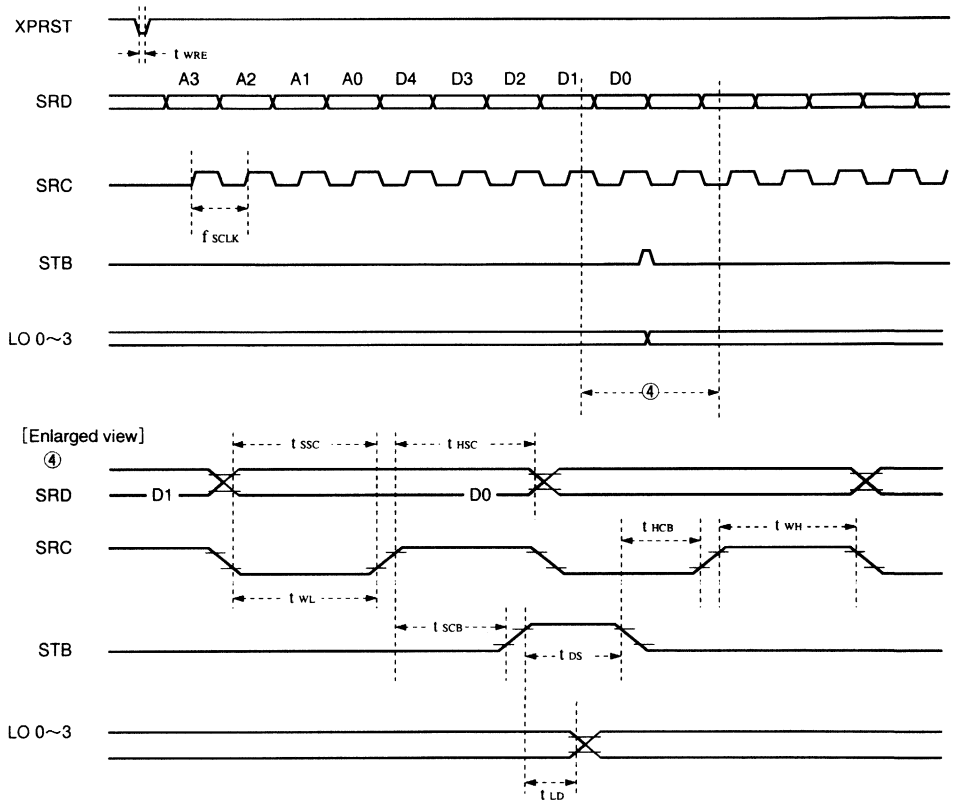
■ TIMING CHART

• Codec-Related Signals



*1 From first CLK Down to second CLK Down, SYNC = H.

• Microcomputer Data-Related Signals



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min.	Max.	
Power supply voltage	V_S	− 0.3	7.0	V
Analog input voltage	V_{AIN}	− 0.3	+V_S + 0.3	V
Digital input voltage	V_{DIN}	− 0.3	+V_S + 0.3	V
Storage temperature	Vstg	− 55	+ 125	°C

Note: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Pin name	Value			Unit
			Min.	Typ.	Max.	
Operating temperature	Ta	—	−20	+25	+80	℃
Power supply voltage	V_S	VDD, VDDAB, VDDAC, VDDSP 1, VDDSP2	4.75	5.0	5.25	V
Digital input voltage	V_L	All digital input pins	0.0	—	V_S	V
Analog output load resistance	R_{LB}	BBO, PTBO, TONEO, BTO, BTPO	75	—	—	kΩ
Analog output load capacity	C_{LB}		—	—	20	pF
Analog output load resistance*1	R_{LE}	Between EAR-XEAR	—	32	—	Ω
Analog output load capacity*2	C_{LE}		—	—	70	nF
Analog output load resistance*1	R_{LJ}	JEAR	—	32	—	Ω
Analog output load capacity*2	C_{LJ}		—	—	70	nF
Analog output load resistance*1	R_{LT}	Between TONE-XTONE	—	32	—	Ω
Analog output load capacity*2	C_{LT}		—	—	70	nF
Analog output load resistance	R_{LM1}	MICO, JMICO	10	—	—	kΩ
	R_{LM2}	SGO, BBI, OP1, OP2	50	—	—	kΩ
Analog output load capacity	C_{LM}	MICO, JMICO, SGO, BBI, OP1, OP2	—	—	20	pF
Analog output load resistance*3	R_{LM}	RAUD	5	—	—	kΩ
Analog output load capacity*3	C_{LM}		—	—	20	pF
Analog output voltage	V_{AOUT}	All analog output pins	1.25	—	3.75	V
Analog input voltage	V_{AIN}	All analog input pins	1.25	—	3.75	V

*1: Dynamic typ speakers
*2: Piezoelectric type speakers
*3: When SW8 = on, SW12 = off

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

Parameter		Symbol	Pin	Conditions	Value			Unit
					Min.	Typ.	Max.	
Power supply current at full power-down mode		I_{VSST1}	All V_{DD} pins	PSC0 = 0 : PSC1 = 0 : PSC2 = 0, Ain = AG, Din = L	—	0.5	50	μA
Power supply current with VREF operating		I_{VSST2}		PSC0 = 0 : PSC1 = 0 : PSC2 = 1, Ain = SGC, Din = L	—	480	800	μA
Power supply current with TONE operating		I_{VSST3}		PSC0 = 0 : PSC1 = 1, Ain = SGC, Din = ICN SW6 = SW7 = SW8 = SW9 = off	—	1.8	3.0	mA
Power supply current for normal operation (only speaker ampmute)		I_{VSST4}		PSC0 = 1, Ain = SGC, Din = ICN SW6 = SW7 = SW9 = off	—	8.2	12.0	mA
Speaker amp power supply voltage	Receiver amps EAR, XEAR	I_{VSST5}		PSC0 = 0, PSC1 = 1, Ain = SGC, Din = ICN, Power supply current differential when SW6 is on/off.	—	5.0	7.0	mA
	Earphone amp JEAR	I_{VSST6}		PSC0 = 0, PSC1 = 1, Ain = SGC, Din = ICN, Power supply current differential when SW7 is on/off.	—	2.7	4.0	mA
	Tone amps TONE, XTONE	I_{VSST8}		PSC0 = 0, PSC1 = 1, Ain = SGC, Din = ICN, Power supply current differential when SW9 is on/off.	—	5.0	7.0	mA
Digital input voltage		V_{IH}	All digital input pins	—	Vs*0.7	—	Vs	V
		V_{IL}		—	0	—	Vs*0.3	V
Digital input current		I_{IH}	All digital input pins except STP pin	—	—	—	10	μA
		I_{IL}		—	—	—	10	μA
Input offset voltage		V_{FM}	Between MIC-XMIC, between JMIC-XJMIC	—	−10	—	10	mA
Output offset voltage		V_{FR}	RAUD	BBI = SGC SW8 = on, SW6 = SW7 = SW9 = SW12 = off	−15	—	15	mV
		V_{FE}	Between EAR-XEAR	BBI = SGC SW6 = on, SW7 = SW8 = SW9 = SW12 = off	−20	—	20	mV
		V_{FT}	Between TONE-XTONE	IMTON = SGC SW9 = on, SW6 = SW7 = SW8 = SW12 = off	−20	—	20	mV
		V_{FP}	PTBO	Din = ICN, EV2 = 0 dB	−100	—	100	mV
		V_{OH}	Between MIC0-BBO	EV0 = 0 dB	−100	—	100	mV
		V_{OL}	Between JMIC0-BBO					

(Continued)

(Continued)

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min.	Typ.	Max.	
SGC output voltage	V_{SGC}	SGC	—	2.30	2.40	2.50	V
SGO output voltage	V_{SGO}	SGO	—	2.25	2.40	2.55	V
VRH output voltage	I_{VRH}	VRH	—	—	4.0	—	V
Digital output voltage	V_{OH}	All digital output pins	$I_{OH} = -0.5$ mA	$V_S * 0.8$	—	V_S	V
Digital output voltage	V_{OL}	All digital output pins	$I_{OL} = 0.5$ mA	0.0	—	$V_S * 0.2$	V
Resistance between pins SWI and SWO	R_{SW}	Between SWI-SWO	SW10 = on	—	—	1	kΩ

Note: Measurement conditions: ■ Standard Test Circuit

2. AC Characteristics

(1) Codec-Related Signals

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Digital input rise time	t_R	Vs∗0.3→Vs∗0.7	—	—	50	ns
Digital input fall time	t_F		—	—	50	ns
Shift clock frequency	f_C	μ-law, A-law	64	—	3152	kHz
		Linear	256	—	3152	kHz
Shift clock pulse width (H)	t_{WCH}	V_{IH}=Vs∗0.7	1/fc∗0.3	—	1/fc∗0.7	ns
Shift clock pulse width (L)	t_{WCL}	V_{IL}=Vs∗−0.3	1/fc∗0.3	—	1/fc∗0.3	ns
Sync frequency	f_S	—	—	8	—	kHz
Sync pulse width	t_{WSH}	—	1/fc	—	62	μs
SYNC to CLK setup time	t_{SX}	—	100	—	—	ns
CLK to SYNC hold time	t_{XS}	—	50	—	—	ns
CLK to DIN hold time	t_{RD}	—	50	—	—	ns
DIN to CLK setup time	t_{DR}	—	50	—	—	ns
SYNC to DOUT delay time	t_{ZD}	BIT 1	—	—	200	ns
CLK to DOUT delay time	t_{CO}	BIT 2 to 8	—	—	200	ns
CLK to DOUT disable time	t_{DZ}	"H"	—	—	200	ns
DOUT fall time	t_{DF}	—	10	—	100	ns

(2) Microcomputer Data-Related Signals

Parameter	Symbol	Pin	Value			Unit
			Min.	Typ.	Max.	
SRC to SRD data setup time	t_{SSC}	SRD, SRC	50	—	—	ns
SRC to SRD data hold time	t_{HSC}		50	—	—	ns
SRC to STB setup time	t_{SCB}	SRC, STB50	—	—	ns	
SRC pulse width (H)	t_{WH}	SRC	200	—	—	ns
SRC pulse width (L)	t_{WL}		200	—	—	ns
STB pulse width	t_{DS}	STB	50	—	—	ns
STB to SRC hold time	t_{HCB}	STB, SRC50	—	—	ns	
LO0 to 3 delay time	t_{LD}	LO0 to 3	—	—	200	ns
Shift clock frequency	f_{SCLK}	SRC	—	—	2048	kHz
Reset pulse width	t_{WRE}	XPRST	1	—	—	μs

3. Transmission Characteristics

(1) Microphone Amp System

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Gain (between MIC0 and BBO)	G_{MB}	MICO=−20 dBv, 1020 Hz SW3=on, SW4=SW5=SW14=off EV 0=0 dB	−1.5	—	1.5	dB
Gain (between JMIC0 and BBO)	G_{JB}	JMICO=−20 dBv, 1020 Hz SW4=on, SW3=SW5=SW14=off EV 0=0 dB	−1.5	—	1.5	dB
Signal to noise ratio (between MIC and BBO) (between XMIC and BBO)	S_{MB}	Ain1=−40 dBv (+20 dBgain) SW3=on, SW4=SW5=SW14=off EV0=0 dB, 1020 Hz C message	40	—	—	dB
Signal to noise ratio (between JMIC and BBO) (between XJMIC and BBO)	S_{JB}	Ain2=−40 dBv (+20 dBgain) SW4=on, SW3=SW5=SW14=off EV0=0 dB, 1020 Hz C message	40	—	—	dB

Note: Measurement conditions: ■ Standard Test Circuit

(2) Speaker Amp System

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Gain (between EAR and XEAR)	G_{BE}	BBI=−20 dBv, 1020 Hz	—	6.0	—	dB
Gain (between BBI and JEAR)	G_{BJ}	BBI=−20 dBv, 1020 Hz, ATT=0 dB	—	0.0	—	dB
	G_{BJ6}	BBI=−20 dBv, 1020 Hz, ATT=−6 dB	—	−6.0	—	dB
Gain (between BBI and RAUD)	G_{BR}	BBI=−20 dBv, 1020 Hz SW8=on, SW6=SW7=SW12=off	—	0.0	—	dB
Output power	W_E	R=32Ω, between EAR-XEAR THD=10%	10.0	—	—	mW
	W_T	R=25Ω, between TONE-XTONE gain=0 dB, THD=10%	200.0	—	—	mW
	W_J	R=32Ω, JEAR, ATT=−2.5 dB THD=10%	5.0	—	—	mW

Note: Measurement conditions: ■ Standard Test Circuit

(3) TONE System

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
TONE output level (TONE0)	G_{T1}	1 tone generated, SW2=on f_1=948.1 kHz	—	−10.0	—	dBv
	G_{T2}	2 tone generated, SW2=on f_1=948.1 kHz, f_2=1219.1 kHz	—	−10.0	—	dBv

Note: Measurement conditions: ■ Standard Test Circuit

(4) Electric Volume System

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Volume gain error EV0 (between MICO-BBO)	G_{E0}	SW3=on, SW4=SW14=off TAUD=−20 dBv, 1020 Hz	−0.7	—	0.7	dB
Volume gain error EV1 (between DIN-PTBO)	G_{E1}	D_{IN}=−20 dBm0, 1020 Hz	−0.8	—	0.8	dB
Volume gain error EV2 (between IM 2-BTO)	G_{E2}	IM2=−20 dBv, 1020 Hz	−1.0	—	1.0	dB
Volume gain error EV3 (TONEO)	G_{E3}	SW2=on 1 tone generated f1=948.1kHz	−0.5	—	0.5	dB

Note: Measurement conditions: ■ Standard test circuit

(5) Sending/Receiving System (Codec, Analog Block)

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Crosstalk (send→receive)	CTX	Ain1=1020 Hz, −40 dBv (20 dBgain) D_{IN}=ICN Measured at RAUD pin	—	—	−50	dB
Crosstalk (send→receive)	CTR	D_{IN}=1020 Hz, 0 dBm0 A_{IN}=SGC Measured at DOUT pin	—	—	−50	dB

Note: Measurement conditions: ■ Standard test circuit

(6) Codec

Parameter	Symbol	Conditions		Value			Unit
				Min.	Typ.	Max	
Gain tracking (A to D) BTPO→DOUT	GTX	1020 Hz, −10 dBm0 Reference value	+3 to −40 dBm0	−0.2	—	0.2	dB
			−40 to −50 dBm0	−0.4	—	0.4	dB
			−50 to −55 dBm0	−0.8	—	0.8	dB
Gain tracking (D to A) DIN→PTBO	GTR	1020 Hz, −10 dBm0 Reference value EV1=0 dB	+3 to −40 dBm0	−0.4	—	0.4	dB
			−40 to −50 dBm0	−0.6	—	0.6	dB
			−50 to −55 dBm0	−1.0	—	1.0	dB
Gain tracking (A to D) (Linear) BTPO→DOUT	GTXL	1020 Hz, AFST−3 dB Reference value	AFST to AFST−43 dB	−0.2	—	0.2	dB
			AFST−43 to AFST−53 dB	−0.4	—	0.4	dB
			AFST−53 to AFST−53 dB	−0.8	—	0.8	dB
Gain tracking (D to A) (Linear) DIN→PTBO	GTRL	1020 Hz, AFSR−3 dB Reference value EV1=0 dB	AFSR to AFSR−43 dB	−0.4	—	0.4	dB
			AFSR−43 to AFSR−53 dB	−0.6	—	0.6	dB
			AFSR−53 to AFSR−53 dB	−1.0	—	1.0	dB
Sending frequency characteristics (A to D) BTPO→DOUT	FRX	0 dBm0 (Linear : AFST−3 dB) 1020 Hz Reference value	0 to 60 Hz	24.0	—	—	dB
			60 to 300 Hz	−0.20	—	—	dB
			300 to 3000 Hz	−0.20	—	0.20	dB
			3000 to 3400 Hz	−0.20	—	0.8	dB
			3400 to 4600 Hz	*	—	—	dB
			4600 to 12 kHz	32.0	—	—	dB
Receiving frequency characteristics (D to A) DIN→PTBO	FRR	0 dBm0 (Linear : AFSR−3 dB) 1020 Hz Reference value EV1=0 dB	0 to 300 Hz	−0.30	—	—	dB
			300 to 3000 Hz	−0.30	—	0.30	dB
			3000 to 3400 Hz	−0.30	—	1.10	dB
			3400 to 4600 Hz	*	—	—	dB
			4600 to 12 kHz	32.0	—	—	dB
Sending absolute gain (A to D) BTPO→DOUT	GAX	1020 Hz, 0 dBm0 (Linear : AFST−3 dB) EV1=0 dB, Vs=3.0 V, Ta=+25°C		−2.0	0	−2.0	dB
		Power supply variation		—	±0.02	—	dB
		Temperature variation		—	±0.001	—	dB/°C
Receiving absolute gain (D to A) DIN→PTBO	GAR	1020 Hz, 0 dBm0 (Linear : AFSR−3 dB) Vs=3.0 V, Ta=+25°C		−2.50	0	2.50	dB
		Power supply variation		—	±0.04	—	dB
		Temperature variation		—	±0.002	—	dB/°C
Absolute level	VABS	Over load level μ-Law=3.17 dB A-Law=3.14 dB		—	1.2081	—	V_{OP}

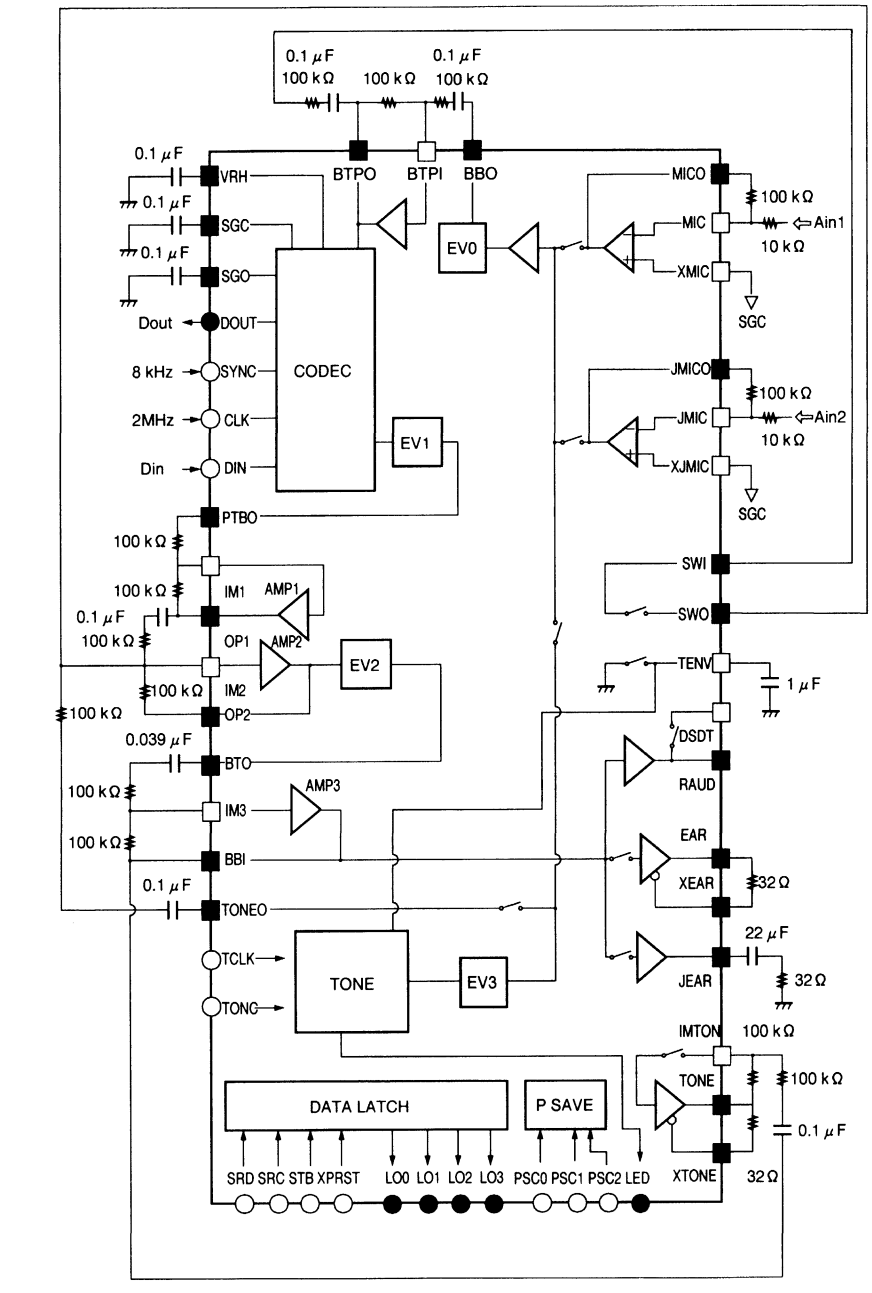
(Continued)

(Continued)

Parameter	Symbol	Conditions		Value Min.	Value Typ.	Value Max	Unit
Sending signal to noise ratio BTPO→DOUT	SDX	1020 Hz C message (A to D)	0 to −30 dBm0	34.0	—	—	dB
			−40 dBm0	28.0	—	—	dB
			−45 dBm0	23.0	—	—	dB
Receiving signal to noise ratio DIN→DOUT	SDR	1020 Hz C message (D to A)	0 to −30 dBm0	33.0	—	—	dB
			−40 dBm0	27.0	—	—	dB
			−45 dBm0	22.0	—	—	dB
Sending signal to noise ratio BTPO→DOUT (Linear)	SDXL	1020 Hz C message (A to D)	AFST−3 to AFST−33 dB	34.0	—	—	dB
			AFST−43 dB	28.0	—	—	dB
			AFST−45 dB	23.0	—	—	dB
Receiving signal to noise ratio BTPO→DOUT (Linear)	SDRL	1020 Hz C message (D to A)	AFSR−3 to AFSR−33 dB	34.0	—	—	dB
			AFSR−43 dB	28.0	—	—	dB
			AFSR−45 dB	23.0	—	—	dB
Sending no-talk noise BTPO→DOUT	ICNX	C message (A to D)		—	−72	−70	dBm0C
Receiving no-talk noise DIN→PTBO	ICNR	C message (D to A)		—	−72	−70	dBm0C
Analog input level BTPO	AILU	1020 Hz, 0 dBm0, Ta=+25°C Vs=3.0 V μ-law		0.4692	0.5907	0.7437	Vrms
Analog output level PTBO	AOLU	1020 Hz, 0 dBm0, Ta=+25°C Vs=3.0 V μ-law		0.4692	0.5907	0.7437	Vrms
Analog input level BTPO	AILA	1020 Hz, 0 dBm0, Ta=+25°C Vs=3.0 V A-law		0.4728	0.5952	0.7493	Vrms
Analog output level PTBO	AOLA	1020 Hz, 0 dBm0, Ta=+25°C Vs=3.0 V A-law		0.4728	0.5927	0.7493	Vrms
Analog input fullscale level BTPO	AFST	Vs=3.0 V, Ta=+25°C Linear		0.9596	1.2081	1.5211	V_{OP}
Analog output fullscale level PTBO	AFSR	Vs=3.0 V, Ta=+25°C Linear		0.9596	1.2081	1.5211	V_{OP}

∗ : $14.5 \times \left\{1 - \mathrm{SIN}\frac{\pi\,(4000-f)}{1200}\right\}$

■ STANDARD TEST CIRCUIT



○ : Digital input ● : Digital output □ : Analog input ■ : Analog output ◪ : Input/output ▲ : V_{DD} △ : GND

Note: Sufficient path capacitance must be placed between VDDAB–BAG, VDDAC–CAG, VDDSP1–SPG1, VDDSP2–SPG2, VDD–AG.

■ ORDERING INFORMATION

Part number	Package	Remarks
MB86434PF	64 pins, Plastic QFP (FPT-64P-M07)	

MEMO

FUJITSU SEMICONDUCTOR
DATA SHEET

DS04–23004–1E

ASSP

CMOS

3V Single Power Supply Audio Interface Unit (AIU)

MB86435

■ DESCRIPTION

The FUJITSU MB86435 is an AIU (audio interface unit) LSI for +3 V single-power source digital telephone devices, manufactured using CMOS process technology. The codec transmission filter characteristics meet G.712 standards, and can handle input and output in A-Law, μ-Law and linear conversion modes. The MB86435 also contains the necessary DTMF, microphone and receiver amps for telephone devices.

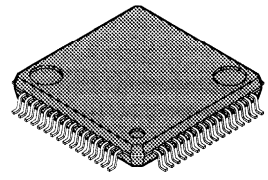
■ FEATURES

- +3 V single power supply
- Low power consumption : muting settings for each operating mode
  - Normal operation : 6.0 mA TYP (speaker amp mute)
  - Tone generation : 1.8 mA TYP (speaker amp mute)
  - Standby mode : 0.5 μA TYP
- On-chip codec filter meets G.712 standards
- Selection of codec conversion methods (A-law, μ-law, linear)
- On-chip low-noise microphone amp (2-channel) (0 to 35 dB amplification)
- On-chip receiver speaker amps (32 ΩBTL type: 6.4 mW MIN)
- On-chip tone speaker amp (25 ΩBTL type: 10 mW MIN)
- On-chip earphone speaker amps (32 Ω single type: 2 mW MIN)

(Continued)

■ PACKAGE

64 pin, Plastic SQFP



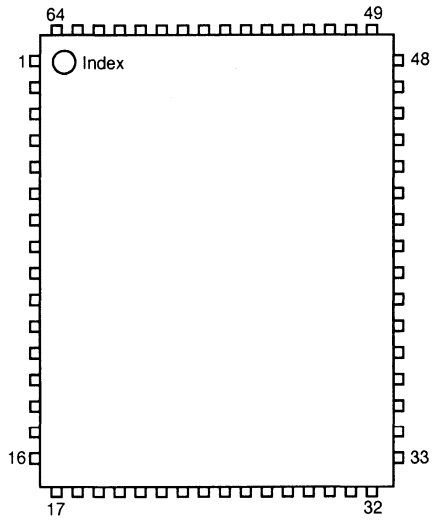
(FPT-64P-M03)

(Continued)

- On-chip electronic volume gain adjustments (sending, receiving, tone)
- On-chip accessory input/output circuits
- DTMF generator function
- Service tone generation
- CMOS compatible input/output

■ PIN ASSIGNMENT

(TOP VIEW)



(FPT-64P-M03)

■ PIN DESCRIPTION

Pin No.	Symbol	I/O	A/D	Description
1	VRH	O	A	Bypass capacitor connector pin for the A/D D/A referencevoltage generator circuit. Place capacitor between VRH and CAG pins.
2	SGC	O	A	Bypass capacitor connector pin for the signal ground potential generator circuit. Place capacitor between SGC and CAG pins.
3	VDDAC	P	A	Analog power supply pin for codec block. To be set within range 2.7 to 3.6 V.
6	SYNC	I	D	PCM codec send/receive synchronization signal input pin. Operating clock frequency 8 kHz. CMOS interface. Constant H/L level signal will cause part of codec block to power-down.
7	CLK	I	D	Send/receive PCM signal series bit rate setting input pin. Data rate for μ-law, A-law modes may be set to any level in the range 64 k to 3.152 MHz, and for linear mode in the range 256 k to 3.152 MHz. Constant H or L level signal will cause part of codec block to power-down. CMOS interface.
8	DIN	I	D	PCM signal input pin. This signal is picked up internally at the fall of the CLK signal. CMOS interface.
9	DOUT	O	D	PCM signal output pin. Data is output in sync with the rise of the CLK signal. After data output, loses PLL synchronization, and at power-down this signal is fixed at H level. CMOS interface.
10	VDD	P	D	Digital power supply pin. To be set within range 2.7 to 3.6 V.
11	DG	G	D	Digital ground pin. To be set to 0V.
12	PSC0	I	D	Power-down control signal input pin. CMOS interface. Used with PSC1,2 pins for power-down settings.
13	PSC1	I	D	Power-down control signal input pin. CMOS interface. Used with PSC0,2 pins for power-down settings.
14	PSC2	I	D	Power-down control signal input pin. CMOS interface. Used with PSC0,1 pins for power-down settings.
15	SRD	I	D	9-bit serial data input pin. CMOS interface. Data is written at the rise of the signal from this pin.
16	SRC	I	D	Clock input pin for 9-bit serial data writing. CMOS interface. Data is written at the rise of this pin.
17	STB	I	D	Serial data latch strobe signal. Data is latched by the L level signal. CMOS interface.
18	XPRST	I	D	Digital reset signal input pin. CMOS interface. L level: internal latch initialization H level: normal operation
19	LO0	O	D	External control latch output pin. Outputs value D_0 of address 1000. CMOS interface.
20	LO1	O	D	External control latch output pin. Outputs value D_1 of address 1000. CMOS interface.

PSC 2 1 0
0 0 0 Full power-down
1 0 0 V_{REF} operating
— 1 0 Tone operating
— — 1 All operations available
(—: value not determined)

(Continued)

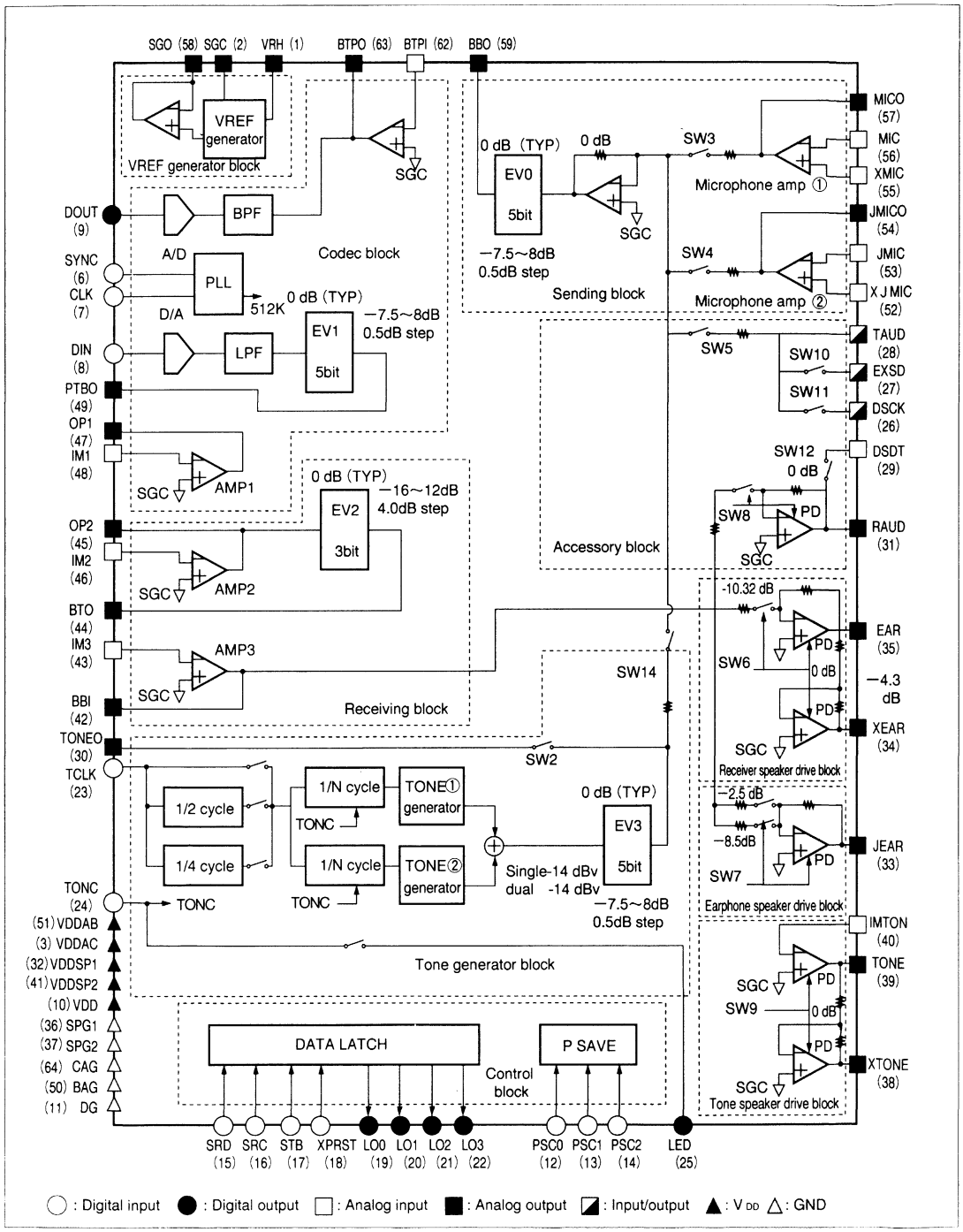
Pin No.	Symbol	I/O	A/D	Description
21	LO2	O	D	External control latch output pin. Outputs value D_2 of address 1000. CMOS interface.
22	LO3	O	D	External control latch output pin. Outputs value D_3 of address 1000. CMOS interface.
23	TCLK	I	D	Tone generator clock input pin. Can be used as a tone CLK signal by using address 1110 D4D3 to subdivide the internal clock signal by factors of 1/1, 1/2, 1/4. CMOS interface.
24	TONC	I	D	Tone generator cycle control input pin. CMOS interface. Hlevel signal outputs tone.
25	LED	O	D	Ring LED control output pin. CMOS interface.
26	DSCK	I/O	A	Can be connected to EXSD or TAUD by switching bus.
27	EXSD	I/O	A	Can be connected to DSCK or TAUD by switching bus.
28	TAUD	I/O	A	Can be connected to EXSD or DSCK by switching bus.
29	DSDT	I	A	Can be connected to RAUD by switching bus.
30	TONEO	O	A	Tone signal output pin.
31	RAUD	O	A	Output pin for external speaker, or audio test signal. Can be connected to DSDT by switching paths.
32	VDDSP1	P	A	Speaker amp power supply pin. To be set within range 2.7 to 3.6 V.
33	JEAR		O	Earphone speaker amp output pin. Capable of 2 mW output at 32 Ω load.
34	XEAR	O	A	Receiver speaker amp output pin. Internally connected to EAR and BTL. Maximum output of 6.4 mW can be obtained at 32 Ω load by connecting speaker between EAR and XEAR.
35	EAR	O	A	Receiver speaker amp output pin. Connected to XEAR and BTL.
36	SPG1	G	A	Speaker amp ground pin. To be set to 0 V
37	SPG2	G	A	Speaker amp ground pin. To be set to 0 V.
38	XTONE	O	A	Speaker amp tone output pin. Internally connected to TONE and BLT. Maximum output of 10 mW can be obtained at 25 Ω load by connecting speaker between TONE and XTONE.
39	TONE	O	A	Speaker amp tone output pin. When speaker amp is not used for tone, TONE should be shorted to IMTON.
40	IMTON	I	A	Speaker drive inverted (–) signal input pin. Can be used to adjust gain by connecting resistance to TONE and IMTON.
41	VDDSP 2	P	A	Speaker amp power supply pin. To be set within range 2.7 to 3.6 V.
42	BBI	O	A	AMP3 output pin. Should be included in HPF together with IM3, to prevent DC offset from entering speakers.
43	IM3	I	A	AMP3 inverted (–) signal input pin.
44	BTO	O	A	Receiving volume adjustment circuit output pin.

(Continued)

(Continued)

Pin No.	Symbol	I/O	A/D	Description
45	OP2	O	A	AMP2 output pin. If AMP2 is not used, IM2 should be shorted to OP2.
46	IM2	I	A	AMP2 inverted (–) signal input pin. Can form a circuit with OP2 to add sidetone or tone. Melody circuits, if used, can alsobe connected here.
47	OP1	O	A	AMP1 output pin. Can form a circuit with IM1 to include LPF or HPF in receiving block. If AMP1 is not used, IM1 should be shorted to OP1.
48	IM1	I	A	AMP1 inverted (–) signal input pin.
49	PTBO	O	A	PCM receiver output pin.
50	BAG	G	A	Analog ground pin for sending, receiving blocks. To be set to 0 V.
51	VDDAB	P	A	Analog power supply pin for sending, receiving blocks. To be set within range 2.7 to 3.6 V.
52	XJMIC	I	A	Microphone amp (2) non-inverted (+) signal input pin.
53	JMIC	I	A	Microphone amp (2) inverted (–) signal input pin.
54	JMICO	O	A	Microphone amp (2) output pin.
55	XMICI	I	A	Microphone amp (1) non-inverted (+) signal input pin.
56	MIC	I	A	Microphone amp (1) inverted (–) signal input pin.
57	MICO	O	A	Microphone amp (1) output pin.
58	SGO	O	A	Sending block signal ground potential output pin. Buffers SGC voltage.
59	BBO	O	A	Sending analog signal output pin.
62	BTPI	I	A	PCM ENCODE block input OP amp negative input pin.
63	BTPO	O	A	PCM ENCODE block input OP amp output pin.
64	CAG	G	A	Analog ground pin for codec block. To be set to 0 V.
4, 5, 60, 61	NC	—	—	Not connected. To be left open.

■ BLOCK DIAGRAM



■ FUNCTIONAL DESCRIPTION

1. Register Settings

The MB86435 IC chip controls all electronic volume, switching, tone generator circuits and power-down control circuits by means of the SRD, STB and SRC data input signals.

The MB86435 uses a 9-bit serial data format consisting of a 4-bit address followed by 5 data bits. Data is picked up at the rise of the SRC signal, and latched by the STB L-level signal. The 9-bits of serial data preceding the STB signal are considered valid. These register settings are not reset at power-down. They can be reset when data is initialized by an XPRST L-level signal.

(1) Mode Settings

Control segment	Address	Data bit	Setting description	Initial data bit setting (at reset)	Remarks
	A_3 A_2 A_1 A_0	$D_4D_3D_2D_1D_0$		$D_4D_3D_2D_1D_0$	
EV0	0 0 0 1	$D_4D_3D_2D_1D_0$	Sending audio level adjustment. Adjusts EV0 gain.	0 1 1 1 1	
EV1	0 0 1 0	$D_4D_3D_2D_1D_0$	Sending audio level adjustment. Adjusts EV1 gain.	0 1 1 1 1	*1
EV2	0 0 1 1	* * $D_2D_1D_0$	Sending audio level adjustment. Adjusts EV2 gain.	* * 1 0 0	
TX-MUTE	0 1 0 0	D_4 * * * D_0	D_0: Sending audio mute SW 3, 4, 5 on/off control. Mute: 1, Unmute: 0	0 * * * 0	*2, *3
RX-MUTE			D_4: Sending audio mute SW 6, 7, 8, 9 on/off control. Mute: 1, Unmute: 0		*3, *4
SW5	0 1 0 1	D_4 * $D_2D_1D_0$	D_0: TAUD mute SW 5 on/off control. Mute: 1, Unmute: 0	0 * 0 0 0	*2, *5
SW4			D_1: JMIC mute SW 4 on/off control. Mute: 1, Unmute: 0		*2
SW3			D_2: MIC mute SW 3 on/off control. Mute: 1, Unmute: 0		
SW8			D_4: RAUD mute SW 8 on/off control. Mute: 1, Unmute: 0		*3, *4, *6
SW6	0 1 1 0	D_4 * $D_2D_1D_0$	D_0: EAR, XEAR mute SW 6 on/off control. Mute: 1, Unmute: 0	0 * 0 0 0	*4
SW9			D_1: TONE, XTONE mute SW 9 on/off control. Mute: 1, Unmute: 0		
SW7			D_2: JEAR mute SW 7 on/off control. Mute: 1, Unmute: 0		
ATT			D_4: JEAR attenuation level switch. 0: -2.5 dB, 1: -8.5 dB.		
SW10	0 1 1 1	$D_4D_3D_2D_1D_0$	D_0: EXSD pin selection SW 10 on/off control. On: 1, Off: 0	0 0 0 0 0	*3, *5
SW12			D_1: DSDT pin selection SW 12 on/off control. On: 1, Off: 0		*3, *6
SW11			D_2: DSCK pin selection SW 12 on/off On: 1, Off: 0		*3, *5
SW2			D_3: TONEO mute SW 2 on/off control. Mute: 1, Unmute: 0		*7
SW14			D_4: TONE sending add SW 14 on/off control. On: 1, Off: 0		

(Continued)

(Continued)

Control segment		Address	Data bit	Setting description	Initial data bit setting (at reset)	Remarks
		A_3 A_2 A_1 A_0	D_4 D_3 D_2 D_1 D_0		D_4 D_3 D_2 D_1 D_0	
Serial / parallel converter		1 0 0 0	* D_3 D_2 D_1 D_0	Parallel output D_3=LO3, D_2=LO2, D_1=LO1, D_0=LO0	* 0 0 0 0	*8
EV3		1 0 0 1	D_4 D_3 D_2 D_1 D_0	Tone level adjustment. Adjusts EV3 gain.	0 1 1 1 1	*1
TONE control	Frequency control	1 0 1 0	X_8 X_7 X_6 X_5 X_4	Tone (1) frequency control, set by 8-bit value X_7 to X_0. X_8 = 1 to output trapezoidal wave, X_8 = 0 to output sine wave.	0 0 0 0 0	*9, *10
		1 0 1 1	* X_3 X_2 X_1 X_0		* 0 0 1 0	
		1 1 0 0	Y_8 Y_7 Y_6 Y_5 Y_4	Tone (2) frequency control, set by 8-bit value Y_7 to Y_0. Y_8 = 1 to output trapezoidal wave, Y8 = 0 to output sine wave.	0 0 0 0 0	
		1 1 0 1	* Y_3 Y_2 Y_1 Y_0		* 0 0 1 0	
	Output control	1 1 1 0	D_4 D_3 D_2 D_1 D_0	Tone generator control D_0: tone (2) on/off control. On: 1, off: 0 D_1: tone (1) on/off control. On: 1, off: 0 D_2: LED output on/off control. On: 1, off: 0	0 0 1 1 1	*7, *11, *12
	Master clock control			Tone CLK D_4, D_3 0 0 : TCLK1/1 frequency selected 0 1 : TCLK1/2 frequency selected 1 0 : TCLK1/4 frequency selected 1 1 : Prohibited		*9
PCM		1 1 1 1	* * * D_1 D_0	PCM control D_1, D_0 0 0 : μ-law mode selected 1 0 : A-law mode selected 0 1 : linear mode selected	* * * 0 0	*13, *14
TEST		0 0 0 0	D_4 D_3 D_2 D_1 D_0	Do not write in test mode.	0 0 0 0 0	

*1: See (4) Electronic Volume Controls
*2: See (2) Sending Audio Mute Setting
*3: See 5. Power Saving Modes
*4: See (3) Receiving Audio Mute Settings
*5: See 2. Analog Input (2) Accessory Input
*6: See 3. Analog Output (2) Accessory Output
*7: See (5) Tone Generator Circuit • Tone Generator Control Output Level
*8: See (8) Parallel Output
*9: See (5) Tone Generator Circuit • Tone Frequency Control Registers
*10: See (5) Tone Generator Circuit • Tone Output Waveforms
*11: See (5) Tone Generator Circuit • Tone Output Controls
*12: See (5) Tone Generator Circuit • LED Output Controls
*13: See (6) Codec Input/Output
*14: See (7) The Codec SYNC Pin

(2) Sending Audio Mute Settings

Switches SW 3 to SW 5 have the following functions. Address 0100 signals have priority.

Setting			Switching setting		
Address	A_3 A_2 A_1 A_0	A_3 A_2 A_1 A_0			
	0 1 0 0	0 1 0 1			
	D_4 D_3 D_2 D_1 D_0	D_4 D_3 D_2 D_1 D_0	SW 3	SW4	SW5
Data bit	— * * * 1	— * — — —	○	○	○
	— * * * 0	— * — — 1	—	—	○
	— * * * 0	— * — 1 —	—	○	—
	— * * * 0	— * 1 — —	○	—	—
	— * * * 0	— * — — 0	—	—	×
	— * * * 0	— * — 0 —	—	×	—
	— * * * 0	— * 0 — —	×	—	—

○ : muted, × : unmuted, — : not determined

(3) Receiving Audio Mute Settings

Switches SW 6 to SW 9 have the following functions. Address 0100 signals have priority.

Setting				Switching setting			
Address	A_3 A_2 A_1 A_0	A_3 A_2 A_1 A_0	A_3 A_2 A_1 A_0				
	0 1 0 0	0 1 0 1	0 1 1 0				
	D_4 D_3 D_2 D_1 D_0	D_4 D_3 D_2 D_1 D_0	D_4 D_3 D_2 D_1 D_0	SW 8	SW 7	SW 9	SW 6
Data bit	1 * * * —	— * — — —	— * — — —	○	○	○	○
	0 * * * —	— * — — —	— * — — 1	—	—	—	○
	0 * * * —	— * — — —	— * — 1 —	—	—	○	—
	0 * * * —	— * — — —	— * 1 — —	—	○	—	—
	0 * * * —	1 * — — —	— * — — —	○	—	—	—
	0 * * * —	— * — — —	— * — — 0	—	—	—	×
	0 * * * —	— * — — —	— * — 0 —	—	—	×	—
	0 * * * —	— * — — —	— * 0 — —	—	×	—	—
	0 * * * —	0 * — — —	— * — — —	×	—	—	—

○ : muted, × : unmuted, — : not determined

(4) Electronic Volume Controls

There are four different electronic volume controls, EV0 through EV3, with the following specifications. Electronic volume control settings are made by the SRD, SRC and STB signals, and setting values are reset by the XPRST signal. However, settings are not reset by PSC0, PSC1, PSC2 power-down mode operations.

Table 1 Relation of Volume Control Data bit Values to Gain

Step	Data bit value	EV0 sending gain adjustment	EV1 receiving gain adjustment	EV2 receiver volume adjustment	EV3 tone gain adjustment	Unit
	D_4 D_3 D_2 D_1 D_0	Typ.	Typ.	Typ.	Typ.	
0	0 0 0 0 0	−7.5	−7.5	−16	−7.5	
1	0 0 0 0 1	−7.0	−7.0	−12	−7.0	
2	0 0 0 1 0	−6.5	−6.5	−8	−6.5	
3	0 0 0 1 1	−6.0	−6.0	−4	−6.0	
4	0 0 1 0 0	−5.5	−5.5	0	−5.5	
5	0 0 1 0 1	−5.0	−5.0	4	−5.0	
6	0 0 1 1 0	−4.5	−4.5	8	−4.5	
7	0 0 1 1 1	−4.0	−4.0	12	−4.0	
8	0 1 0 0 0	−3.5	−3.5		−3.5	
9	0 1 0 0 1	−3.0	−3.0		−3.0	
10	0 1 0 1 0	−2.5	−2.5		−2.5	
11	0 1 0 1 1	−2.0	−2.0		−2.0	
12	0 1 1 0 0	−1.5	−1.5		−1.5	
13	0 1 1 0 1	−1.0	−1.0		−1.0	
14	0 1 1 1 0	−0.5	−0.5		−0.5	
15	0 1 1 1 1	0.0	0.0		0.0	
16	1 0 0 0 0	0.5	0.5		0.5	dB
17	1 0 0 0 1	1.0	1.0		1.0	
18	1 0 0 1 0	1.5	1.5		1.5	
19	1 0 0 1 1	2.0	2.0		2.0	
20	1 0 1 0 0	2.5	2.5		2.5	
21	1 0 1 0 1	3.0	3.0		3.0	
22	1 0 1 1 0	3.5	3.5		3.5	
23	1 0 1 1 1	4.0	4.0		4.0	
24	1 1 0 0 0	4.5	4.5		4.5	
25	1 1 0 0 1	5.0	5.0		5.0	
26	1 1 0 1 0	5.5	5.5		5.5	
27	1 1 0 1 1	6.0	6.0		6.0	
28	1 1 1 0 0	6.5	6.5		6.5	
29	1 1 1 0 1	7.0	7.0		7.0	
30	1 1 1 1 0	7.5	7.5		7.5	
31	1 1 1 1 1	8.0	8.0		8.0	

Note: Each setting value is determined in relation to the initial setting value.
Returns to initial value at reset (—— parts)
EV2 data bits D_4, D_3 are *.

Table 2 Volume Gain Deviation

Volume control No.	Condition	Min.	Typ.	Max.	Unit
EV0 EV1 EV3	Gain deviation, with respect to reference value shown in Table1	Reference value − 0.5 dB	Reference value	Reference value + 0.5 dB	dB
EV2	Input frequency = 1020 Hz Input level = − 20 dBv	Reference value − 1.0 dB	Reference value	Reference value + 1.0 dB	

(5) Tone Generator Circuit

- **Tone Frequency Control Registers**
  The tone generator uses a clock signal obtained by subdividing the TCLK clock signal input by 1/1, 1/2 or 1/4 according to the data bit in address 1110.

Table 3 Tone Clock Frequency Register Control

Address 1110		Tone generator clock signal (f_{IN})
D_4	D_3	
0	0	TCLK input clock signal
0	1	TCLK input clock signal subdivided by 1/2
1	0	TCLK input clock signal subdivided by 1/4
1	1	Prohibited

Frequency settings available through the tone frequency control register are determined by the following formula.
Frequency setting $f = f_{IN}/(12 * (1+n))$, n=1, 2, 3, ..., 255. (where f_{IN}: tone generator clock signal frequency).
Therefore the available frequency setting range when f_{IN} = 512 kHz is between f_{min} = 167 Hz and f_{max} = 21333 Hz.

Frequency settings corresponding to each DTMF rated reference frequency are shown in the following table.

Table 4 Tone Frequency Register Control

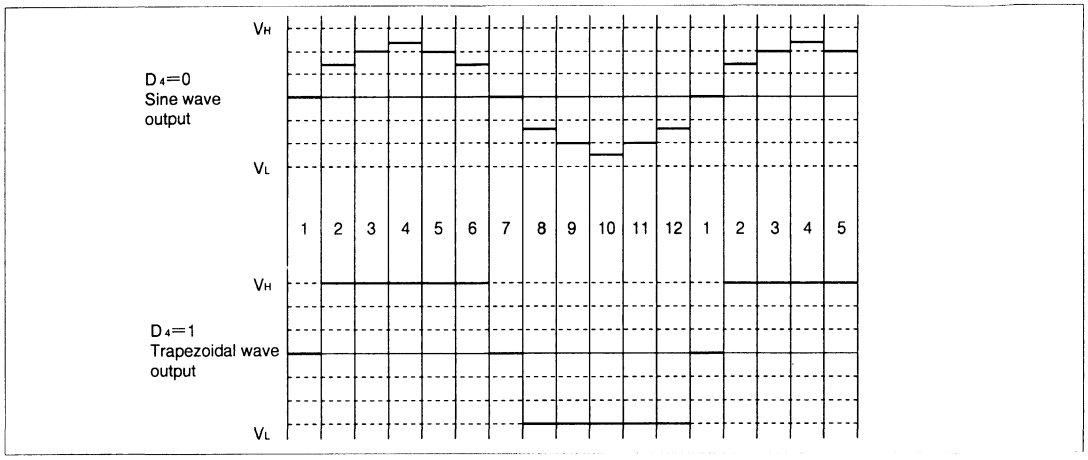
(Condition: 512 kHz)

Tone type		Rated reference frequency (generator frequency)	Frequency setting	Address 1010/1100 Data bit D_4 D_3 D_2 D_1 D_0	Address 1011/1101 Data bit D_4 D_3 D_2 D_1 D_0	n	Error
Service tone (single tone)		262 Hz	261.7 Hz	— 1 0 1 0	* 0 0 1 0	162	−0.11%
		384 Hz	384.4 Hz	— 0 1 1 0	* 1 1 1 0	110	0.10%
		400 Hz	398.7 Hz	— 0 1 1 0	* 1 0 1 0	106	−0.32%
		2000 Hz	2031.7 Hz	— 0 0 0 1	* 0 1 0 0	20	1.56%
		2600 Hz	2666.7 Hz	— 0 0 0 0	* 1 1 1 1	15	2.50%
DTMF	Low tone	697 Hz	699.4 Hz	— 0 0 1 1	* 1 1 0 0	60	0.34%
		770 Hz	775.7 Hz	— 0 0 1 1	* 0 1 1 0	54	0.74%
		852 Hz	853.3 Hz	— 0 0 1 1	* 0 0 0 1	49	0.15%
		941 Hz	948.1 Hz	— 0 0 1 0	* 1 1 0 0	44	0.75%
	High tone	1209 Hz	1219.0 Hz	— 0 0 1 0	* 0 0 1 0	34	0.82%
		1336 Hz	1333.3 Hz	— 0 0 0 1	* 1 1 1 1	31	−0.20%
		1477 Hz	1471.3 Hz	— 0 0 0 1	* 1 1 0 0	28	−0.38%
		1633 Hz	1641.0 Hz	— 0 0 0 1	* 1 0 0 1	25	0.48%

Note: • Setting values are BIN display values
• Error represents frequency setting error with respect to rated reference frequency.

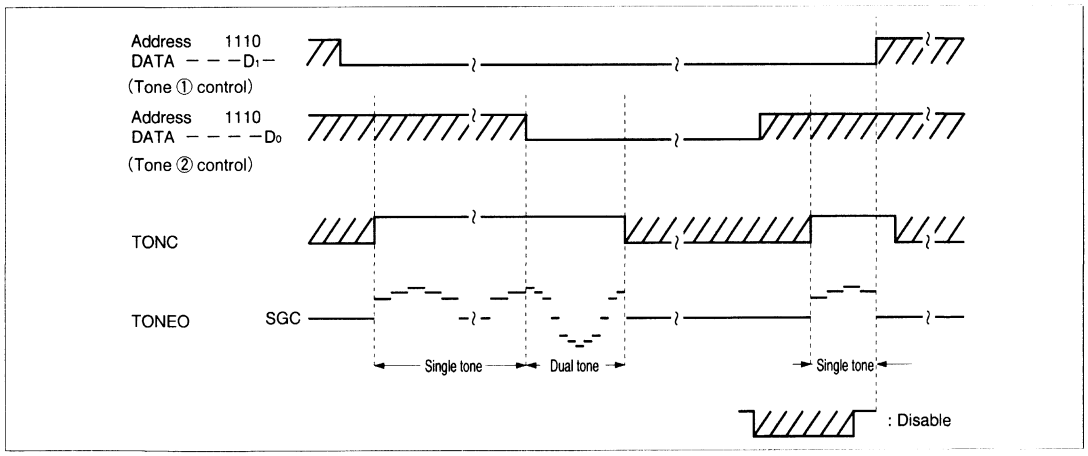
• Tone Output Waveform

The D_4 data bit at address 1010, 1100 may be used to select either sine-wave or trapezoidal waveforms for tone output.



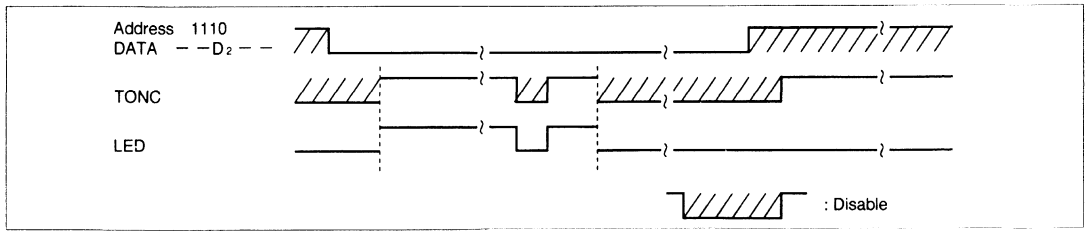
• Tone Output Control

Tone output may be controlled by address and through the external tone control input pin TONC. In addition, the tone control offers a choice of sine or trapezoidal waveforms.



• LED Output Controls

Output from the LED output pins can be controlled by the TONC signal and the address 1110 data bit D_2. When the TONC signal is H-level, and the address 1110 data bit D_2 value is L-level, the output level will be high. Output levels are CMOS levels.



• Tone Generator Control Output Level

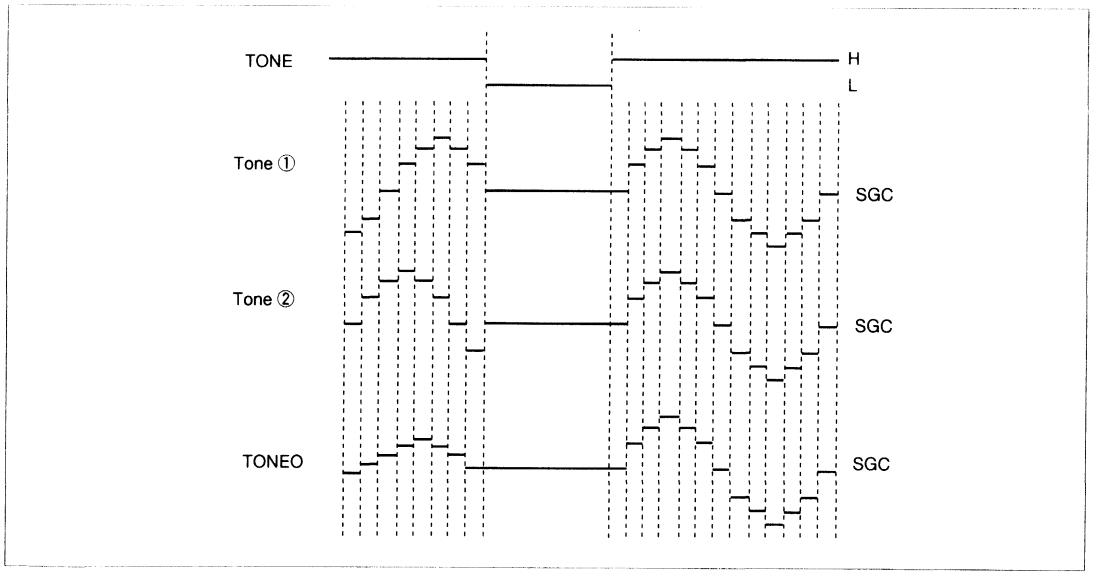
(Condition: EV3 = 0 dB)

External pins				Address 1110 data bits			Address 0111 data bits	Tone generator circuit operating mode		Output pin mode		Remarks
PSC2	PSC1	PSC0	TONC	D_2	D_1	D_0	D_3 (SW2)	Tone ①	Tone ②	LED	TONEO	
0	0	0	—	—	—	—	—	×	×	L	H-Z	
1	0	0	—	—	—	—	—	×	×	L	H-Z	
—	1 or 1		0	—	—	—	0	SGC	SGC	L	SGC	
—	1 or 1		0	—	—	—	1	SGC	SGC	L	H-Z	
—	1 or 1		1	1	—	—	—	—	—	L	—	
—	1 or 1		1	0	—	—	—	—	—	○	—	
—	1 or 1		1	—	1	1	0	SGC	SGC	—	SGC	
—	1 or 1		1	—	1	0	0	SGC	○	—	−14 dBv	Single tone output
—	1 or 1		1	—	0	1	0	○	SGC	—	−14 dBv	Single tone output
—	1 or 1		1	—	0	0	0	○	○	—	−14 dBv	Dual tone output

○ : Operational, × : Power down, H-Z : High-impedance, L : L-level fixed, SGC : SGC fixed

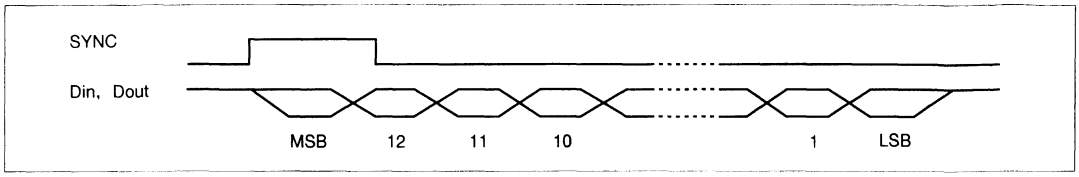
Note: When the TONC pin signal is L-level, the tone generator circuit counters will be reset. When a dual tone is generated at the time of reset, the initial phase settings for tone ① and tone ② will be in phase.

• Example: When Tone ①, Tone ② are at the same frequency:



(6) Codec Input/Output

Both the μ-law and A-law coding/decoding conversion processes used by the MB86435 codec are compatible with CCITT Recommendation G.711. In addition, linear coding in the form of 14-bit two's complement code can be output starting with MSB values.



MSB	Code	LSB	PTBO reference voltage (V)
0	1 1 1 1 1 1 1 1 1 1 1 1 1		0.7354
	⟆		⟆
0	0 0 0 0 0 0 0 0 0 0 0 0 1		1.4991
0	0 0 0 0 0 0 0 0 0 0 0 0 0		1.5000
1	1 1 1 1 1 1 1 1 1 1 1 1 1		1.5009
	⟆		⟆
1	0 0 0 0 0 0 0 0 0 0 0 0 1		2.2647

(7) The Codec SYNC Pin

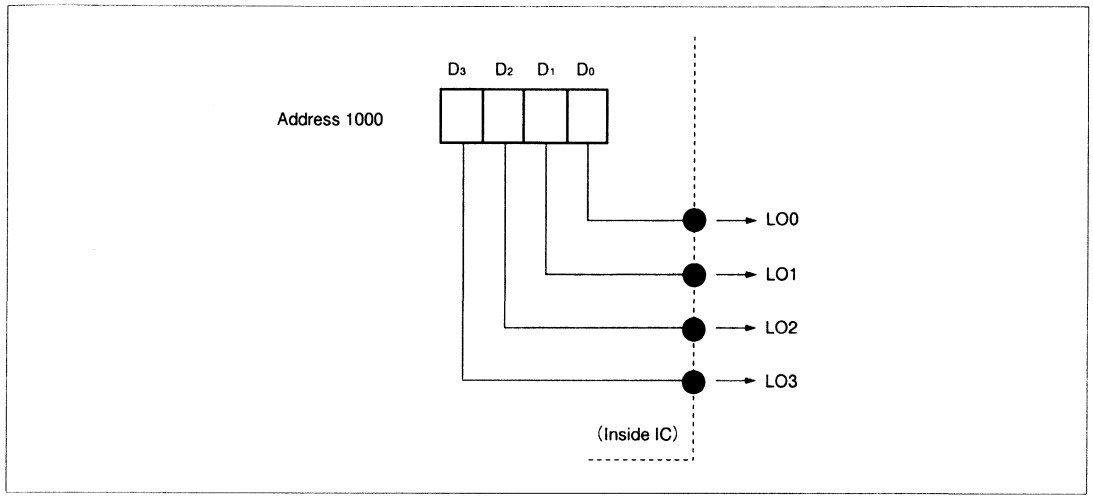
The codec block requires the input of an 8 kHz sampling clock signal at the SYNC pin, as well as a data transfer clock at the CLK pin. In order to conserve power consumption, whenever the SYNC pin or CLK pin signal is inactive, the system goes into SYNC power-down mode and stops code conversion.

Also, if either the SYNC or CLK pins encounters jitter of 5 μs or greater, the system may go into power-down mode.Table 1.10 shows the status of output pins in SYNC power-down mode.

Pin symbol	Operation
SGC	Normal operation (1.5 V)
SGO	Normal operation (1.5 V)
VRH	Normal operation (2.5 V)
DOUT	H-level fixed
PTBO	SGC
BTPO	High impedance

(8) Parallel Output

The LO0 to 3 pins carry latched output for external controls. The data written to address 1000 can be output through these pins. Output is CMOS output.



2. Analog Input

Analog input signals in the MB86435 include the two microphone inputs and the three accessory input.

(1) Microphone Amps

The microphone amps take the incoming signal from the microphones and amplify it to any desired level of gain. The microphone lines are low-noise types for use with piezoelectric-ceramic or capacitor microphones, and are capable of a wide range of amplification. All microphones and amps must be coupled with capacitors to prevent amplification of offset signals.

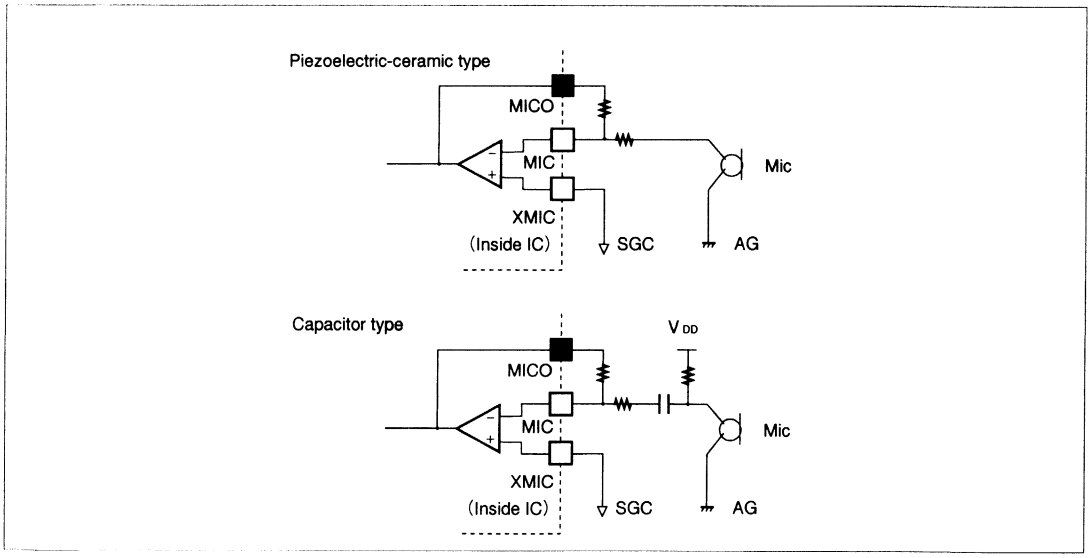


Table Microphone Amp Characteristics

Parameter	Characteristics (typ)
Gain measurement range	0 to 35 dB
Minimum load level	50 kΩ
Maximum output level	0.75 V_{OP}

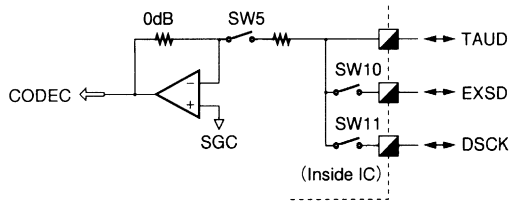
(2) Accessory Input

Direct input from the TAUD to the codec unit is possible through SW5, without passing through the microphone amp. Care must be taken with the input signal in this case, however, because input resistance is not at high-impedance level.

Microphone amp output may be added to the signal by using switching controls.

In this case, the result will be at the additional output level.

In addition, SW10 and SW11 may be used to transmit digital data from the TAUD to EXSD and DSCK, allowing the sending of fax or PC data without modification.



Note: TAUD, EXSD, and DSCK contain no digital buffers. If not used, TAUD, EXSD and DSCK should be connected to SGC.

3. Analog Output

The MB86435 has a total of four analog output circuits, including the three speaker drive circuits (receiver, earphone and tone) and the accessory output.

(1) Speaker Drive Amp

The speaker drive amps include two circuits (receiver and tone) with BTL output and one system (earphone) with single output. Because the speaker amp requires relatively high levels of power, it is connected to speaker selection switches (sw6-sw9) for power-down mode selection.

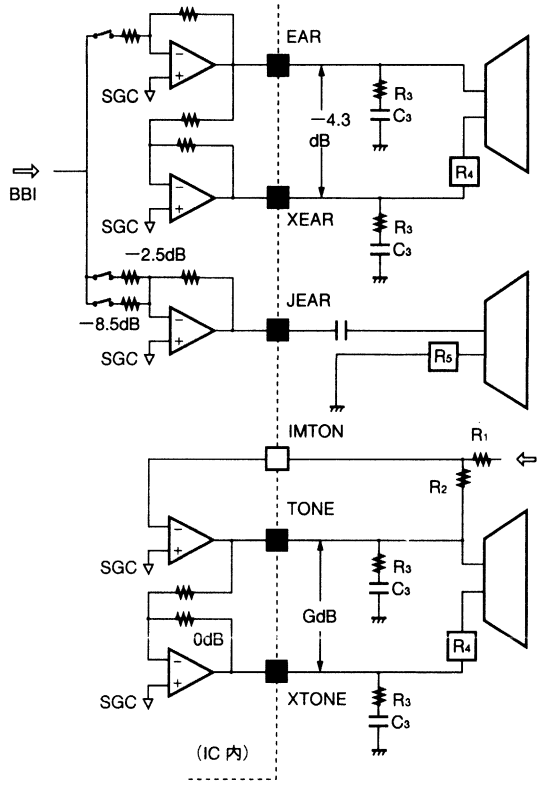
Two systems (receiver and earphone) have fixed gain levels, while the other system (tone) allows gain adjustment by means of external resistors.

Table Speaker Drive Amp Output Standards

Parameter	Receiver speaker amps (EAR, XEAR)	Earphone speaker amp (JEAR)	Tone speaker amps (TONE, XTONE)
Output type	BTL	Single	BTL
Load resistance *1	32 Ω (typ)	32 Ω (typ)	25 Ω (typ)
Load resistance *2	2.8 kΩ (typ)	2.8 kΩ (typ)	2.8 kΩ (typ)
Load capacity *2	70 nF	70 nF	70 nF
Final stage gain	−4.3 dB (between EAR-XEAR)	−2.5 dB/−8.5 dB (JEAR)	−5 to 20 dB (between TONE-XTONE)
Maximum output power	6.4 mW (min)	2 mW (min)	10 mW (min)

*1: Dynamic-type speaker
*2: Piezoelectric-ceramic type speaker

• Analog Output Connection Example



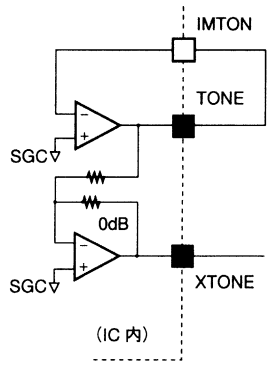
Receiver speaker
Dynamic type: 32 Ω (typ)
Piezoelectric-ceramic type: 70 nF, 2.8 kΩ (typ)

Earphone speaker
Dynamic type: 32 Ω (typ)
Piezoelectric-ceramic type: 70 nF, 2.8 kΩ (typ)

Tone speaker
Dynamic type: 32 Ω (typ)
Piezoelectric-ceramic type: 70 nF, 2.8 kΩ (typ)
$G=20 \log (2 * R_2/R_1)$ [dB]

Note: • R_3, C_3 should be given the respective values 80Ω, 0.01 μF in order to prevent unwanted oscillation.
• If a piezoelectric-ceramic type microphone is used, R_4, R_5 should be given the respective values 20Ω, 10Ω in order to prevent unwanted oscillation.

• Tone Speaker Amp Not Used



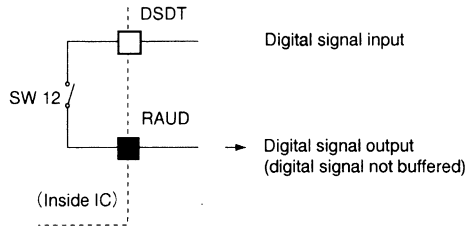
Note: When no tone speaker amp is used, the amp input IMTON and output TONE should be shorted together.

(2) Accessory Output

The accessory output (RAUD pin) can carry either digital or analog output signals, and is controlled by address 0101 data bit D_4 (SW 8), and address 0111 data bit D_1 (SW 12).

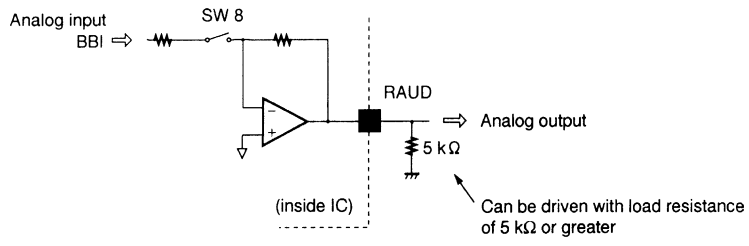
When both SW 8 and SW 12 are in off position, the accessory outputline is in H-Z (high impedance) state. Caution: never place both SW 8 and SW 12 in on position at the same time. This may cause the MB86435 to function improperly.

• SW12 in On Position



Address				Data bit				
A_3	A_2	A_2	A_1	D_4	D_3	D_2	D_1	D_0
0	1	1	1	—	—	—	1	—

• SW8 in On Position

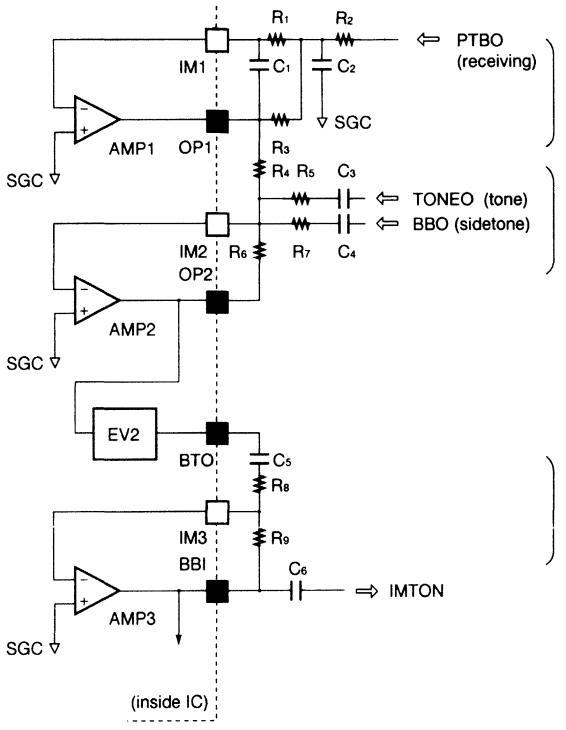


Address				Data bit				
A_3	A_2	A_2	A_1	D_4	D_3	D_2	D_1	D_0
0	1	0	0	0	*	*	*	—
0	1	0	1	0	*	—	—	—

4. Receiver Connections

It is possible to add tones and adjust sidetones by using amp 1,2 and 3 and the electronic volume control. When using amp 3, however, it is necessary to include HPF to avoid interference from the speaker amp DC.

• Tone and Sidetone Addition by Inclusion of Secondary LPF and Primary HPF.



Secondary LPF

$A = -R_2/R_3$

$\omega/Q = 1/C_2 * (1/R_1 + 1/R_2 + 1/R_3)$

$\omega^2 = 1/(R_1 R_3 C_1 C_2)$

Signal addition

$R_4 = R_5 = R_6 = R_7 = 100\ k\Omega$

$C_3 = C_4 = 0.1\ \mu F$

Primary HPF

$A = -R_9/R_8$

$f_c = 1/(2\pi C_5 R_8)$

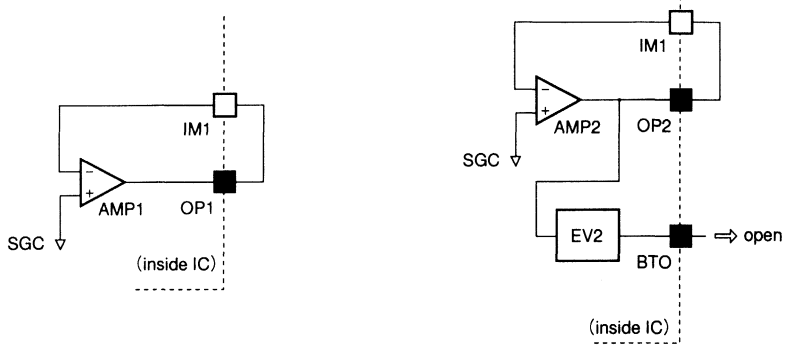
$C_6 = 0.1\ \mu F$

The following settings are necessary to comply with CCITT Recommendation

$R_8 = R_9 = 100\ k\Omega$

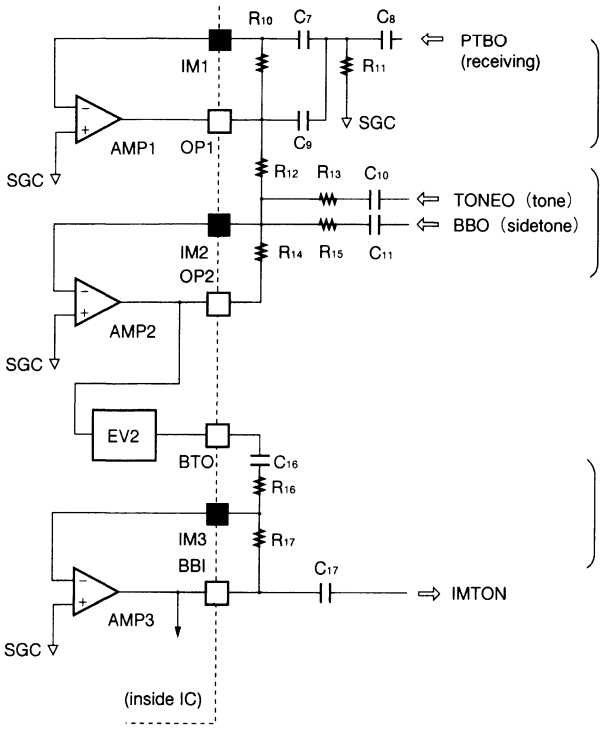
$C_5 = 0.039\ \mu F$

• Amp1, Amp2 not used



Note: When amps are not used, the amp input and output should be shorted together.

• **Tone and Sidetone Addition by Inclusion of Third-Order HPF**



Secondary HPF

$A = -C_8/C_9$

$\omega/Q = 1/(R_{10} C_9 C_7) * (C_7 + C_8 + C_9)$

$\omega^2 = 1/(R_{10} R_{11} C_9 C_7)$

Signal addition

$R_{12} = R_{13} = R_{14} = R_{15} = 100\ k\Omega$

$C_{10} = C_{11} = 0.1\ \mu F$

Primary HPF

$A = -R_9/R_8$

$f_c = 1/(2\pi C_{16} R_8)$

$C_{17} = 0.1\ \mu F$

5. Power Saving Modes

(1) Mode Selection

The MB86435 power saving modes can be controlled by using the external control signal lines (3 lines). It is also possible to apply power saving modes to the speaker amps with high power consumption levels by writing changes to register settings. Whenever the MB86435 changes directly from a power-down mode to normal operating mode, there is a possibility that speaker tones may be produced. The recommended sequence of coding changes to go into normal mode is (VREF mode) → (Tone mode) → (Normal mode).

Power Saving Modes

Mode	External pins			Address 0100		Address 0101	Address 0110			Output pin status												Operating circuit status									Power supply current (mA) (typ)
	PS C2	PS C1	PS C0	D4	D0	D	D	D	D	EAR XEAR	JEAR	TONE XTONE	RAUD	DOUT	SGC SGO	OP2 BTO	PTBO BTPO	OP1	MICO JMICO BBO VRH	BBI	CODEC	VREF generator	TONE generator	Sending	Receiving	Receiver	Earphone	Tone	Accessory	
						SW8	SW7	SW9	SW6	SW6	SW7	SW9	SW8													SW6	SW7	SW9	SW8	
All power-down	0	0	0	—	—	—	—	—	—	ZA	H-Z	ZB	H-Z	H	H-Z	ZC	H-Z	H-Z	H-Z	*	×	×	×	×	×	×	×	×	×	0.0005
VREF	1	0	0	—	—	—	—	—	—	ZA	H-Z	ZB	H-Z	H	○	ZC	H-Z	H-Z	H-Z	*	×	○	×	×	×	×	×	×	×	0.41
Tone	—	1	0	1	1	—	—	—	—	ZA	H-Z	ZB	H-Z	H	○	○	H-Z	H-Z	H-Z	○	×	○	○	×	○	×	×	×	×	1.8
	—	1	0	0	1	0	1	1	1	ZA	H-Z	ZB	○	H	○	○	H-Z	H-Z	H-Z	○	×	○	○	×	○	×	×	×	○	2.4
	—	1	0	0	1	1	0	1	1	ZA	○	ZB	H-Z	H	○	○	H-Z	H-Z	H-Z	○	×	○	○	×	○	×	○	×	×	4.4
	—	1	0	0	1	1	1	0	1	ZA	H-Z	○	H-Z	H	○	○	H-Z	H-Z	H-Z	○	×	○	○	×	○	×	×	○	×	6.6
	—	1	0	0	1	1	1	1	0	○	H-Z	ZB	H-Z	H	○	○	H-Z	H-Z	H-Z	○	×	○	○	×	○	○	×	×	×	6.6
Normal	—	—	1	0	0	0	1	1	1	ZA	H-Z	ZB	○	○	○	○	○	○	○	○	○	○	○	○	○	×	×	×	○	6.0
	—	—	1	0	0	1	0	1	1	ZA	○	ZB	H-Z	○	○	○	○	○	○	○	○	○	○	○	○	×	○	×	×	8.0
	—	—	1	0	0	1	1	0	1	ZA	H-Z	○	H-Z	○	○	○	○	○	○	○	○	○	○	○	○	×	×	○	×	10.2
	—	—	1	0	0	1	1	1	0	○	H-Z	ZB	H-Z	○	○	○	○	○	○	○	○	○	○	○	○	○	×	×	×	10.2
	—	—	1	0	0	0	0	0	0	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	18.2

Note: • ○: Operational, ×: Power-down, H-Z: High impedance, H: H-level fixed

*: High impedance may not be applied, depending on status of SW6, SW7, SW8.

ZA: EAR and XEAR are floating, however high resistance connection between EAR and XEAR.

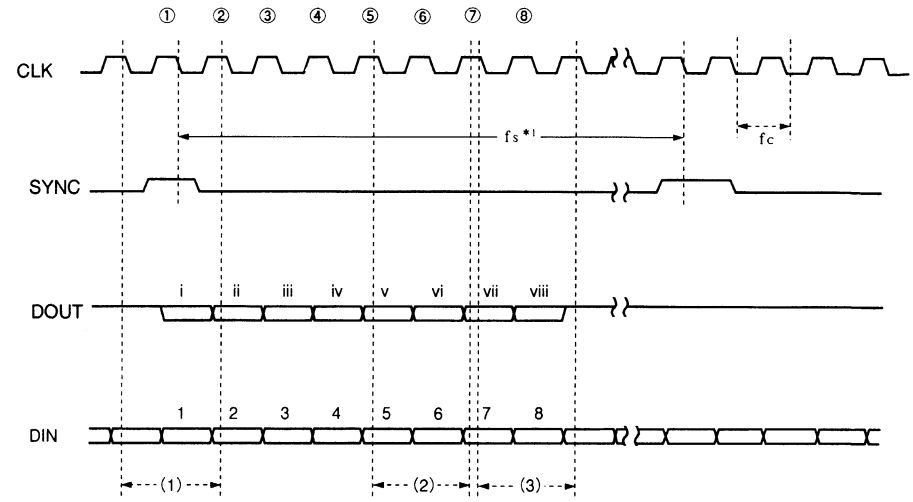
ZB: TONE and XTONE are floating, however, high resistance connection between TONE and XTONE, and between SGO and XTONE.

ZC: Floating, however high resistance connection between OP2 and BTO. Codec in [Normal] mode operates with SYNC = 8 kHz, CLK = 2048 kHz.

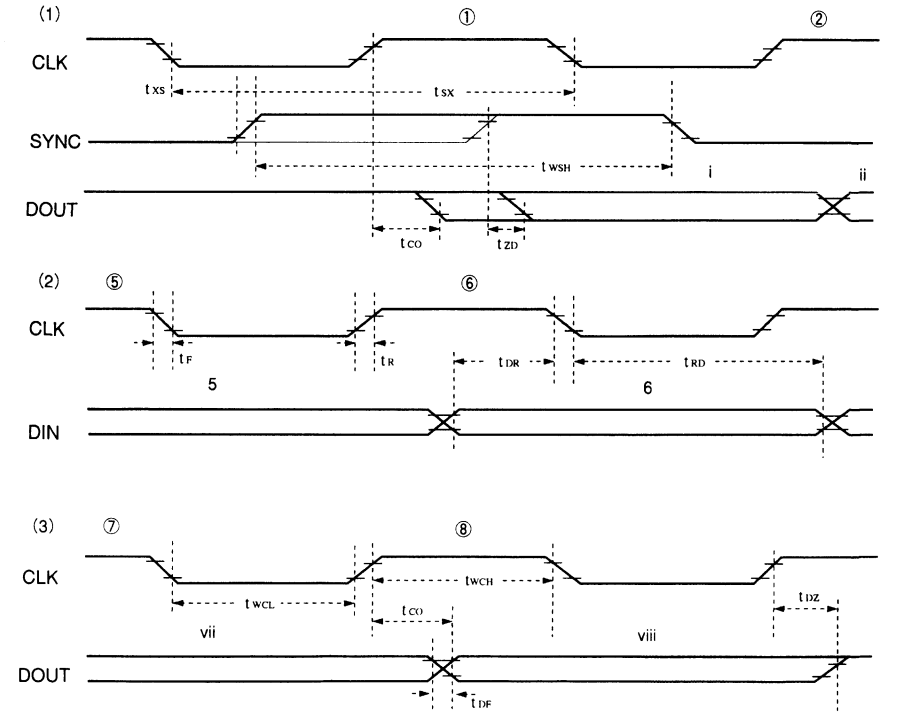
- When RAUD is operating, address 0111 data bit D1 value should be "0" (SW12 off).
- In tone mode, address 0111 data bit D3 should be "0" (SW2 on), and address 0111 data bit D4 should be "0" (SW14 off).
- When the SYNC and CLK pin signals are fixed at either L-level or H-level, part of the codec unit will go into power-down mode. At this time the PTBO signal will be SGC level, BTPO will be H-Z, and VRH output will be approximately 4.0 V.

■ TIMING CHART

• Codec-Related Signals

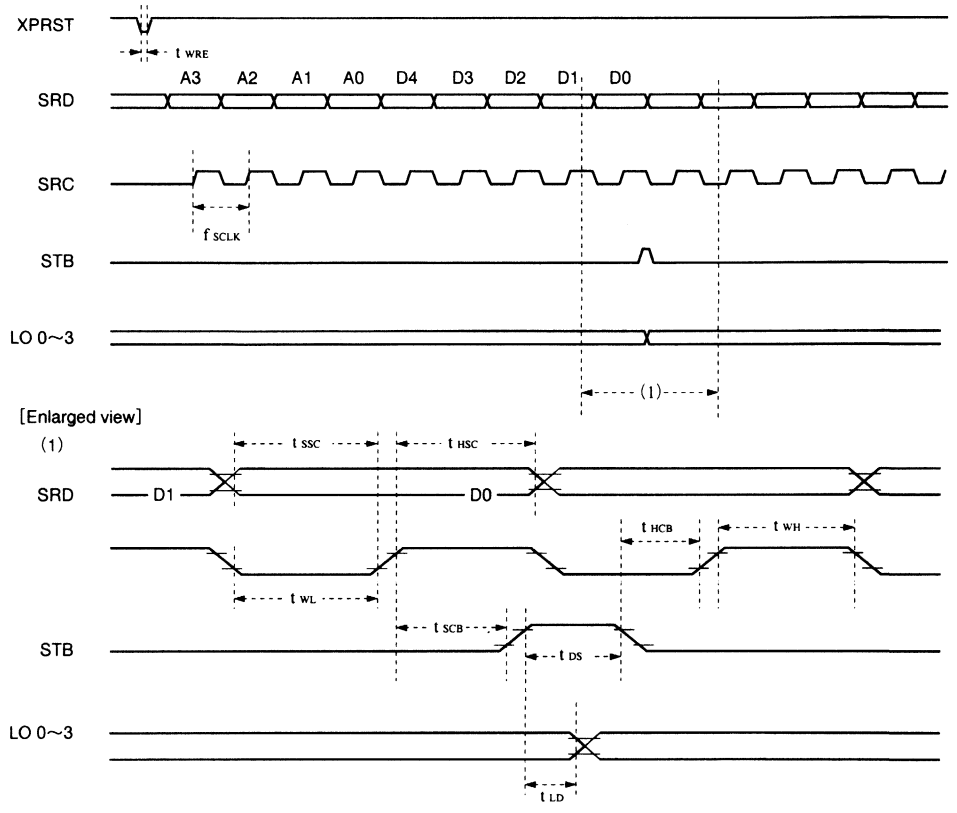


[Enlarged view]



*1 From first CLK Down to second CLK Down, SYNC = H.

• Microcomputer Data-Related Signals



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min.	Max.	
Power supply voltage	V_S	− 0.3	7.0	V
Analog input voltage	V_{AIN}	− 0.3	+V_S + 0.3	V
Digital input voltage	V_{DIN}	− 0.3	+V_S + 0.3	V
Storage temperature	Vstg	− 55	+ 125	°C

Note: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Pin name	Value			Unit
			Min.	Typ.	Max.	
Operating temperature	Ta	—	−20	+25	+80	℃
Power supply voltage	V_S	VDD, VDDAB, VDDAC, VDDSP 1, VDDSP2	2.7	3.0	3.6	V
Digital input voltage	V_L	All digital input pins	0.0	—	V_S	V
Analog output load resistance	R_{LB}	BBO, PTBO, TONEO, BTO, BTPO	75	—	—	kΩ
Analog output load capacity	C_{LB}		—	—	20	pF
Analog output load resistance*1	R_{LE}	Between EAR-XEAR	—	32	—	Ω
Analog output load capacity*2	C_{LE}		—	—	70	nF
Analog output load resistance*1	R_{LJ}	JEAR	—	32	—	Ω
Analog output load capacity*2	C_{LJ}		—	—	70	nF
Analog output load resistance*1	R_{LT}	Between TONE-XTONE	—	25	—	Ω
Analog output load capacity*2	C_{LT}		—	—	70	nF
Analog output load resistance	R_{LM}	MICO, JMICO, SGO, BBI, OP1, OP2	50	—	—	kΩ
Analog output load capacity	C_{LM}		—	—	20	pF
Analog output load resistance*3	R_{LM}	RAUD	5	—	—	kΩ
Analog output load capacity*3	C_{LM}		—	—	20	pF
Analog output voltage	V_{AOUT}	All analog output pins	0.45	—	V_{DD}−0.45	V
Analog input voltage	V_{AIN}	All analog input pins	1.2	—	1.8	V

*1: Dynamic typ speakers
*2: Piezoelectric type speakers
*3: When SW8 = on, SW12 = off

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

Parameter		Symbol	Pin	Conditions	Value			Unit
					Min.	Typ.	Max.	
Power supply current at full power-down mode		I_{VSST1}	All V_{DD} pins	PSC0 = 0 : PSC1 = 0 : PSC2 = 0, Ain = AG, Din = L	—	0.5	50	μA
Power supply current with VREF operating		I_{VSST2}		PSC0 = 0 : PSC1 = 0 : PSC2 = 1, Ain = SGC, Din = L	—	410	800	μA
Power supply current with TONE operating		I_{VSST3}		PSC0 = 0 : PSC1 = 1, Ain = SGC, Din = ICN SW6 = SW7 = SW8 = SW9 = off	—	1.8	3.0	mA
Power supply current for normal operation (only speaker ampmute)		I_{VSST4}		PSC0 = 1, Ain = SGC, Din = ICN SW6 = SW7 = SW9 = off	—	6.0	8.5	mA
Speaker amp power supply voltage	Receiver amps EAR, XEAR	I_{VSST5}		PSC0 = 0, PSC1 = 1, Ain = SGC, Din = ICN, Power supply current differential when SW6 is on/off.	—	4.8	7.0	mA
	Earphone amp JEAR	I_{VSST6}		PSC0 = 0, PSC1 = 1, Ain = SGC, Din = ICN, Power supply current differential when SW7 is on/off.	—	2.6	4.0	mA
	Tone amps TONE, XTONE	I_{VSST8}		PSC0 = 0, PSC1 = 1, Ain = SGC, Din = ICN, Power supply current differential when SW9 is on/off.	—	4.8	7.0	mA
Digital input voltage		V_{IH}	All digital input pins	—	Vs*0.7	—	Vs	V
		V_{IL}		—	0	—	Vs*0.3	V
Digital input current		I_{IH}		—	—	—	10	μA
		I_{IL}		—	—	—	10	μA
Input offset voltage		V_{FM}	Between MIC-XMIC, between JMIC-XJMIC	—	−10	—	10	mA
Output offset voltage		V_{FR}	RAUD	BBI = SGC SW8 = on, SW6 = SW7 = SW9 = SW12 = off	−15	—	15	mV
		V_{FE}	Between EAR-XEAR	BBI = SGC SW6 = on, SW7 = SW8 = SW9 = SW12 = off	−20	—	20	mV
		V_{FT}	Between TONE-XTONE	IMTON = SGC SW9 = on, SW6 = SW7 = SW8 = SW12 = off	−20	—	20	mV
		V_{FP}	PTBO	Din = ICN, EV2 = 0 dB	−100	—	100	mV
		V_{OH}	Between MIC0-BBO	EV0 = 0 dB	−100	—	100	mV
		V_{OL}	Between JMIC0-BBO					

(Continued)

(Continued)

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min.	Typ.	Max.	
SGC output voltage	V_{SGC}	SGC	—	1.40	1.50	1.60	V
SGO output voltage	V_{SGO}	SGO	—	1.40	1.50	1.60	V
VRH output voltage	I_{VRH}	VRH	—	—	2.5	—	V
Digital output voltage	V_{OH}	All digital output pins	I_{OH} = – 0.5 mA	V_S * 0.8	—	V_S	V
Digital output voltage	V_{OL}	All digital output pins	I_{OL} = 0.5 mA	0.0	—	V_S * 0.2	V
Resistance between pins TAUD and DSCK	R_{DR}	Between DSTD-RAUD	SW12 = on, SW8 = off	—	—	2	kΩ
Resistance between pins TAUD and EXSD	R_{TE}	Between TAUD-EXSD	SW10 = on, SW11 = off	—	—	2	kΩ
Resistance between pins DSTD and RAUD	R_{DE}	Between TAUD-DSCK	SW11 = on, SW10 = off	—	—	2	kΩ

Note: Measurement conditions: ■ Standard Test Circuit

2. AC Characteristics

(1) Codec-Related Signals

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Digital input rise time	t_R	Vs∗0.3→Vs∗0.7	—	—	50	ns
Digital input fall time	t_F		—	—	50	ns
Shift clock frequency	f_C	μ-law, A-law	64	—	3152	kHz
		Linear	256	—	3152	kHz
Shift clock pulse width (H)	t_{WCH}	V_{IH}=Vs∗0.7	1/fc∗0.3	—	1/fc∗0.7	ns
Shift clock pulse width (L)	t_{WCL}	V_{IL}=Vs∗−0.3	1/fc∗0.3	—	1/fc∗0.3	ns
Sync frequency	f_S	—	—	8	—	kHz
Sync pulse width	t_{WSH}	—	1/fc	—	62	μs
SYNC to CLK setup time	t_{SX}	—	100	—	—	ns
CLK to SYNC hold time	t_{XS}	—	50	—	—	ns
CLK to DIN hold time	t_{RD}	—	50	—	—	ns
DIN to CLK setup time	t_{DR}	—	50	—	—	ns
SYNC to DOUT delay time	t_{ZD}	BIT 1	—	—	200	ns
CLK to DOUT delay time	t_{CO}	BIT 2 to 8	—	—	200	ns
CLK to DOUT disable time	t_{DZ}	"H"	—	—	200	ns
DOUT fall time	t_{DF}	—	10	—	100	ns

(2) Microcomputer Data-Related Signals

Parameter	Symbol	Pin	Value			Unit
			Min.	Typ.	Max.	
SRC to SRD data setup time	t_{SSC}	SRD, SRC	50	—	—	ns
SRC to SRD data hold time	t_{HSC}		50	—	—	ns
SRC to STB setup time	t_{SCB}	SRC, STB50	—	—	ns	
SRC pulse width (H)	t_{WH}	SRC	200	—	—	ns
SRC pulse width (L)	t_{WL}		200	—	—	ns
STB pulse width	t_{DS}	STB	50	—	—	ns
STB to SRC hold time	t_{HCB}	STB, SRC50	—	—	ns	
LO0 to 3 delay time	t_{LD}	LO0 to 3	—	—	200	ns
Shift clock frequency	f_{SCLK}	SRC	—	—	2048	kHz
Reset pulse width	t_{WRE}	XPRST	1	—	—	μs

3. Transmission Characteristics

(1) Microphone Amp System

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Gain (between MIC0 and BBO)	G_{MB}	MICO=−20 dBv, 1020 Hz SW3=on, SW4=SW5=SW14=off EV 0=0 dB	−1.5	—	1.5	dB
Gain (between JMIC0 and BBO)	G_{JB}	JMICO=−20 dB V, 1020 Hz SW4=on, SW3=SW5=SW14=off EV 0=0 dB	−1.5	—	1.5	dB
Signal to noise ratio (between MIC and BBO) (between XMIC and BBO)	S_{MB}	Ain1=−40 dBv (+20 dBgain) SW3=on, SW4=SW5=SW14=off EV0=0 dB, 1020 Hz C message	40	—	—	dB
Signal to noise ratio (between JMIC and BBO) (between XJMIC and BBO)	S_{JB}	Ain2=−40 dBv (+20 dBgain) SW4=on, SW3=SW5=SW14=off EV0=0 dB, 1020 Hz C message	40	—	—	dB

Note: Measurement conditions: ■ Standard Test Circuit

(2) Speaker Amp System

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Gain (between EAR and XEAR)	G_{BE}	BBI=−20 dBv, 1020 Hz	—	−4.3	—	dB
Gain (between BBI and JEAR)	G_{BJ}	BBI=−20 dBv, 1020 Hz, ATT=−2.5 dB	—	−2.5	—	dB
	G_{BJ6}	BBI=−20 dBv, 1020 Hz, ATT=−8.5 dB	—	−8.5	—	dB
Gain (between BBI and RAUD)	G_{BR}	BBI=−20 dBv, 1020 Hz SW8=on, SW6=SW7=SW12=off	—	0.0	—	dB
Output power	W_E	R=32Ω, between EAR-XEAR THD=10%	6.4	—	—	mW
	W_T	R=25Ω, between TONE-XTONE gain=0 dB, THD=10%	10.0	—	—	mW
	W_J	R=32Ω, JEAR, ATT=−2.5 dB THD=10%	2.0	—	—	mW

Note: Measurement conditions: ■ Standard Test Circuit

(3) TONE System

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
TONE output level (TONE0)	G_{T1}	1 tone generated, SW2=on f_1=948.1 kHz	—	−14.0	—	dBv
	G_{T2}	2 tone generated, SW2=on f_1=948.1 kHz, f_2=1219.1 kHz	—	−14.0	—	dBv

Note: Measurement conditions: ■ Standard Test Circuit

(4) Electric Volume System

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Volume gain error EV0 (between TAUD-BBO)	G_{E0}	SW5=on, SW3=SW4=SW14=off TAUD=−20 dBv, 1020 Hz	−0.7	—	0.7	dB
Volume gain error EV1 (between DIN-PTBO)	G_{E1}	D_{IN}=−20 dBm0, 1020 Hz	−0.8	—	0.8	dB
Volume gain error EV2 (between IM 2-BTO)	G_{E2}	IM2=−20 dBv, 1020 Hz	−1.0	—	1.0	dB
Volume gain error EV3 (TONEO)	G_{E3}	SW2=on 1 tone generated f 1=948.1kHz	−0.5	—	0.5	dB

Note: Measurement conditions: ■ Standard test circuit

(5) Sending/Receiving System (Codec, Analog Block)

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Crosstalk (send→receive)	CTX	Ain1=1020 Hz, −40 dBv (20 dBgain) D_{IN}=ICN Measured at RAUD pin	—	—	−50	dB
Crosstalk (send→receive)	CTR	D_{IN}=1020 Hz, 0 dBm0 A_{IN}=SGC Measured at DOUT pin	—	—	−50	dB
Power supply noise reduction ratio	PSRR	0<f<50 kHz, V_{DD}+30 mV$_{OP}$ C message A_{IN}=SGC, D_{IN}=ICN	—	22	—	dB

Note: Measurement conditions: ■ Standard test circuit

(6) Codec

Parameter	Symbol	Conditions		Value Min.	Value Typ.	Value Max	Unit
Gain tracking (A to D) BTPO→DOUT	GTX	1020 Hz, −10 dBm0 Reference value	+3 to −40 dBm0	−0.2	—	0.2	dB
			−40 to −50 dBm0	−0.4	—	0.4	dB
			−50 to −55 dBm0	−0.8	—	0.8	dB
Gain tracking (D to A) DIN→PTBO	GTR	1020 Hz, −10 dBm0 Reference value EV1=0 dB	+3 to −40 dBm0	−0.4	—	0.4	dB
			−40 to −50 dBm0	−0.6	—	0.6	dB
			−50 to −55 dBm0	−1.0	—	1.0	dB
Gain tracking (A to D) (Linear) BTPO→DOUT	GTXL	1020 Hz, AFST−3 dB Reference value	AFST to AFST−43 dB	−0.2	—	0.2	dB
			AFST−43 to AFST−53 dB	−0.4	—	0.4	dB
			AFST−53 to AFST−53 dB	−0.8	—	0.8	dB
Gain tracking (D to A) (Linear) DIN→PTBO	GTRL	1020 Hz, AFSR−3 dB Reference value EV1=0 dB	AFSR to AFSR−43 dB	−0.4	—	0.4	dB
			AFSR−43 to AFSR−53 dB	−0.6	—	0.6	dB
			AFSR−53 to AFSR−53 dB	−1.0	—	1.0	dB
Sending frequency characteristics (A to D) BTPO→DOUT	FRX	0 dBm0 (Linear : AFST−3 dB) 1020 Hz Reference value	0 to 60 Hz	24.0	—	—	dB
			60 to 300 Hz	−0.20	—	—	dB
			300 to 3000 Hz	−0.20	—	0.20	dB
			3000 to 3400 Hz	−0.20	—	0.8	dB
			3400 to 4600 Hz	*	—	—	dB
			4600 to 12 kHz	32.0	—	—	dB
Receiving frequency characteristics (D to A) DIN→PTBO	FRR	0 dBm0 (Linear : AFSR−3 dB) 1020 Hz Reference value EV1=0 dB	0 to 300 Hz	−0.30	—	—	dB
			300 to 3000 Hz	−0.30	—	0.30	dB
			3000 to 3400 Hz	−0.30	—	1.10	dB
			3400 to 4600 Hz	*	—	—	dB
			4600 to 12 kHz	32.0	—	—	dB
Sending absolute gain (A to D) BTPO→DOUT	GAX	1020 Hz, 0 dBm0 (Linear : AFST−3 dB) EV1=0 dB, Vs=3.0 V, Ta=+25°C		−1.0	0	−1.0	dB
		Power supply variation		—	±0.02	—	dB
		Temperature variation		—	±0.001	—	dB/°C
Receiving absolute gain (D to A) DIN→PTBO	GAR	1020 Hz, 0 dBm0 (Linear : AFSR−3 dB) Vs=3.0 V, Ta=+25°C		−1.20	0	1.20	dB
		Power supply variation		—	±0.04	—	dB
		Temperature variation		—	±0.002	—	dB/°C
Absolute level	VABS	Over load level μ-Law=3.17 dB A-Law=3.14 dB		—	0.7647	—	V_{OP}

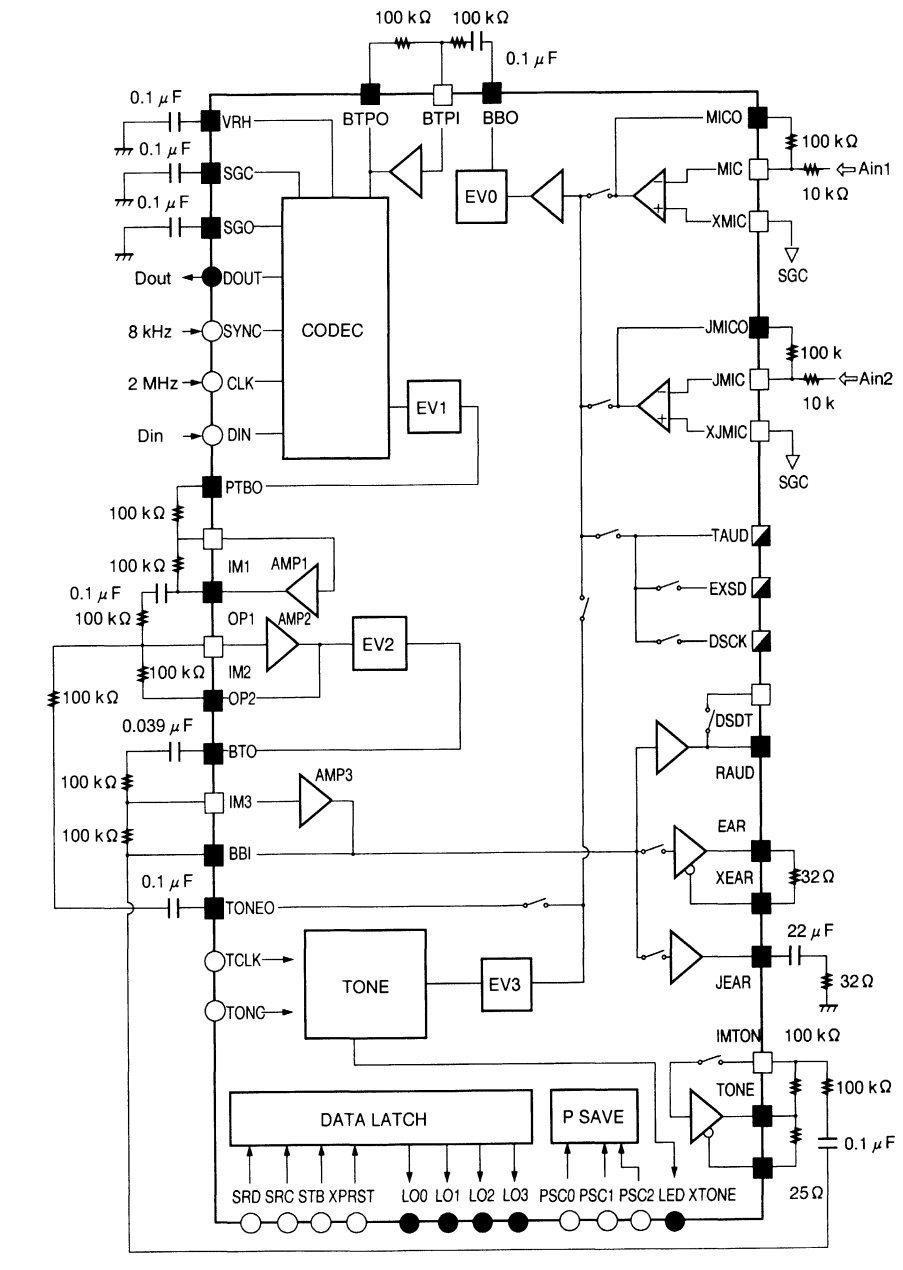
(Continued)

(Continued)

Parameter	Symbol	Conditions		Value Min.	Value Typ.	Value Max	Unit
Sending signal to noise ratio BTPO→DOUT	SDX	1020 Hz C message (A to D)	0 to −30 dBm0	34.0	—	—	dB
			−40 dBm0	28.0	—	—	dB
			−45 dBm0	23.0	—	—	dB
Receiving signal to noise ratio DIN→DOUT	SDR	1020 Hz C message (D to A)	0 to −30 dBm0	34.0	—	—	dB
			−40 dBm0	28.0	—	—	dB
			−45 dBm0	23.0	—	—	dB
Sending signal to noise ratio BTPO→DOUT (Linear)	SDXL	1020 Hz C message (A to D)	AFST−3 to AFST−33 dB	34.0	—	—	dB
			AFST−43 dB	28.0	—	—	dB
			AFST−45 dB	23.0	—	—	dB
Receiving signal to noise ratio BTPO→DOUT (Linear)	SDRL	1020 Hz C message (D to A)	AFSR−3 to AFSR−33 dB	34.0	—	—	dB
			AFSR−43 dB	28.0	—	—	dB
			AFSR−45 dB	23.0	—	—	dB
Sending no-talk noise BTPO→DOUT	ICNX	C message (A to D)		—	−72	−68	dBm0C
Receiving no-talk noise DIN→PTBO	ICNR	C message (D to A)		—	−72	−68	dBm0C
Analog input level BTPO	AILU	1020 Hz, 0 dBm0, Ta=+25℃ Vs=3.0 V μ-law		0.3290	0.3739	0.4195	Vrms
Analog output level PTBO	AOLU	1020 Hz, 0 dBm0, Ta=+25℃ Vs=3.0 V μ-law		0.3290	0.3739	0.4195	Vrms
Analog input level BTPO	AILA	1020 Hz, 0 dBm0, Ta=+25℃ Vs=3.0 V A-law		0.3315	0.3767	0.4227	Vrms
Analog output level PTBO	AOLA	1020 Hz, 0 dBm0, Ta=+25℃ Vs=3.0 V A-law		0..3315	0.3767	0.4227	Vrms
Analog input fullscale level BTPO	AFST	Vs=3.0 V, Ta=+25℃ Linear		0.6729	0.7647	0.8581	V_{OP}
Analog output fullscale level PTBO	AFSR	Vs=3.0 V, Ta=+25℃ Linear		0.6729	0.7647	0.8581	V_{OP}
Overall absolute delay (BTPO→PTBO)	PDA	Fc ≥ 1544 kHz (DOUT-DiN short)		—	490	550	μs
Single frequency noise (BTPO→PTBO)	SFNA	BTPO=SCG (DOUT-DIN short)	0-4 kHz 4.6-200 kHz	—	—	−70 −50	dBm0 dBm0
Discrimination (BTPO→PTBO)	DISA	BTPO=0 dBmO, 4.6-200 kHz (DOUT-DIN short)		30	—	—	dB
In-band spurious response (BTPO→PTBO)	IBSA	Second and third harmonic, BTPO=0 dBmO 700-1100 Hz (DOUT-DIN short)		43	—	—	dB

∗ : $14.5\times\left\{1-\mathrm{SIN}\frac{\pi\ (4000-f)}{1200}\right\}$

■ STANDARD TEST CIRCUIT



○ : Digital input ● : Digital output □ : Analog input ■ : Analog output ◪ : Input/output ▲ : V_{DD} △ : GND

Note: Sufficient path capacitance must be placed between VDDAB–BAG, VDDAC–CAG, VDDSP1–SPG1, VDDSP2–SPG2, VDD–AG.

■ ORDERING INFORMATION

Part number	Package	Remarks
MB86435PFV	64 pins, Plastic SQFP (FPT-64P-M03)	

MEMO

FUJITSU SEMICONDUCTOR
DATA SHEET

DS04–23501–4E

ASSP

ANALOG PROCESSOR LSI

MB87085

■ DESCRIPTION

The Fujitsu MB87085 is an audio processor LSI for cellular radio application, fabricated in Fujitsu Advanced CMOS Technology.

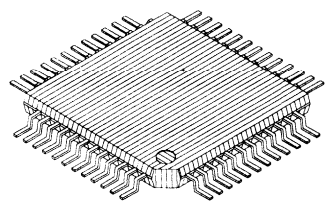
The MB87085 contains filter, electronic volume and limiter circuit.

The MB87085 is designed for AMPS (U.S.), TACS (U.K.) and NMT (Scandinavia) systems and is used with the Fujitsu MB87084 Analog Processor LSI.

■ FEATURES

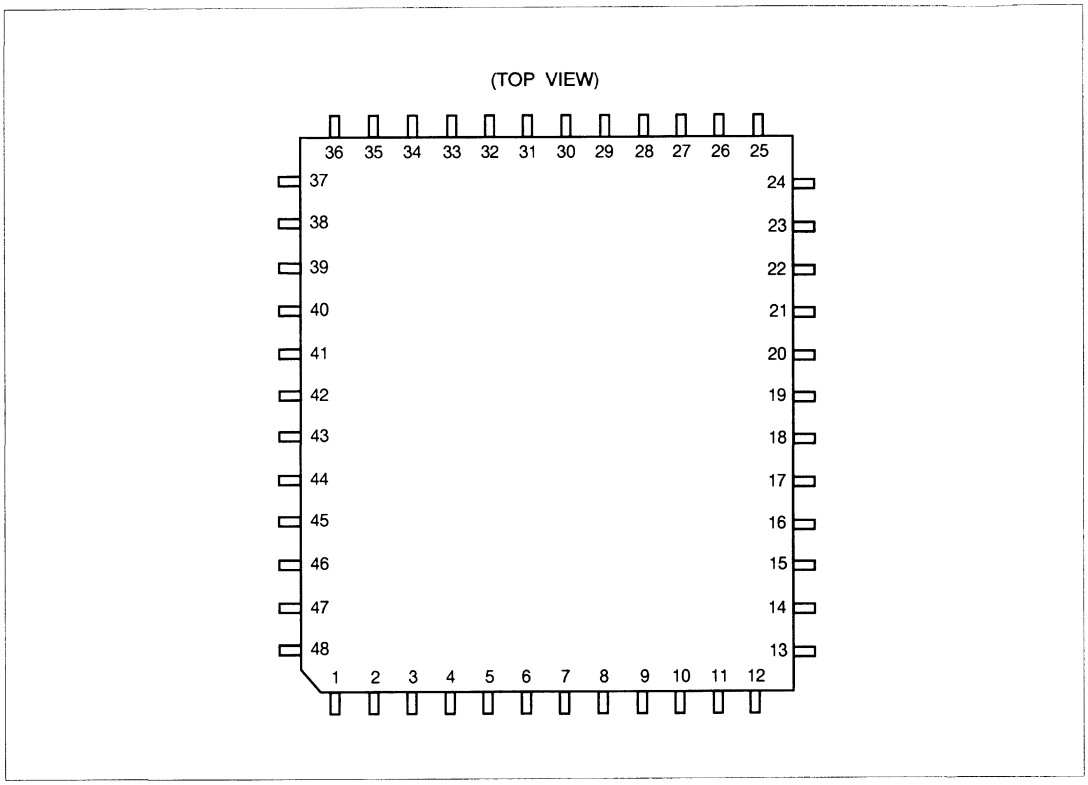
- AMPS, TACS or NMT mode is selected by select pin.
- Limiter circuit suppresses an instantaneous frequency deviation in FM modulation.
- Differential input structure prevents input noise of transmit section.
- Not required external parts of filter because filter consists of SCF is on chip. This enables stable performance.
- Electronic volume gain is digitally controlled for precision.
- Mute control of transmit/reception circuits are achieved respectively.
- Output pins for compressor and expander are provided.
- Power down mode is achieved by stand-by control function.
- Filter characteristics, electronic volume and stand-by mode are easily set by serial data input.
- I/O's are TTL compatible.

■ PACKAGE



PLASTIC PACKAGE
FPT-48P-M02

■ PIN ASSIGNMENT



■ PIN NAME TABLE

Pin No.	I/O	Pin Name	Pin No.	I/O	Pin Name	Pin No.	I/O	Pin Name
1	I	TAM	17	I	DEM	33	I	TVDD/2
2	I	BYPASS	18	O	MSK	34	—	N.C.
3	I	RAM	19	P	V_{DD}	35	I	COMP2
4	—	N.C.	20	O	AFOUT	36	—	N.C.
5	I	DATA	21	I	TONE	37	O	RT1
6	I	CLK	22	O	RR3	38	I	RT2
7	I	STB	23	I	RR2	39	O	RT3
8	I	$\overline{\text{RESET}}$	24	O	RR1	40	—	N.C.
9	I	CLOCK	25	I	EXP2	41	O	C1
10	P	DG	26	O	EXP1	42	I	C2
11	—	N.C.	27	O	RE3	43	P	V_{DD}
12	O	TVDD2	28	I	RE2	44	I	AFIN (–)
13	O	TREF	29	O	RE1	45	I	AFIN (+)
14	O	RREF	30	I	RVDD/2	46	—	N.C.
15	O	RVDD2	31	P	AG	47	O	MOD
16	—	N.C.	32	O	COMP1	48	I	AN

■ PIN DESCRIPTIONS

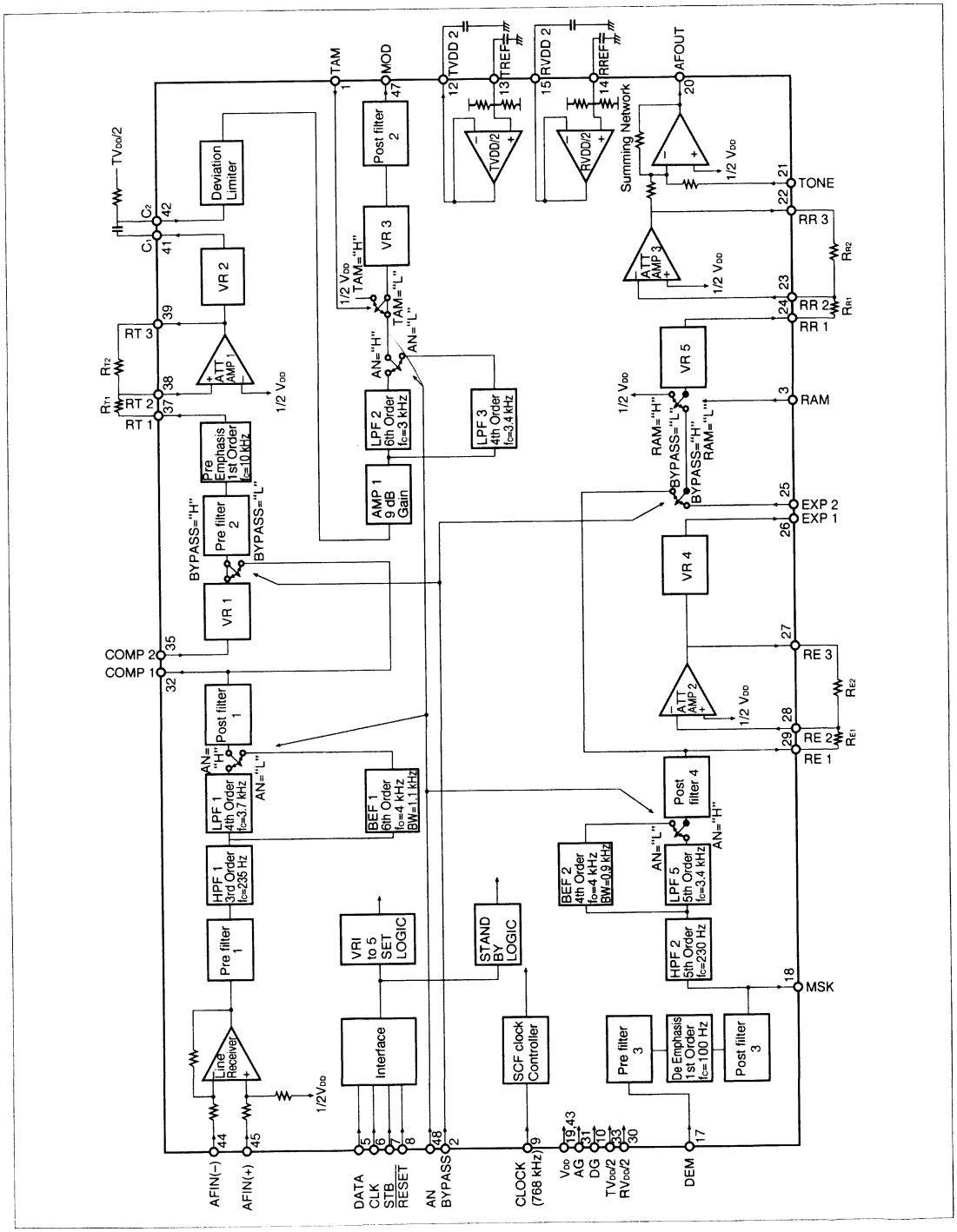
<table>
<tr><th>I/O</th><th>Pin No.</th><th>Pin Name</th><th>Descriptions</th></tr>
<tr><td rowspan="16">Input Pins</td><td>19, 43</td><td>V_{DD}</td><td>Power supply voltage input. (V_{DD} = 5 V ± 10%)</td></tr>
<tr><td>31</td><td>AG</td><td>Ground for analog circuit.</td></tr>
<tr><td>10</td><td>DG</td><td>Ground for digital circuit.</td></tr>
<tr><td>45</td><td>AFIN (+)</td><td>Differential input (+) to transmit section.</td></tr>
<tr><td>44</td><td>AFIN (–)</td><td>Differential input (–) to transmit section.</td></tr>
<tr><td>48</td><td>AN</td><td>Filter characteristics select input.
When low, NMT filter is selected.
When high, AMPS and TACS filter is selected.</td></tr>
<tr><td>2</td><td>BYPASS</td><td>Internal circuit bypass control signal input.
When low, transmit VR1 (external compressor) and reception VR4, ATTAMP2 (external expander) are bypassed.</td></tr>
<tr><td>1</td><td>TAM</td><td>Transmit mute control signal input.
When high, transmit filter output signal is muted.</td></tr>
<tr><td>3</td><td>RAM</td><td>Reception mute control signal input.
When high, reception filter output signal is muted.</td></tr>
<tr><td>5</td><td>DATA</td><td>The 25-bit of serial data input.</td></tr>
<tr><td>6</td><td>CLK</td><td>Clock input for 25-bit serial shift register.
On rising edge of CLK signal, one bit of serial data is shifted into the serial shift register.</td></tr>
<tr><td>7</td><td>STB</td><td>Strobe signal input.
On rising edge of STB signal, the data is stored in buffer register.</td></tr>
<tr><td>8</td><td>$\overline{\text{RESET}}$</td><td>Reset signal input.
When low, the data stored in the buffer register is reset as follows.
When high, stored data is kept.
<table>
<tr><th></th><th>S5</th><th>S4</th><th>S3</th><th>S2</th><th>S1</th><th>Gain</th><th>SB1</th><th>SB2</th></tr>
<tr><td>VR1, 4</td><td>—</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0 dB</td><td rowspan="3">"H"</td><td rowspan="3">"H"</td></tr>
<tr><td>VR2, 3</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0 dB</td></tr>
<tr><td>VR5</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0 dB</td></tr>
</table></td></tr>
<tr><td>9</td><td>CLOCK</td><td>Reference clock (768 kHz) input of switched capacitor filter (SCF).</td></tr>
<tr><td>17</td><td>DEM</td><td>Reception signal input. Input for pre filter 3.</td></tr>
<tr><td>35</td><td>COMP2</td><td>Signal input from an external compressor. When BYPASS pin is set low, this input signal is ignored.</td></tr>
<tr><td>25</td><td>EXP2</td><td>Signal input from an external expander. When BYPASS pin is set low, this input signal is ingored.</td></tr>
<tr><td>21</td><td>TONE</td><td>Reception adder input. After filtering an input signal from DEM pin, output the signal added with TONE signal to AFOUT pin.</td></tr>
</table>

(Continued)

(Continued)

I/O	Pin No.	Pin Name	Descriptions
Input Pins	42	C2	Limiter circuit input. After cutting DC level signal by a condenser placed between C1 and C2 pins is input.
	38	RT2	Transmit gain control signal input. External resistor RT1 and RT2 at pins RT1, RT2 and RT3 set the gain of ATTAMP1 (–15 dB to +5 dB) given by: Gain G = $-R_{T2}/R_{T1}$
	28	RE2	Reception gain control signal input. External resistor RE1 and RE2 at pins RE1, RE2 and RE3 set the gain of ATTAMP2 (0 dB to +20 dB) given by: Gain G = $-R_{E2}/R_{E1}$
	23	RR2	Reception gain control signal input. External resistor RR1 and RR2 at pins RR1, RR2 and RR3 set the gain of ATTAMP3 (–10 dB to +10 dB) given by: Gain G = $-R_{R2}/R_{R1}$
	33	TVDD/2	Transmit reference level (1/2 · V_{DD}) input. Please connect this pin and TVDD2 pin together externally. Transmit analog circuit operates referenced to this input level.
	30	RVDD/2	Reception reference level (1/2 · V_{DD}) input. Please connect this pin and RVDD2 pin together externally. Reception analog circuit operates referenced to this input level.
Output Pins	32	COMP1	Output for an external compressor.
	26	EXP1	Output for an external expander.
	18	MSK	Output of reception de emphasis circuit. After De Emphasising, an input signal from DEM pin is output.
	47	MOD	Output of transmit section.
	20	AFOUT	Output of reception section.
	37	RT1	Transmit gain control signal output. Transmit gain of ATTAMP1 (–15 dB to +5 dB) is controlled by external resistors. Gain G = $-R_{T2}/R_{T1}$
	39	RT3	Transmit gain control signal output. Transmit gain of ATTAMP1 (–15 dB to +5 dB) is controlled by external resistors. Gain G = $-R_{T2}/R_{T1}$
	29	RE1	Reception gain control signal output. Reception gain of ATTAMP2 (0 dB to +20 dB) is controlled by external resistors. Gain G = $-R_{E2}/R_{E1}$
	27	RE3	Reception gain control signal output. Reception gain of ATTAMP2 (0 dB to +20 dB) is controlled by external resistors. Gain G = $-R_{E2}/R_{E1}$
	24	RR1	Reception gain control signal output. Reception gain of ATTAMP3 (–10 dB to +10 dB) is controlled by external resistors. Gain G = $-R_{R2}/R_{R1}$
	22	RR3	Reception gain control signal output. Reception gain of ATTAMP3 (–10 dB to +10 dB) is controlled by external resistors. Gain G = $-R_{R2}/R_{R1}$
	41	C1	Output for DC level cutting. Please cut DC level by a capacitor connected between C1 and C2 pins.
	12	TVDD2	Reference voltage output for transmit section.
	13	TREF	REF output voltage pin.
	15	RVDD2	Reference voltage output for reception section.
	14	RREF	REF output voltage pin.

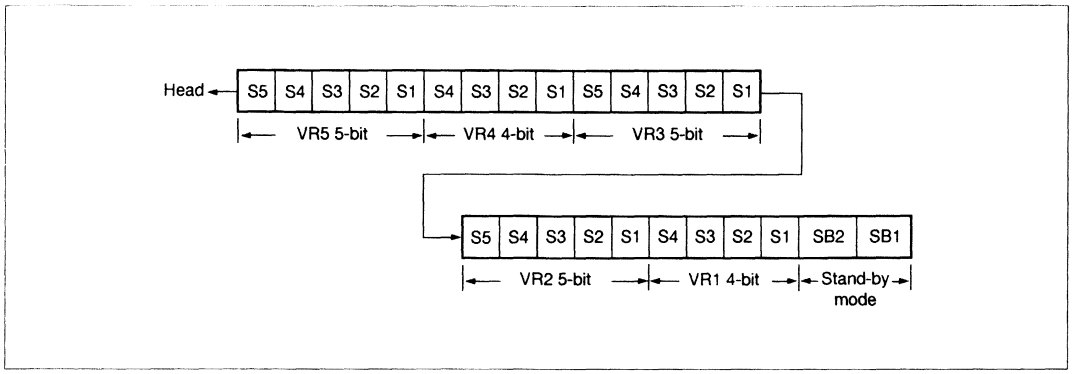
■ BLOCK DIAGRAM



■ FUNCTIONAL DESCRIPTIONS

1. Electronic Volume Gain Setting

Electronic volume gain and stand-by mode are set by 25-bit of serial data. The 25-bit of serial data format is shown below.



On each rising edge of CLK shifts one bit of serial data into internal shift register. On each rising edge of STB, the data stored in shift register is transferred into the buffer register.
Read data is cleard by $\overline{\text{RESET}}$ signal.

Gain of volume VR1 to VR5 are set depending upon S1 to S5 data.

S5	S4	S3	S2	S1	VR1, VR4	VR2, VR3	VR5
1	1	1	1	1	1.4 dB	3.0 dB	10.5 dB
1	1	1	1	0	1.2 dB	2.8 dB	9.8 dB
1	1	1	0	1	1.0 dB	2.6 dB	9.1 dB
1	1	1	0	0	0.8 dB	2.4 dB	8.4 dB
1	1	0	1	1	0.6 dB	2.2 dB	7.7 dB
1	1	0	1	0	0.4 dB	2.0 dB	7.0 dB
1	1	0	0	1	0.2 dB	1.8 dB	6.3 dB
1	1	0	0	0	0.0 dB	1.6 dB	5.6 dB
1	0	1	1	1	–0.2 dB	1.4 dB	4.9 dB
1	0	1	1	0	–0.4 dB	1.2 dB	4.2 dB
1	0	1	0	1	–0.6 dB	1.0 dB	3.5 dB
1	0	1	0	0	–0.8 dB	0.8 dB	2.8 dB
1	0	0	1	1	–1.0 dB	0.6 dB	2.1 dB
1	0	0	1	0	–1.2 dB	0.4 dB	1.4 dB
1	0	0	0	1	–1.4 dB	0.2 dB	0.7 dB
1	0	0	0	0	–1.6 dB	0.0 dB	0.0 dB

(Continued)

(Continued)

S5	S4	S3	S2	S1	VR1, VR4	VR2, VR3	VR5
0	1	1	1	1	—	–0.2 dB	–0.7 dB
0	1	1	1	0	—	–0.4 dB	–1.4 dB
0	1	1	0	1	—	–0.6 dB	–2.1 dB
0	1	1	0	0	—	–0.8 dB	–2.8 dB
0	1	0	1	1	—	–1.0 dB	–3.5 dB
0	1	0	1	0	—	–1.2 dB	–4.2 dB
0	1	0	0	1	—	–1.4 dB	–4.9 dB
0	1	0	0	0	—	–1.6 dB	–5.6 dB
0	0	1	1	1	—	–1.8 dB	–6.3 dB
0	0	1	1	0	—	–2.0 dB	–7.0 dB
0	0	1	0	1	—	–2.2 dB	–7.7 dB
0	0	1	0	0	—	–2.4 dB	–8.4 dB
0	0	0	1	1	—	–2.6 dB	–9.1 dB
0	0	0	1	0	—	–2.8 dB	–9.8 dB
0	0	0	0	1	—	–3.0 dB	–10.5 dB
0	0	0	0	0	—	–3.2 dB	–11.2 dB

2. Stand-by Mode Setting

Stand-by mode is set depending upon SB1 and SB2 data.

SB1		H	H	L	L
SB2		H	L	H	L
Transmit system block		0	x	x	x
Reception system block	Pre filter 3	0	x	0	0
	De emphasis	0	x	0	0
	Post filter 3	0	x	0	0
	Summing network	0	0	x	0
	RVDD/2	0	0	0	0
	Others reception block	0	x	x	x
SW, control block		0	0	0	0

0: Operating mode
x: Stand-by mode
When RESET signal is low, SB1 and SB2 are set high.

3. Output Pins Condition at Stand-by Mode

Pin No.	SB1	H	H	L	L
	SB2	H	L	H	L
32	COMP1	ST	HZ	HZ	HZ
26	EXP1	ST	RVDD/2	RVDD/2	RVDD/2
18	MSK	ST	HZ	ST	ST
47	MOD	ST	HZ	HZ	HZ
20	AFOUT	ST	ST	RVDD/2	ST
37	RT1	ST	HZ	HZ	HZ
39	RT3	ST	TVDD/2*1	TVDD/2*1	TVDD/2*1
29	RE1	ST	RVDD/2	RVDD/2	RVDD/2
27	RE3	ST	RVDD/2	RVDD/2	RVDD/2
24	RR1	ST	ST	RVDD/2	ST
22	RR3	ST	ST	RVDD/2	ST
41	C1	ST	TVDD/2	TVDD/2	TVDD/2
12	TVDD2	ST	HZ	HZ	HZ
13	TREF	ST	ST	ST	ST
15	RVDD2	ST	ST	ST	ST
14	RREF	ST	ST	ST	ST

HZ: High impedance.
ST: Standard output level.
*1: Pulled up by a high resistor.

■ ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Pin Name	Value	Unit
Supply Voltage	V_{DD}	V_{DD}	−0.3 to 7	V
Input Voltage	V_{IN}	All input pins	−0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT}	All output pins	−0.3 to V_{DD} + 0.3	V
Output Current	I_{OUT}	All output pins	−10 to 10	mA
Storage Temperature	T_{stg}	—	−40 to 85	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods my affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Pin Name	Value			Unit
			Min.	Typ.	Max.	
Supply Voltage	V_{DD}	V_{DD}	4.5	5.0	5.5	V
Input Voltage	V_{IN}	All input pins	0	—	V_{DD}	V
Analog Output Load Resistance 1	R_{L1}	RT1, RT3, RE1, RE3, RR1, RR3	30	—	—	kΩ
Analog Output Load Resistance 2	R_{L2}	COMP1, MOD, MSK, EXP1, AFOUT, TVDD2, RVDD2	10	—	—	kΩ
Analog Output Load Capacitance 1	C_{L1}	TREF, RREF	—	1.0	—	µF
Analog Output Load Capacitance 2	C_{L2}	TVDD2, RVDD2	—	—	100	pF
Operating Temperature	T_a	—	−30	—	60	°C

■ ELECTRICAL CHARACTERISTICS

(V_{DD} = 5.0 V ± 10%, T_a = −30 to 60°C)

Parameter	Symbol	Pin Name	Condition	Value			Unit
				Min.	Typ.	Max.	
Supply Current 1	I_{DD}	V_{DD}	MOD, MSK, AFOUT are open. SB1 = "H" SB2 = "H"	—	—	14	mA
Supply Current 2	I_{DST1}	V_{DD}	MOD, MSK, AFOUT are open. SB1 = "L" SB2 = "L"	—	—	2.0	mA
Supply Current 3	I_{DST2}	V_{DD}	MOD, MSK, AFOUT are open. SB1 = "H" SB2 = "L"	—	—	1.5	mA
Digital Input Low Voltage	V_{IL}	$\overline{DATA}$, CLK, STB, $\overline{RESET}$, AN, BYPASS, CLOCK, TAM, RAM	—	0	—	0.8	V
Digital Input High Voltage	V_{IH}	$\overline{DATA}$, CLK, STB, $\overline{RESET}$, AN, BYPASS, CLOCK, TAM, RAM	—	2.2	—	V_{DD}	V
Digital Input Low Current	I_{IL}	$\overline{DATA}$, CLK, STB, $\overline{RESET}$, AN, BYPASS, CLOCK, TAM, RAM	V_{IN} = GND	−10	—	10	µA
Digital Input High Current	I_{IH}	$\overline{DATA}$, CLK, STB, $\overline{RESET}$, AN, BYPASS, CLOCK, TAM, RAM	V_{IN} = V_{DD}	−10	—	10	µA
Analog Input Voltage	V_{IA}	COMP2, RT2, C2, DEM, RE2, EXP2, RR2, TONE	—	1/5 V_{DD}	—	4/5 V_{DD}	V
Analog Common-mode Input Voltage	V_{IAC}	AFIN (+) AFIN (−)	—	1/5 V_{DD}	—	4/5 V_{DD}	V
Analog Differential Input Voltage	V_{IAD}	AFIN (+) AFIN (−)	V_{IAD} = AFIN (+) −AFIN (−)	−2/5 V_{DD}	—	2/5 V_{DD}	V

(Continued)

(Continued)

Parameter	Symbol	Pin Name	Condition	Value			Unit
				Min.	Typ.	Max.	
Analog Input Resistance 1	R_{AIN1}	COMP2, RT2, C2, DEM, RE2, EXP2, RR2, TONE	Between input pins and 1/2 · V_{DD} pin.	100	—	—	kΩ
Analog Input Resistance 2	R_{AIN2}	AFIN (+) AFIN (−)	$\lvert V_{IAFIN}(+) - V_{IAFIN}(-) \rvert$ / $\lvert I_{IAFIN}(+) - I_{IAFIN}(-) \rvert$	30	—	—	kΩ
Analog Output Load Resistance 1	R_{LA1}	COMP1, MOD, MSK, EXP1, AFOUT	Between output pins and 1/2 · V_{DD} pin.	10	—	—	kΩ
Analog Output Load Resistance 2	R_{LA2}	RT1, RT3, RE1, RE3, RR1, RR3	—	30	—	—	kΩ
Analog Output Load Capacitance 1	C_{LA1}	TVDD2 RVDD2	Between output pins and AG pin.	—	—	100	pF
Analog Output Load Capacitance 2	C_{LA2}	TREF RREF	Between output pins and AG pin.	—	1.0	—	µF
Analog Output Voltage	V_{OA}	COMP1, C1, MOD, MSK, EXP1, AFOUT, RT1, RT3, RE1, RE3, RR1, RR3	—	1.5	—	3.5	V
Transmit Gain	T_{GAIN}	AFIN-MOD	Input: −27 dBV 1 kHz VR1 to VR3: 0 dB $R_{T1} = R_{T2} = 100$ kΩ COMP1 and COMP2 are shorted.	7.0	9.0	11.0	dB
Transmit Mute Attenuation	T_{MUTE}	AFIN-MOD	Input: −27 dBV 1 kHz VR1 to VR3: 0 dB $R_{T1} = R_{T2} = 100$ kΩ COMP1 and COMP2 are shorted.	45	—	—	dB

(Continued)

(Continued)

Parameter	Symbol	Pin Name	Condition	Value			Unit
				Min.	Typ.	Max.	
Transmit S/N Ratio	$T_{S/N}$	AFIN-MOD	Input: –27 dBV 1 kHz VR1 to VR3: 0 dB $R_{T1} = R_{T2} = 100\ k\Omega$ COMP1 and COMP2 are shorted. BW = 50 Hz to 20 kHz	40	—	—	dB
Transmit Distortion	$T_{S/D}$	AFIN-MOD	Input: –27 dBV 1 kHz VR1 to VR3: 0 dB $R_{T1} = R_{T2} = 100\ k\Omega$ COMP1 and COMP2 are shorted. BW = 50 Hz to 20 kHz	—	—	–40	dB
Reception Gain	R_{GAIN}	DEM-AFOUT	Input: –26 dBV 1 kHz VR4, 5: 0 dB $R_{R1} = R_{R2} = 100\ k\Omega$ $R_{E1} = R_{E2} = 100\ k\Omega$ EXP1 and EXP2 are shorted. TONE = 1/2 · V_{DD}	–1.0	0	1.0	dB
Reception Adder Gain	R_{GSUM}	TONE-AFOUT	Input: –26 dBV 1 kHz RR2: 1/2 · V_{DD}	–1.0	0	1.0	dB
Reception MSK Gain	R_{GMSK}	DEM-MSK	Input: –26 dBV 1 kHz	–1.0	0	1.0	dB
Reception Mute Attenuation	R_{MUTE}	DEM-AFOUT	Input: –18 dBV 1 kHz VR4, 5: 0 dB $R_{R1} = R_{R2} = 100\ k\Omega$ $R_{E1} = R_{E2} = 100\ k\Omega$ EXP1 and EXP2 are shorted. TONE = 1/2 · V_{DD}	45	—	—	dB

(Continued)

(Continued)

Parameter	Symbol	Pin Name	Condition	Value			Unit
				Min.	Typ.	Max.	
Reception S/N Ratio	$R_{S/N}$	DEM-AFOUT	Input: −18 dBV 1 kHz VR4, 5: 0 dB $R_{R1} = R_{R2} = 100\ k\Omega$ $R_{E1} = R_{E2} = 100\ k\Omega$ EXP1 and EXP2 are shorted. TONE = 1/2 · V_{DD} BW = 50 Hz to 20 kHz	45	—	—	dB
Reception Distortion	$R_{S/N}$	DEM-AFOUT	Input: −18 dBV 1 kHz VR4, 5: 0 dB $R_{R1} = R_{R2} = 100\ k\Omega$ $R_{E1} = R_{E2} = 100\ k\Omega$ EXP1 and EXP2 are shorted. TONE = 1/2 · V_{DD} BW = 50 Hz to 20 kHz	—	—	−40	dB
Deviation Limit High Voltage	V_{DLH}	C2-MOD	VR3 = 0 dB V_{C2} = 4/5 · V_{DD} TAM = L	1/2 V_{DD} + 0.050 V_{DD}	1/2 V_{DD} + 0.053 V_{DD}	1/2 V_{DD} + 0.056 V_{DD}	V
Deviation Limit Low Voltage	V_{DLL}	C2-MOD	VR3 = 0 dB V_{C2} = 1/5·V_{DD} TAM = L	1/2 V_{DD} − 0.056 V_{DD}	1/2 V_{DD} − 0.053 V_{DD}	1/2 V_{DD} − 0.050 V_{DD}	V
Electronic Volume Minimum Step Voltage 1	V_{STEP1}	COMP2-RT1 RT3-C1 C2-MOD RE3-EXP1	Min. step of volume VR1 to VR4	0.1	0.2	0.3	dB
Electronic Volume Minimum Step Voltage 2	V_{STEP2}	EXP2-RR1	Min. step of VR5	0.4	0.7	1.0	dB
Electronic Volume Maximum Variable Width 1	V_{VR1}	COMP2-RT1 RE3-EXP1	Max. variable width of VR1, VR4	2.6	3.0	3.4	dB
Electronic Volume Maximum Variable Width 2	V_{VR2}	RT3-C1 C2-MOD	Max. variable width of VR2, VR3	5.4	6.2	7.0	dB
Electronic Volume Maximum Variable Width 3	V_{VR3}	EXP2-RR1	Max. variable width of VR5	20.9	21.7	22.5	dB
Clock Duty	D_{CLK}	CLOCK	—	38	50	62	%

■ AC CHARACTERISTICS

(V_{DD} = 5.0 V ± 10%, T_a = –30 to 60°C)

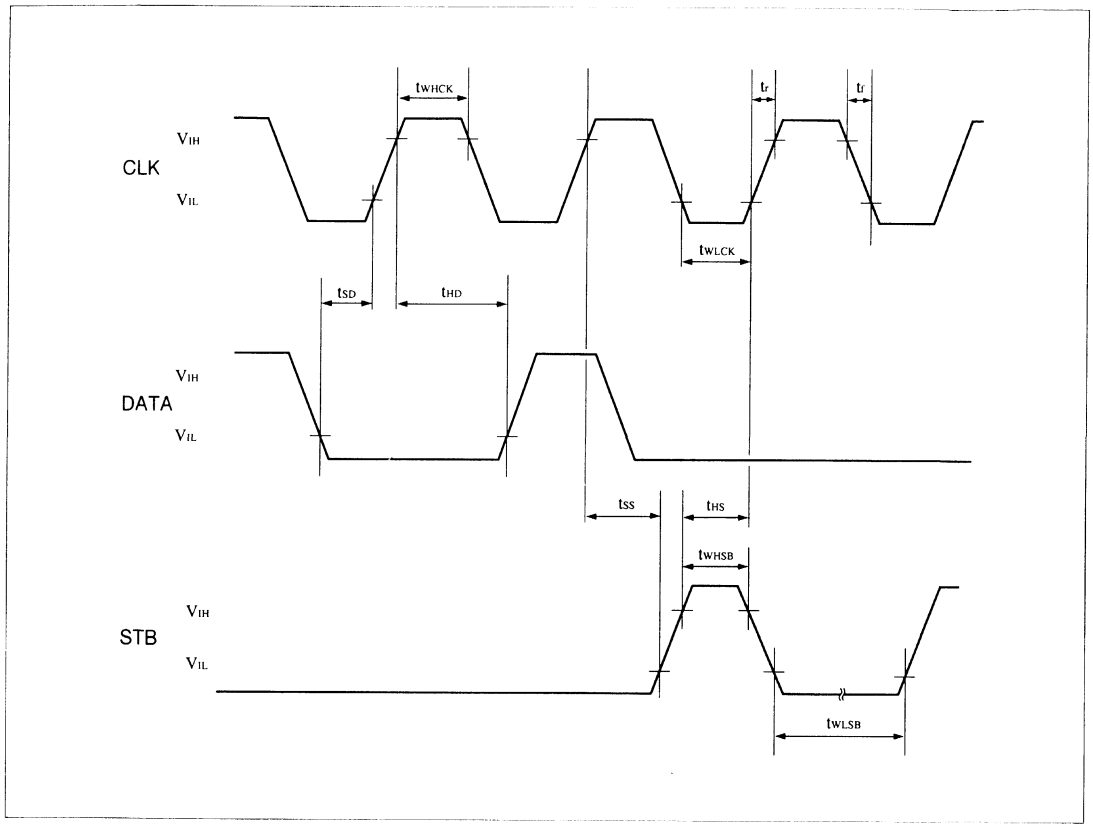
Parameter	Symbol	Pin Name	Condition	Value			Unit
				Min.	Typ.	Max.	
Clock High-level Width	t_{WHCK}	CLK	—	1.0	—	—	µs
Clock Low-level Width	t_{WLCK}	CLK	—	1.0	—	—	µs
Data Setup Time	t_{SD}	DATA, CLK	—	1.0	—	—	µs
Data Hold Time	t_{HD}	DATA, CLK	—	1.0	—	—	µs
Strobe Signal High-level Width	t_{WHSB}	STB	—	1.0	—	—	µs
Strobe-Signal Low-level Width	t_{WLSB}	STB	—	1.0	—	—	µs
Strobe Signal Setup Time	t_{SS}	STB, CLK	—	1.0	—	—	µs
Strobe Signal Hold Time	t_{HS}	STB, CLK	—	1.0	—	—	µs
Rise Time	t_r	CLK, DATA, STB	—	0	—	100	ns
Fall Time	t_f	CLK, DATA, STB	—	0	—	100	ns

■ TRANSMISSION CHARACTERISTICS

(V_{DD} = 5.0 V ± 10%, T_a = –30 to 60°C, 0 dBV = 1.0 Vrms)

Parameter	Symbol	Pin Name	Condition	Note
Transmission Characteristics	TFA	AFIN-MOD	VR1 to 3: 0 dB COMP1 and COMP2 are shorted. AN = H, R_{T1} = R_{T2} = 100 kΩ Input Level: –27 dBV	Please see Fig. 1
	TFN	AFIN-MOD	VR1 to 3: 0 dB COMP1 and COMP2 are shorted. AN = L, R_{T1} = R_{T2} = 100 kΩ Input Level: –27 dBV	Please see Fig. 2
Reception Characteristics	RFA	DEM-AFOUT	VR4, 5: 0 dB EXP1 and EXP2 are shorted. AN = H, R_{E1} = R_{E2} = 100 kΩ R_{R1} = R_{R2} = 100 kΩ T_{ONE}: 1/2·V_{DD} Input Level: –26 dBV	Please see Fig. 3
	RFN	DEM-AFOUT	VR4, 5: 0 dB EXP1 and EXP2 are shorted. AN = L, R_{E1} = R_{E2} = 100 kΩ R_{R1} = R_{R2} = 100 kΩ T_{ONE}: 1/2·V_{DD} Input Level: –26 dBV	Please see Fig, 4

■ TIMING CHART



■ TRANSMISSION CHARACTERISTICS CURVES

Fig.1 – TRANSMISSION AMPS STANDARD (AN = "H")

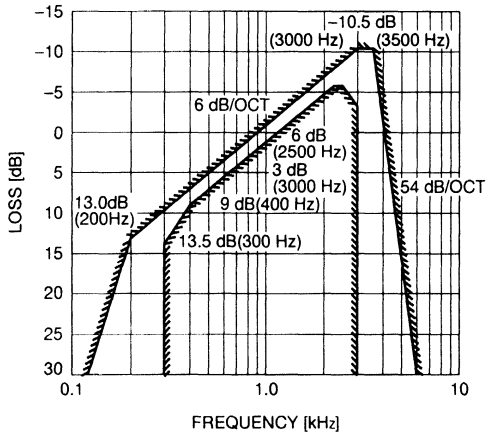


Fig.2 – TRANSMISSION NMT STANDARD (AN = "L")

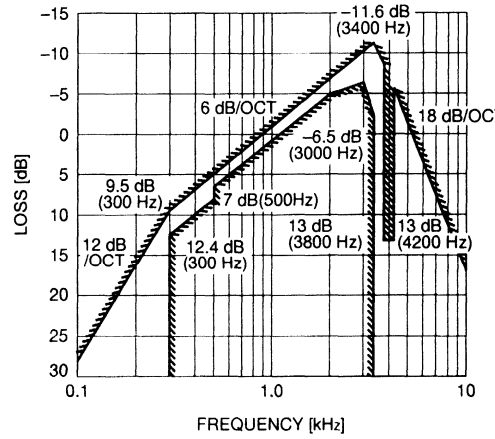


Fig.3 – RECEPTION AMPS STANDARD (AN = "H")

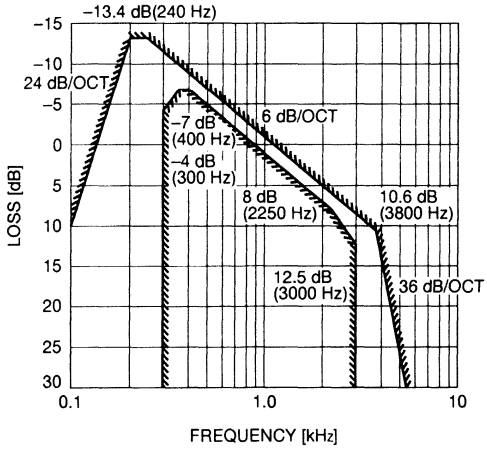
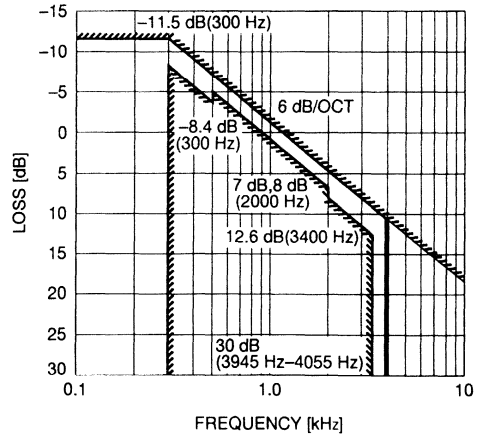


Fig.4 – RECEPTION NMT STANDARD (AN = "L")



MEMO

FUJITSU SEMICONDUCTOR
DATA SHEET

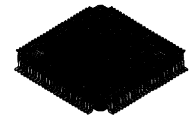
DS04-23503-2E

ASSP
CMOS AUTOMOBILE TELEPHONE AUDIO PROCESSOR
MB86490

The MB86490 processes the baseband signal for automobile telephones for both AMPS (United States) and TACS (United Kingdom) systems.
The MB86490 combines the control signal processing functions of the MB87084 and the audio signal processing functions of the MB87085 on one chip.
The MB86490's digital electronic volume enables highly precise gain control and consists of a 34-step switched capacitor filter (SCF).

- Receiver
  Phase shifter circuit: signal phase adjustable from 0 to 180 degrees.
  Pins for external expander
  Muting control
- Transmitter
  Limiter circuit suppresses instantaneous frequency deviation at frequency modulation
  Muting control
  DTMF circuit (dual- and single-tone)
  High group : 1633, 1477, 1336, 1209 and 1150 Hz
  Low group : 941, 852, 770 and 697 Hz
  Output level of low group can be set 2 dB lower than high group
- Power controller
  7-bit DAC LSB selectable: 4 mV or 20 mV
  Level shifter circuit (5 to 1 Vp-p)
- Electronic volume, DAC, DTMF and stand-by mode controlled by serial data
- Power-saving stand-by function
- Inputs and outputs CMOS compatible
- Supply voltage: +5 V

PLASTIC PACKAGE
(FPT-80P-M06)



PLASTIC PACKAGE
(FPT-100P-M05)

ABSOLUTE MAXIMUM RATINGS (See NOTE)

(GND = 0 V)

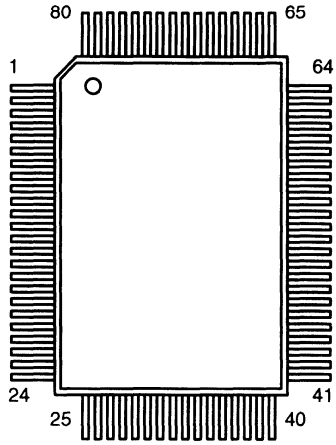
Ratings	Symbol	Pin name	Value			Unit
			Min	Typ	Max	
Supply voltage	V_{DD}	V_{DD}	GND–0.3	–	7.0	V
Input voltage	V_I	All input pins	GND–0.3	–	V_{DD}+0.3	V
Output voltage	V_O	All output pins	GND–0.3	–	V_{DD}+0.3	V
Output current	I_O	All output pins	–10	–	10	mA
Storage temperature	Tstg	–	–40	–	125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

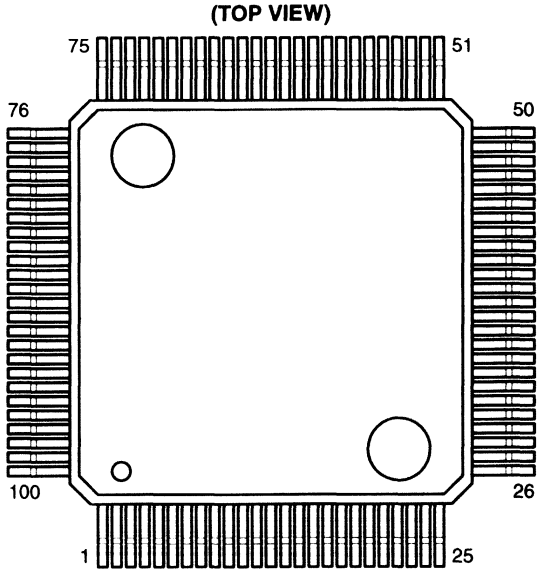
PIN ASSIGNMENT

(TOP VIEW)



(FPT-80P-M06)

Pin No.	I/O	Symbol	Pin No.	I/O	Symbol	Pin No.	I/O	Symbol	Pin No.	I/O	Symbol
1	–	(N.C.)	21	I	STB3	41	–	(N.C.)	61	O	AFOUT
2	O	LIMH	22	I	STB2	42	I	CMP2I	62	I	AMP8I
3	O	LIML	23	I	STB1	43	–	(N.C.)	63	O	AMP8O
4	O	LIMO	24	I	MODE	44	I	DISC	64	I	RR2
5	O	VR1O	25	I	DATA	45	–	(N.C.)	65	O	RR3
6	I	AFIN1	26	I	CLK	46	–	(N.C.)	66	O	RVDD2
7	I	AFIN2	27	I	$\overline{\text{RESET}}$	47	I	R2	67	O	RREF
8	O	AFINO	28	I	DTMFSS	48	O	PHSO	68	–	(N.C.)
9	I	AMP2I	29	I	RAM	49	O	C2	69	O	TVDD2
10	O	AMP2O	30	I	BYPS	50	I	R1	70	O	TREF
11	O	VR2O	31	O	RSAT	51	O	C1	71	O	DTMF2
12	–	AGT	32	O	RWBD	52	–	(N.C.)	72	I	AMP3I
13	–	(N.C.)	33	–	VDD1	53	O	AMP6O	73	–	VDD2
14	–	DG	34	–	AGR	54	I	DEM	74	O	AMP3O
15	I	SATS	35	O	PCONT	55	O	RE1	75	I	AFINN
16	I	WBDS	36	O	LS	56	I	EXP2	76	O	AMP1O
17	I	DTMFTS	37	I	PDET	57	O	RR1	77	I	WBDI
18	I	TAM	38	O	VREF	58	O	EXP1	78	I	TSAT
19	I	FRQC	39	I	ATT	59	I	RE2	79	O	TX
20	I	FCLK	40	I	DAREF	60	O	RE3	80	I	LIMI



(FPT-100P-M05)

Pin No.	I/O	Symbol	Pin No.	I/O	Symbol	Pin No.	I/O	Symbol	Pin No.	I/O	Symbol
1	O	LIMH	26	–	(N.C.)	51	I	DISC	76	–	(N.C.)
2	O	LIML	27	I	MODE	52	–	(N.C.)	77	–	(N.C.)
3	O	LIMO	28	–	(N.C.)	53	I	R2	78	I	RR2
4	O	VR1O	29	I	DATA	54	O	PHSO	79	O	RR3
5	I	AFIN1	30	–	(N.C.)	55	O	C2	80	–	(N.C.)
6	I	AFIN2	31	I	CLK	56	I	R1	81	O	RVDD2
7	O	AFIN0	32	–	(N.C.)	57	–	(N.C.)	82	O	RREF
8	I	AMP2I	33	–	(N.C.)	58	O	C1	83	–	(N.C.)
9	O	AMP2O	34	I	/RESET	59	–	(N.C.)	84	O	TVDD2
10	O	VR2O	35	I	STMFSS	60	–	(N.C.)	85	O	TREF
11	–	(N.C.)	36	I	RAM	61	–	(N.C.)	86	O	DTMF2
12	–	AGT	37	I	BYPS	62	O	AMP6O	87	I	AMP3I
13	–	(N.C.)	38	O	RSAT	63	–	(N.C.)	88	–	(N.C.)
14	–	DG	39	O	RWBD	64	I	DEM	89	–	VDD2
15	I	SATS	40	–	VDD1	65	–	(N.C.)	90	O	AMP3O
16	I	WBDS	41	–	(N.C.)	66	O	RE1	91	I	AFINN
17	I	DTMFTS	42	–	AGR	67	I	EXP2	92	–	(N.C.)
18	I	TAM	43	O	PCONT	68	–	(N.C.)	93	O	AMP1O
19	I	FRQC	44	O	LS	69	O	RR1	94	I	WBDI
20	–	(N.C.)	45	I	PDET	70	O	EXP1	95	I	TSAT
21	I	FCLK	46	O	VREF	71	I	RE2	96	–	(N.C.)
22	–	(N.C.)	47	I	ATT	72	O	RE3	97	O	TX
23	I	STB3	48	I	DAREF	73	O	AFOUT	98	I	LIMI
24	I	STB2	49	I	CMP21	74	I	AMP8I	99	–	(N.C.)
25	I	STB1	50	–	(N.C.)	75	O	AMP8O	100	–	(N.C.)

PIN DESCRIPTIONS

Circuit	Pin No. QFP	Pin No. SQFP	I/O	Symbol	Descriptions
Power supply	33	40	–	VDD1	Power supply (+5 V)
	73	89	–	VDD2	
	12	12	–	AGT	Transmitter ground (0 V)
	34	42	–	AGR	Receiver ground (0 V)
	14	14	–	DG	Digital ground (0 V)
Reference voltage section	70	85	O	TREF	Transmitter $V_{DD}/2$ circuit reference voltage
	69	84	O	TVDD2	Transmitter $V_{DD}/2$ circuit output voltage
	67	82	O	RREF	Receiver $V_{DD}/2$ circuit reference voltage
	66	81	O	RVDD2	Receiver $V_{DD}/2$ circuit output voltage
Power controller	40	48	I	DAREF	DAC reference voltage input (5 V)
	39	47	I	ATT	DAC reference voltage input (0 V)
	37	45	I	PDET	Level shifter input
	36	44	O	LS	Level shifter output
	38	46	O	VREF	DAC output
	35	43	O	PCONT	AMP11 output
Data input section	25	29	I	DATA	35-bit serial data controls the electronic volume, DAC, DTMF and stand-by function (for details, refer to the USE section). Data is loaded on the rising edge of the clock (CLK). Input data is loaded into the internal buffer register on the rising edge of STB1 to STB3. Pull the $\overline{\text{RESET}}$ pin low to initialize the buffer register. The MODE pin is used to configure the buffer register.
	26	31	I	CLK	
	27	34	I	$\overline{\text{RESET}}$	
	23	25	I	STB1	
	22	24	I	STB2	
	21	23	I	STB3	
	24	27	I	MODE	Buffer register mode switching pin (for details, see the USE section).
	20	21	I	FCLK	768-kHz clock input This pin is used for the reference clock for the SCF and DTMF generator circuits.

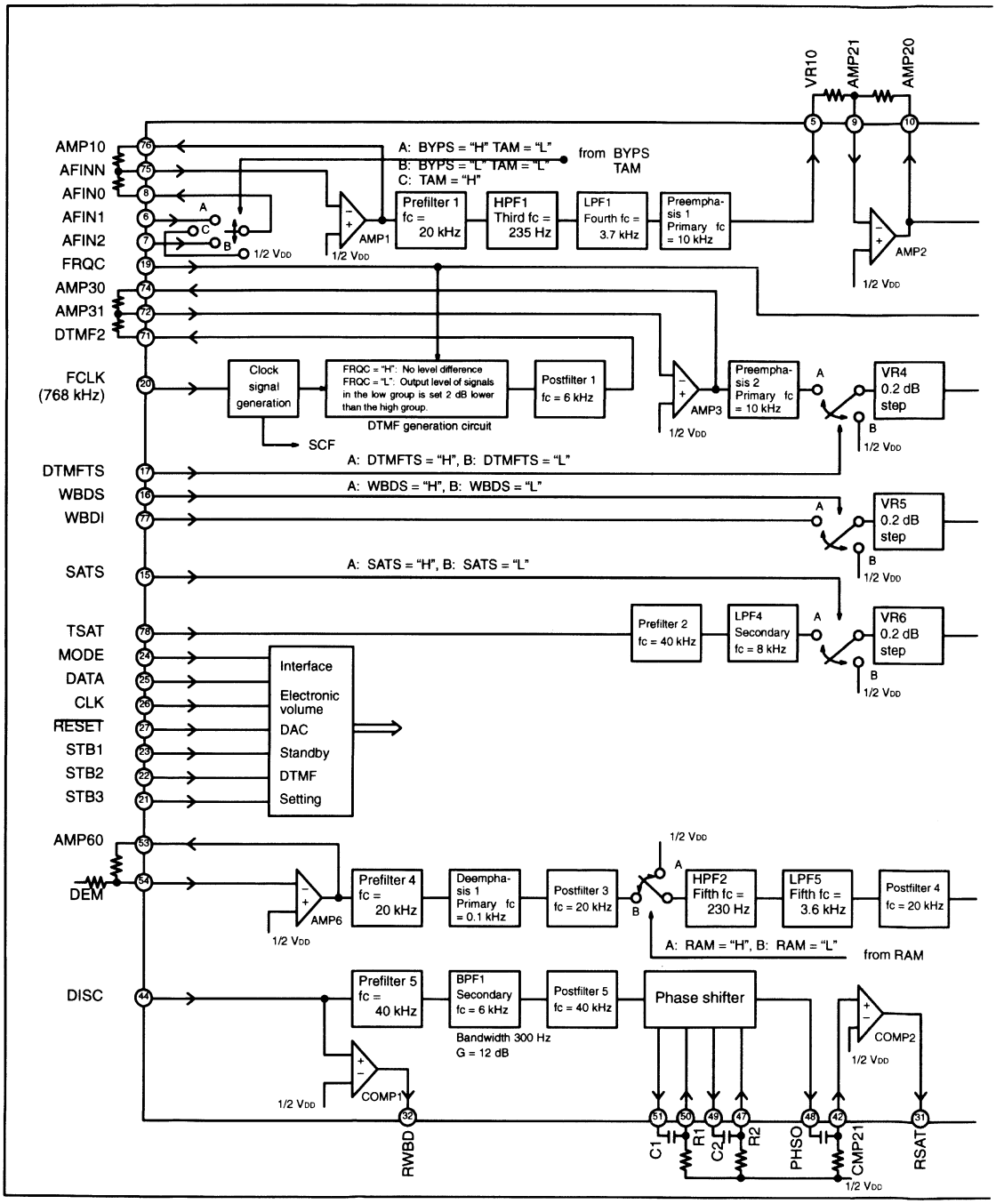
<table>
<tr><th rowspan="2">Circuit</th><th colspan="2">Pin No.</th><th rowspan="2">I/O</th><th rowspan="2">Symbol</th><th rowspan="2">Descriptions</th></tr>
<tr><th>QFP</th><th>SQFP</th></tr>
<tr><td rowspan="8">Data receiver section</td><td>44</td><td>51</td><td>I</td><td>DISC</td><td>Receive signal input</td></tr>
<tr><td>32</td><td>39</td><td>O</td><td>RWBD</td><td>Receiver wideband data output
COMP1 output</td></tr>
<tr><td>51</td><td>58</td><td>O</td><td>C1</td><td rowspan="4">Phase shifter circuit control pins
Signal phase is selectable with an external capacitor and resistor connected between these pins (for details, see the USE section).</td></tr>
<tr><td>50</td><td>56</td><td>I</td><td>R1</td></tr>
<tr><td>49</td><td>55</td><td>O</td><td>C2</td></tr>
<tr><td>47</td><td>53</td><td>I</td><td>R2</td></tr>
<tr><td>48</td><td>54</td><td>O</td><td>PHSO</td><td>Phase shifter circuit output</td></tr>
<tr><td>31</td><td>38</td><td>O</td><td>RSAT</td><td>SAT signal output</td></tr>
<tr><td>42</td><td>49</td><td>I</td><td>CMP2I</td><td>COMP2 positive input</td></tr>
<tr><td rowspan="9">Data transmitter section</td><td>19</td><td>19</td><td>I</td><td>FRQC</td><td>DTMF generator circuit and LPF3 mode switching pin:
<table>
<tr><th>FRQC</th><th>DTMF generator circuit</th><th>LPF3</th></tr>
<tr><td>H</td><td>No level difference</td><td>fc=20kHz</td></tr>
<tr><td>L</td><td>Output level of the low group signal set 2 dB lower than high group signal</td><td>fc=16 kHz</td></tr>
</table></td></tr>
<tr><td>74</td><td>90</td><td>O</td><td>AMP3O</td><td rowspan="2">AMP3 gain setting pins
AMP3O : AMP3 output
AMP3i : AMP3 inverting input</td></tr>
<tr><td>72</td><td>87</td><td>I</td><td>AMP3I</td></tr>
<tr><td>71</td><td>86</td><td>O</td><td>DTMF2</td><td>DTMF signal output</td></tr>
<tr><td>17</td><td>17</td><td>I</td><td>DTMFTS</td><td>DTMF output signal muting control “H” level : No mute
“L” level : Mute</td></tr>
<tr><td>16</td><td>16</td><td>I</td><td>WBDS</td><td>Wideband data signal muting control “H” level : No mute
“L” level : Mute</td></tr>
<tr><td>77</td><td>94</td><td>I</td><td>WBDI</td><td>Wideband data signal input</td></tr>
<tr><td>15</td><td>15</td><td>I</td><td>SATS</td><td>SAT signal muting control “H” level : No mute
“L” level : Mute</td></tr>
<tr><td>78</td><td>95</td><td>I</td><td>TSAT</td><td>SAT signal input</td></tr>
</table>

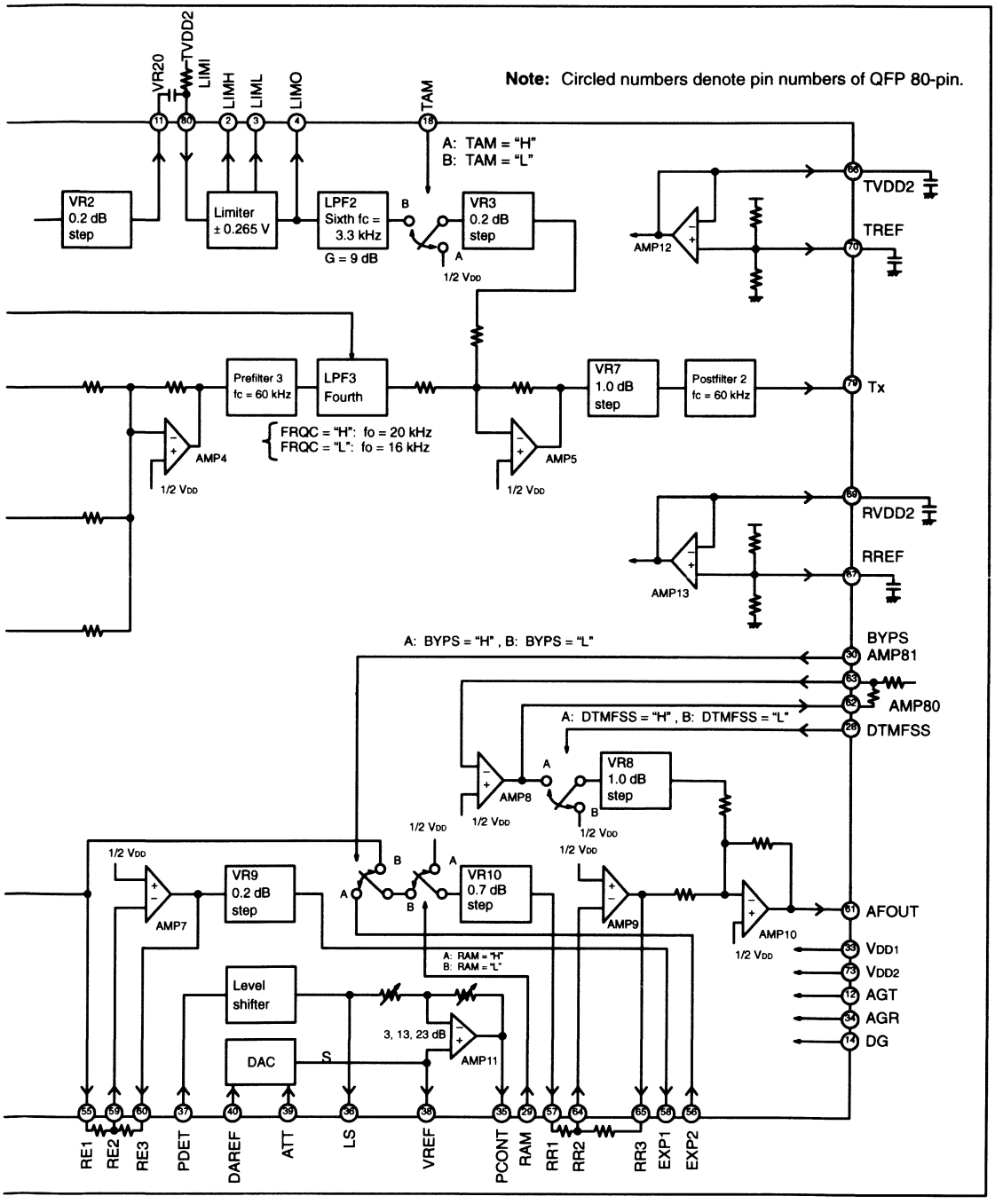
PIN DESCRIPTIONS

Circuit	Pin No. QFP	Pin No. SQFP	I/O	Symbol	Descriptions
Audio signal receiver section	54	64	I	DEM	Received audio signal input pin (AMP6 gain control pins) DEM : AMP6 inverting input AMP6O : AMP6 output
	53	62	O	AMP6O	
	29	36	I	RAM	Received audio signal muting control "H" level : Mute "L" level : No mute
	55	66	O	RE1	AMP7 gain setting pins RE1 : Postfilter 4 output RE2 : AMP7 inverting input RE3 : AMP7 output
	59	71	I	RE2	
	60	72	O	RE3	
	57	69	O	RR1	AMP9 gain setting pins RR1 : VR10 output RR2 : AMP9 inverting input RR3 : AMP9 output
	64	78	I	RR2	
	65	79	O	RR3	
	58	70	O	EXP1	Output to external expander. VR9 output
	56	67	I	EXP2	Input from external expander
	61	73	O	AFOUT	Received audio signal output
	63	75	O	AMP8O	AMP8 gain setting pins AMP8O : AMP8 output AMP8I : AMP8 inverting input
	62	74	I	AMP8I	
	28	35	I	DTMFSS	DTMF signal muting control "H" level : No mute "L" level : Mute
	30	37	I	BYPS	Switch control signal "H" level : An external compander is connected. AFIN1 is strapped to AFINO "L" level : An external compander is not connected. AFIN2 is strapped to AFINO

<table>
<tr><th rowspan="2">Circuit</th><th colspan="2">Pin No.</th><th rowspan="2">I/O</th><th rowspan="2">Symbol</th><th rowspan="2">Descriptions</th></tr>
<tr><th>QFP</th><th>SQFP</th></tr>
<tr><td rowspan="15">Audio signal transmitter section</td><td>6</td><td>5</td><td>I</td><td>AFIN1</td><td rowspan="3">Transmitted audio signal input switching pin:
<table><tr><th>TAM</th><th>BYPS</th><th>SW</th></tr><tr><td>"L"</td><td>"H"</td><td>AFIN1 is strapped to AFINO.</td></tr><tr><td>"L"</td><td>"L"</td><td>AFIN2 is strapped to AFINO.</td></tr><tr><td>"H"</td><td>–</td><td>AFINO is strapped to VDD/2.</td></tr></table></td></tr>
<tr><td>7</td><td>6</td><td>I</td><td>AFIN2</td></tr>
<tr><td>8</td><td>7</td><td>O</td><td>AFINO</td></tr>
<tr><td>5</td><td>4</td><td>O</td><td>VR1O</td><td>Preemphasis 1 output pin</td></tr>
<tr><td>75</td><td>91</td><td>I</td><td>AFINN</td><td rowspan="2">Transmitted audio signal input pin. AMP1 gain setting pins.
AFINN : AMP1 inverting input
AMP1O : AMP1 output</td></tr>
<tr><td>76</td><td>93</td><td>O</td><td>AMP1O</td></tr>
<tr><td>11</td><td>10</td><td>O</td><td>VR2O</td><td>VR2 output</td></tr>
<tr><td>10</td><td>9</td><td>O</td><td>AMP2O</td><td rowspan="2">AMP2 gain setting pins
AMP2O : AMP2 output
AMP2I : AMP2 inverting input</td></tr>
<tr><td>9</td><td>8</td><td>I</td><td>AMP2I</td></tr>
<tr><td>80</td><td>98</td><td>I</td><td>LIMI</td><td>Limiter circuit input</td></tr>
<tr><td>4</td><td>3</td><td>O</td><td>LIMO</td><td>Limiter circuit output</td></tr>
<tr><td>2</td><td>1</td><td>O</td><td>LIMH</td><td>Limiter circuit H-level signal output</td></tr>
<tr><td>3</td><td>2</td><td>O</td><td>LIML</td><td>Limiter circuit L-level signal output</td></tr>
<tr><td>18</td><td>18</td><td>I</td><td>TAM</td><td>Transmitter muting control pin
"H" level : Mute
"L" level : No mute</td></tr>
<tr><td>79</td><td>97</td><td>O</td><td>TX</td><td>Transmitted signal output</td></tr>
</table>

BLOCK DIAGRAM




Note: Circled numbers denote pin numbers of QFP 80-pin.
VR20
TVDD2
LIMI
LIMH
LIML
LIMO
TAM
A: TAM = "H"
B: TAM = "L"
VR2
0.2 dB
step
Limiter
± 0.265 V
LPF2
Sixth fc =
3.3 kHz
G = 9 dB
VR3
0.2 dB
step
1/2 VDD
AMP12
TVDD2
TREF
Prefilter 3
fc = 60 kHz
LPF3
Fourth
FRQC = "H": fo = 20 kHz
FRQC = "L": fo = 16 kHz
VR7
1.0 dB
step
Postfilter 2
fc = 60 kHz
Tx
AMP4
AMP5
RVDD2
RREF
AMP13
A: BYPS = "H", B: BYPS = "L"
BYPS
AMP81
AMP80
A: DTMFSS = "H", B: DTMFSS = "L"
DTMFSS
AMP8
VR8
1.0 dB
step
VR9
0.2 dB
step
VR10
0.7 dB
step
AMP7
AMP9
AMP10
AFOUT
VDD1
VDD2
AGT
AGR
DG
A: RAM = "H"
B: RAM = "L"
Level
shifter
DAC
3, 13, 23 dB
AMP11
RE1
RE2
RE3
PDET
DAREF
ATT
LS
VREF
PCONT
RAM
RR1
RR2
RR3
EXP1
EXP2

CIRCUIT CONFIGURATION

1. Receiver

(1) Audio signal receiver section

The audio signal receiver section processes the demodulated signal input to the demodulator pin (DEM, pin 54). The signal is then output at AFOUT (pin 61). The receiver synthesizes DTMF signals input to AMP8I (pin 62).

- Audio signal receiver section
  Audio receiver section
  - ① Gain control amplifier (AMP6)
  - ② Deemphasis circuit (prefilter 4, deemphasis 1 and postfilter 3)
  - ③ Muteing switch (control pin: RAM)
  - ④ Filter circuit (HPF2, LPF5 and postfilter 4)
  - ⑤ Gain control amplifier (AMP7)
  - ⑥ Electronic volume (VR9)
  - ⑦ Expander connection pin
  - ⑧ Bypass switch (control pin: BYPS)
  - ⑨ Muting switch (control pin: RAM)
  - ⑩ Electronic volume (VR10)
  - ⑪ Gain control amplifier (AMP9)
  - ⑫ Summing amplifier (AMP10)

  DTMF signal input section
  - ① Gain control amplifier (AMP8)
  - ② Muting switch (control pin: DTMFSS)
  - ③ Electronic volume (VR8)
  - ④ To ⑫ summing amplifier (AMP10) in the audio signal receiver section

(2) Data receiver section

The data receiver section processes demodulated signals input to DISC (pin 44) and outputs them at RSAT (pin 31). It also outputs a wideband data signal at RWBD (pin 32).

- Data receiver section
  - ① Wideband data signal output section (comparator 1)
  - ② Filter circuit (prefilter 5, BPF1 and postfilter 5)
  - ③ Phase shifter circuit
  - ④ Comparator 2

2. Transmitter

(1) Audio signal transmitter section

The audio transmitter section processes the audio signals input to AFIN1 (pin 6) or AFIN2 (pin 7) and output them at TX (pin 79).

- Audio transmitter section circuit
  - ① Audio signal input pin selector switch (control pin: BYPS and TAM)
  - ② Gain control amplifier (AMP1)
  - ③ Filter circuit (prefilter 1, HPF1 and LPF1)
  - ④ Preemphasis circuit (preemphasis 1)
  - ⑤ Gain control amplifier (AMP2)
  - ⑥ Electronic volume (VR2)
  - ⑦ Limiter circuit
  - ⑧ Filter circuit (LPF2)
  - ⑨ Muting switch (control pin: TAM)
  - ⑩ Electronic volume (VR3)
  - ⑪ Summing amplifier (AMP5)
  - ⑫ Electronic volume (VR7)
  - ⑬ Filter circuit (postfilter 2)

(2) Data transmitter section

The data transmitter section synthesizes and amplifies the clock input to FCLK (pin 20), the wideband data signal from WBDI (pin 16), and SAT signal from TSAT (pin 78). The audio signal is output at the TX pin (pin 79).

- Data transmitter circuit
  DTMF signal section
  - ① Clock generator circuit
  - ② DTMF generator circuit (DTMF generator circuit and postfilter 1)
  - ③ Gain control amplifier (AMP3)
  - ④ Preemphasis circuit (preemphasis 2)
  - ⑤ Muting switch (control pin: DTMFTS)
  - ⑥ Electronic volume (VR4)
  - ⑦ To transmitted data synthesizing section

  Wideband data signal section
  - ① Muting switch (control pin: WBDS)
  - ② Electronic volume (VR5)
  - ③ To transmitted data synthesizing section

CIRCUIT CONFIGURATION

SAT signal section

① Filter circuit (prefilter 2 and LPF4)

② Muting switch (control pin: SATS)

③ Electronic volume (VR6)

④ To transmitted data synthesizing section

Transmitted data synthesizing section

① Input signals from DTMF, wideband data and SAT signal sections

② Summing amplifier (AMP4)

③ Filter circuit (prefilter 3 and LPF3)

④ To ⑪ summing amplifier (AMP5) in the audio transmitter section

(3) Power controller

The power controller detects the transmission power of the modulated signal input to the PDET (pin 37) and controls the transmitter amplifier output using the signal output from PCONT (pin 35).

- Power controller circuit

① Level shifter circuit

② 7-bit DAC

③ Gain amplifier (AMP11)

(4) Reference voltage generator

The transmitter and receiver operate with the reference voltage output from TVDD2 (pin 69) and RVDD2 (pin 66) respectively.

① VDD/2 generator circuit (AMP12) in transmitter system

② VDD/2 generator circuit (AMP13) in receiver system

USE

The electronic volume, DAC, AMP11, DTMF and the stand-by mode are controlled by data written into the buffer register.

1. Buffer register

(1) Buffer register configuration

- Mode = "H" level

STB1	⎍	–	–
STB2	–	⎍	–
STB3	–	–	⎍
D1	–	VR84	–
D2	–	VR83	–
D3	–	VR82	–
D4	–	VR81	–
D5	–	VR74	–
D6	–	VR73	–
D7	–	VR72	–
D8	–	VR71	–
D9	–	AMS2	–
D10	–	AMS1	–
D11	–	VR55	VR105
D12	–	VR54	VR104
D13	–	VR53	VR103
D14	–	VR52	VR102
D15	–	VR51	VR101
D16	–	VR65	VR94
D17	–	VR64	VR93
D18	–	VR63	VR92
D19	–	VR62	VR91
D20	–	VR61	VR35
D21	–	VR45	VR34
D22	–	VR44	VR33
D23	–	VR43	VR32
D24	–	VR42	VR31
D25	–	VR41	VR25
D26	–	DAS1	VR24
D27	–	DAB7	VR23
D28	–	DAB6	VR22
D29	E/DH	DAB5	VR21
D30	DTS1	DAB4	–
D31	DTS2	DAB3	–
D32	DTS3	DAB2	–
D33	E/DL	DAB1	–
D34	DTS4	SB1	SB2
D35	DTS5	SB2	SB1

- Mode = "L" level

STB1	⎍	–	–
STB2	–	⎍	–
STB3	–	–	⎍
D1	–	–	VR105
D2	–	–	VR104
D3	–	–	VR103
D4	–	–	VR102
D5	–	–	VR101
D6	–	–	VR94
D7	–	–	VR93
D8	–	–	VR92
D9	–	–	VR91
D10	–	–	VR74
D11	–	–	VR73
D12	–	–	VR72
D13	–	–	VR71
D14	–	–	VR65
D15	–	–	VR64
D16	–	–	VR63
D17	–	–	VR62
D18	–	–	VR61
D19	–	–	VR55
D20	E/DH	–	VR54
D21	DTS1	–	VR53
D22	DTS2	–	VR52
D23	DTS3	–	VR51
D24	E/DL	–	VR35
D25	DTS4	–	VR34
D26	DTS5	AMS2	VR33
D27	VR45	AMS1	VR32
D28	VR44	DAS1	VR31
D29	VR43	DAB7	VR25
D30	VR42	DAB6	VR24
D31	VR41	DAB5	VR23
D32	VR84	DAB4	VR22
D33	VR83	DAB3	VR21
D34	VR82	DAB2	SB2
D35	VR81	DAB1	SB1

NOTE: Each control signal in the buffer register is set to the following logic level if the RESET pin is pulled low.

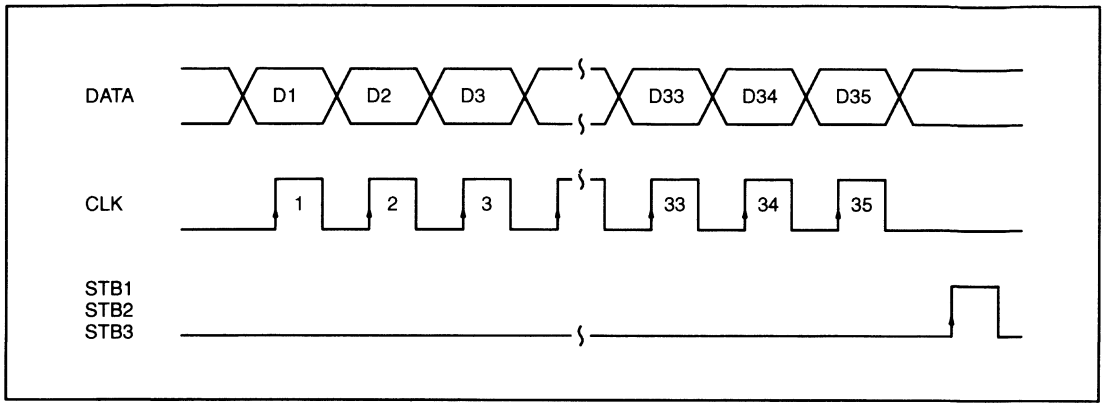
AAA : Control signals are set to "L" level.

AAA : Control signals are set to "H" level.

USE

(2) Timing chart

- DATA signal read timing



The above timing diagram shows how data is clocked into the DATA buffer register.
The DATA signal is read on the rising edge of CLK and latched in the buffer register on the rising edge of STB1, STB2 or STB3.

2. Electronic volume setting

	Buffer register name					Electronic volume No.			
Electronic volume selection conditions	VR25	VR24	VR23	VR22	VR21	VR2	–	–	–
	VR35	VR34	VR33	VR32	VR31	VR3	–	–	–
	VR45	VR44	VR43	VR42	VR41	VR4	–	–	–
	VR55	VR54	VR53	VR52	VR51	VR5	–	–	–
	VR65	VR64	VR63	VR62	VR61	VR6	–	–	–
	–	VR74	VR73	VR72	VR71	–	–	VR7	–
	–	VR84	VR83	VR82	VR81	–	–	VR8	–
	–	VR94	VR93	VR92	VR91	–	VR9	–	–
	VR105	VR104	VR103	VR102	VR101	–	–	–	VR10
	Buffer register input data					**Electronic volume setting value (dB)**			
Setting condition	H	H	H	H	H	3.0	1.4	7.0	10.5
	H	H	H	H	L	2.8	1.2	6.0	9.8
	H	H	H	L	H	2.6	1.0	5.0	9.1
	H	H	H	L	L	2.4	0.8	4.0	8.4
	H	H	L	H	H	2.2	0.6	3.0	7.7
	H	H	L	H	L	2.0	0.4	2.0	7.0
	H	H	L	L	H	1.8	0.2	1.0	6.3
	H	H	L	L	L	1.6	0.0	0.0	5.6
	H	L	H	H	H	1.4	−0.2	−1.0	4.9
	H	L	H	H	L	1.2	−0.4	−2.0	4.2
	H	L	H	L	H	1.0	−0.6	−3.0	3.5
	H	L	H	L	L	0.8	−0.8	−4.0	2.8
	H	L	L	H	H	0.6	−1.0	−5.0	2.1
	H	L	L	H	L	0.4	−1.2	−6.0	1.4
	H	L	L	L	H	0.2	−1.4	−7.0	0.7
	H	L	L	L	L	0.0	−1.6	−8.0	0.0
	L	H	H	H	H	−0.2	–	–	−0.7
	L	H	H	H	L	−0.4	–	–	−1.4
	L	H	H	L	H	−0.6	–	–	−2.1
	L	H	H	L	L	−0.8	–	–	−2.8
	L	H	L	H	H	−1.0	–	–	−3.5
	L	H	L	H	L	−1.2	–	–	−4.2
	L	H	L	L	H	−1.4	–	–	−4.9
	L	H	L	L	L	−1.6	–	–	−5.6
	L	L	H	H	H	−1.8	–	–	−6.3
	L	L	H	H	L	−2.0	–	–	−7.0
	L	L	H	L	H	−2.2	–	–	−7.7
	L	L	H	L	L	−2.4	–	–	−8.4
	L	L	L	H	H	−2.6	–	–	−9.1
	L	L	L	H	L	−2.8	–	–	−9.8
	L	L	L	L	H	−3.0	–	–	−10.5
	L	L	L	L	L	−3.2	–	–	−11.2

To use this table

To set the gain of electronic volume VR2, find VR2 in the "Electronic volume No." column. Then, select a value in the "Electronic volume setting value" column below the "Electronic volume" column. Find the input data in columns of VR25, VR23, VR22, VR21 at the left on the same row of the gain setting value.

USE

3. DAC setting

Buffer register input data							DAC output level	
DAB7	DAB6	DAB5	DAB4	DAB3	DAB2	DAB1	Condition: DAS1 = "H" level	Condition: DAS1 = "L" level
H	H	H	H	H	H	H	3.760 V	1.877 V
H	H	H	H	H	H	L	3.740 V	1.873 V
H	H	H	H	H	L	H	3.720 V	1.869 V
~	~	~	~	~	~	~	~	~
H	H	L	L	L	L	L	3.120 V	1.749 V
~	~	~	~	~	~	~	~	~
H	L	L	L	L	H	L	2.540 V	1.633 V
H	L	L	L	L	L	H	2.520 V	1.629 V
H	L	L	L	L	L	L	2.500 V	1.625 V
L	H	H	H	H	H	H	2.480 V	1.621 V
L	H	H	H	H	H	L	2.460 V	1.617 V
L	H	H	H	H	L	H	2.440 V	1.613 V
~	~	~	~	~	~	~	~	~
L	H	L	L	L	L	L	1.880 V	1.501 V
~	~	~	~	~	~	~	~	~
L	L	L	L	L	H	L	1.260 V	1.377 V
L	L	L	L	L	L	H	1.240 V	1.373 V
L	L	L	L	L	L	L	1.220 V	1.369 V

DAREF = 5.0 V, ATT = 0.0 V

4. AMP11 gain setting

Buffer register input data		AMP11 setting value	
AMS1	AMS2	Gain	PCONT output voltage
H	H	23 (dB)	$V_{REF} - 14.13 \times (LS - V_{REF})$ (V)
L	H		
H	L	13 (dB)	$V_{REF} - 4.46 \times (LS - V_{REF})$ (V)
L	L	3 (dB)	$V_{REF} - 1.41 \times (LS - V_{REF})$ (V)

5. DTMF output level setting

(1) High group frequency setting method

Buffer register input data				Output frequency
E/DH	DTS1	DTS2	DTS3	
H	H	H	L	1633 Hz
H	H	L	L	1477 Hz
H	L	H	L	1336 Hz
H	L	L	L	1209 Hz
H	L	L	H	1150 Hz
H	H	–	H	Counter is not operating.
H	–	H	H	
L	–	–	–	

(2) Low guoup frequency setting method

Buffer register input data			Output frequency
E/DL	DTS4	DTS5	
H	H	H	941 Hz
H	H	L	852 Hz
H	L	H	770 Hz
H	L	L	697 Hz
L	–	–	Counter is not operating.

USE

6. Stand–by mode

(1) Buffer register setting data

SB1 input data		L	H	L	H
SB2 input data		H	L	L	H
Circuit name	COMP1	○	○	○	○
	AMP8, VR8	○	○	○	○
	DTMF generator cercuit, postfilter 1	○	×	○	○
	AMP3, preemphasis 2, VR4, VR6, prefilter 2, LPF4, prefilter 5, BPF1, postfilter 5, Phase shifter, COMP2	×	×	×	○
	Level shifter, DAC, AMP11	○	○	×	○
	VR5, AMP4, prefilter 3, LPF3, AMP5, VR7, postfilter 2	○	○	×	○
	AMP1, prefilter 1, HPF1, LPF1, preemphasis 1, AMP2, VR2, limiter, LPF2, VR3	×	×	×	○
	AMP6, prefilter 4, deemphasis 1, postfilter 3	×	×	×	○
	AMP10	○	○	○	○
	HPF2, LPF5, postfilter 4, AMP7, VR9, VR10, AMP9	×	×	×	○
	AMP12, AMP13	○	○	○	○
	SW, control cercuit, buffer register	○	○	○	○

○ : Operating
× : Stand–by

(2) Output pin status in stand–by mode

Pin No.		Symbol	Output pin status			
QFP	SQFP					
32	39	PWBD	–	–	–	–
31	38	RSAT	L	L	L	–
79	97	TX	–	–	D	–
49	55	C2	D	D	D	–
51	58	C1	D	D	D	–
71	86	DTMF2	–	D	–	–
74	90	AMP3O	D	D	D	–
63	75	AMP8O	–	–	–	–
35	43	PCONT(*)	–	–	Z	–
36	44	LS(*)	–	–	Z	–
38	46	VREF	–	–	Z	–
76	93	AMP1O	D	D	D	–
5	4	VR1O	D	D	D	–
10	9	AMP2O	D	D	D	–
11	10	VR2O	D	D	D	–
2	1	LIMH	–	–	–	–
3	2	LIML	–	–	–	–
4	3	LIMO	D	D	D	–
53	62	AMP6O	D	D	D	–
61	73	AFOUT	–	–	–	–
SB1 input data			L	H	L	H
SB2 input data			H	L	L	H

Pin No.		Symbol	Output pin status			
QFP	SQFP					
55	66	RE1	D	D	D	–
60	72	RE3	D	D	D	–
57	69	RR1	D	D	D	–
65	79	RR3	D	D	D	–
58	70	EXP1	D	D	D	–
48	54	PHSO	D	D	D	–
69	84	TVDD2	–	–	–	–
70	85	TREF	–	–	–	–
66	81	RVDD2	–	–	–	–
67	82	RREF	–	–	–	–
SB1 linput data			L	H	L	H
SB2 input data			H	L	L	H

NOTE: * : LS is strapped to PCONT with a high–resestance.
Z : High impedance
D : $V_{DD}/2$ level
H : V_{DD} level
L : Ground level
– : Normal signal output

RECOMMENDED OPERATING CONDITIONS

(GND=0 V)

Parameter		Symbol	Pin name	Value			Unit
				Min	Typ	Max	
Supply voltage		V_{DD}	V_{DD}	4.5	5.0	5.5	V
Input voltage		V_I	All input pins	0.0	–	V_{DD}	V
Analog section	Output load registance 1	R_{LA1}	TVDD2, RVDD2, VREF, LS, PCONT, EXP1, AFOUT, TX	10	–	–	kΩ
	Output load registance 2	R_{LA2}	AMP1O, AMP3O, AMP6O, C1, C2, RE1, RE3, RR1, RR3, AMP8O, LOMO, VR2O, VR1O	30	–	–	kΩ
	Output load capacitance 1	C_{L1}	TVDD2, RVDD2	–	–	100.0	pF
	Output load capacitance 2	C_{L2}	TREF, RREF	–	1.0	–	µF
	Output load capacitance 3	C_{L3}	TX, LS, VREF, PCONT, DTMF2, AMP3O, AMP6O	–	–	30.0	pF
Operating temperature		T_A	–	–30	–	70	°C

DC CHARACTERISTICS

(V_{DD}=4.5 to 5.5 V, T_A=–30 to +70°C, 0 dBV=1.0 Vrms)

Parameter		Symbol	Pin name	Condition	Value			Unit
					Min	Typ	Max	
Supply current 1		I_{DD1}	V_{DD}	SB1="L", SB2="H"	–	6.1	10.5	mA
Supply current 2		I_{DD2}	V_{DD}	SB1="H", SB2="L"	–	4.9	8.4	mA
Supply current 3		I_{DD3}	V_{DD}	SB1="L", SB2="L"	–	2.9	5.0	mA
Supply current 4		I_{DD4}	V_{DD}	SB1="H", SB2="H"	–	16.0	28.0	mA
Digital section	Low level input voltage	V_{IL}	FRQC, FCLK, DTMFTS, WBDS, SATS, DATA, CLK, $\overline{\text{RESET}}$, STB1, STB2, STB3, RAM, DTMFSS, BYPS, TAM, MODE	–	0.0	–	V_{DD} x0.3	V
	High level input voltage	V_{IH}	FRQC, FCLK, DTMFTS, WBDS, SATS, DATA, CLK, $\overline{\text{RESET}}$, STB1, STB2, STB3, RAM, DTMFSS, BYPS, TAM, MODE	–	V_{DD} x0.7	–	V_{DD}	V
	Low level input current	I_{IL}	FRQC, FCLK, DTMFTS, WBDS, SATS, DATA, CLK, $\overline{\text{RESET}}$, STB1, STB2, STB3, RAM, DTMFSS, BYPS, TAM, MODE	V_I=GND	–10	–	10	µA
	High level input current	I_{IH}	FRQC, FCLK, DTMFTS, WBDS, SATS, DATA, CLK, $\overline{\text{RESET}}$, STB1, STB2, STB3, RAM, DTMFSS, BYPS, TAM, MODE	V_I=V_{DD}	–10	–	10	µA
	Low level output voltage	V_{OL}	RWBD, RSAT	I_{OL}=2.0 mA	0.0	–	0.4	V
	High level output voltage	V_{OH}	RWBD, RSAT	I_{OL}=–0.1 mA	4.0	–	V_{DD}	V
				I_{OL}=–1.0 mA	2.4	–	V_{DD}	

DC CHARACTERISTICS

(V_{DD}=4.5 to 5.5 V, T_A=–30 to +70°C, 0 dBV=1.0 Vrms)

Parameter		Symbol	Pin name	Condition	Value			Unit
					Min	Typ	Max	
Analog section	Input voltage range	V_{IA}	AFINN, AFIN1, AFIN2, AMP3I, WBDI, TSAT, DEM, DISC, R1, R2, RE2, PDET, RR2, EXP2, AMP8I, LIMI, AMP2I	–	1/5V_{DD}	–	4/5V_{DD}	V
	Input registance 1	R_{AIN1}	AFINN, AFIN1, AFIN2, AMP3I, TSAT, DEM, DISC, R1, R2, RE2, RR2, AMP8I, LIMI, AMP2I	Between input pin and V_{DD}/2	200	–	–	kΩ
	Input registance 2	R_{AIN2}	WBDI, DAREF, ATT, PDET, EXP2	Between input pin and V_{DD}/2	30	–	–	kΩ
	Output voltage range	V_{OA}	AMP1O, AFINO, AMP3O, DTMF2, AMP6O, C1, C2, RE1, RE3, VREF, LS, PCONT, RR1, RR3, EXP1, AFOUT, AMP8O, TX, LIMO, VR2O, VR1O	–	1.5	–	3.5	V
	DAC output voltage range	V_{ODA}	VREF	DAC minimum output voltage	–	–	1.5	V
				DAC maximum output voltage DAS1="H" level	3.5	–	–	V
				DAC maximum output voltage DAS1="L" level	1.75	–	–	V
	Level shifter output voltage range	V_{OLS}	PCONT	–	1.5	–	3.5	V
	Limiter high level voltage	V_{DLH}	LIMO	Input level V_{LIMI}=3/4V_{DD}	V_{DD}/2 +0.050 xV_{DD}	V_{DD}/2 +0.053 xV_{DD}	V_{DD}/2 +0.056 xV_{DD}	V
	Limiter low level voltage	V_{DLL}	LIMO	Input level V_{LIMI}=1/4V_{DD}	V_{DD}/2 –0.056 xV_{DD}	V_{DD}/2 –0.053 xV_{DD}	V_{DD}/2 –0.050 xV_{DD}	V

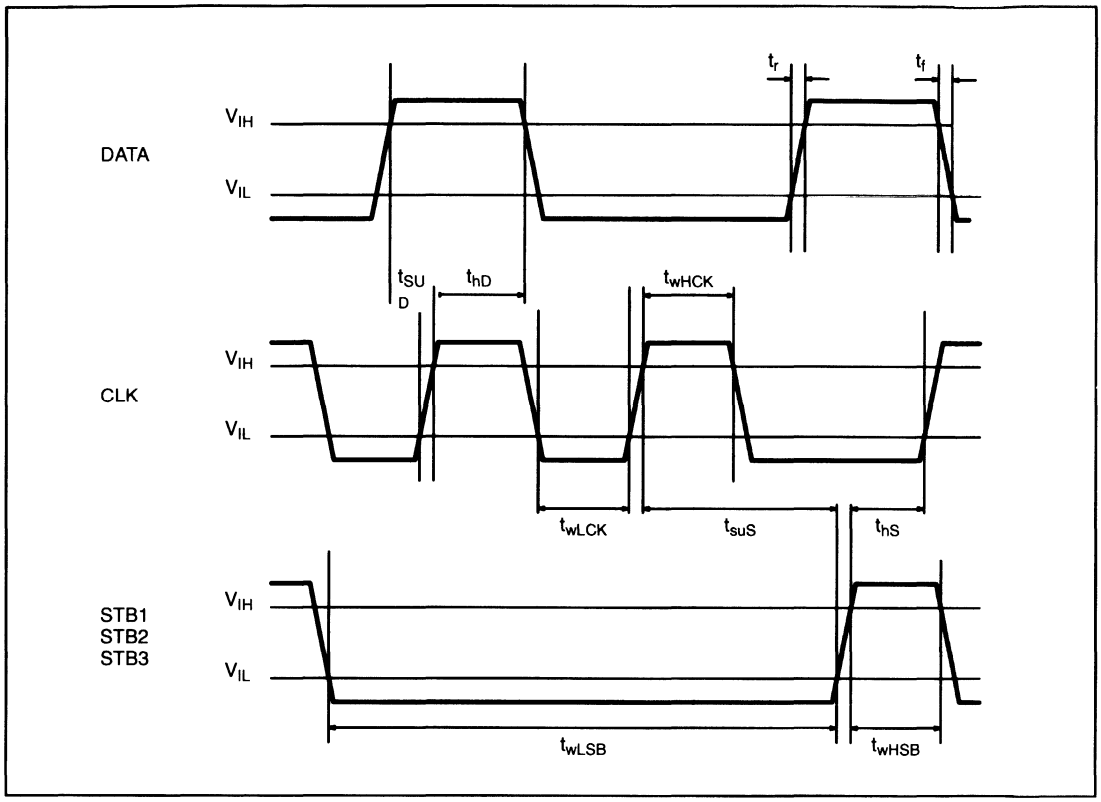
AC CHARACTERISTICS

(V_{DD}=4.5 to 5.5 V, T_A=–30 to +70°C, 0 dBV=1.0 Vrms)

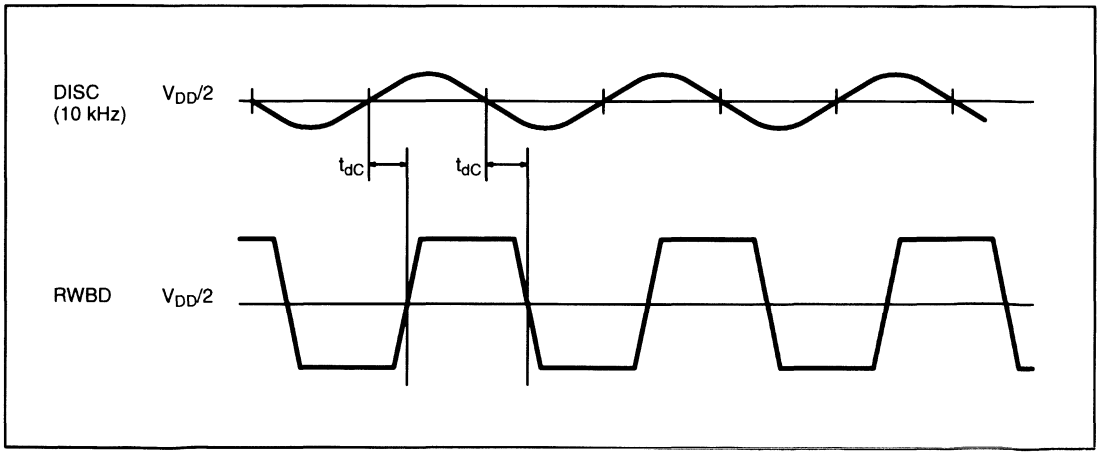
Parameter	Symbol	Pin name	Condition	Value			Unit
				Min	Typ	Max	
Clock duty cycle	D_{CLK}	FCLK	Rate of clock="H" in a clock cycle	38	50	62	%
Clock High level time	t_{wHCK}	CLK	–	1.0	–	–	µs
Clock Low level time	t_{wLCK}	CLK	–	1.0	–	–	µs
Data setup time	t_{suD}	DATA, CLK	–	1.0	–	–	µs
Data hold time	t_{hD}	DATA, CLK	–	1.0	–	–	µs
High level strobe time	t_{wHSB}	STB1, STB2, STB3	–	1.0	–	–	µs
Low level strobe time	t_{wLSB}	STB1, STB2, STB3	–	1.0	–	–	µs
Strobe setup time	t_{suS}	STB1, STB2, STB3, CLK	–	1.0	–	–	µs
Strobe hold time	t_{hS}	STB1, STB2, STB3, CLK	–	1.0	–	–	µs
Rise time	t_r	STB1, STB2, STB3, FCLK, CLK, DATA	–	0	–	100	ns
Fall time	t_f	STB1, STB2, STB3, FCLK, CLK, DATA	–	0	–	100	ns
Comparator delay time	t_{dC}	DISC, RWBD	DISC input level =–17.2 dBV at 10 kHz	0	–	1.0	µs
RSAT duty cycle	D_{RSAT}	DISC, RSAT	DISC input level =–29.0 dBV at 6 kHz Time of RSAT="H" level	75	83	91	µs

TIMING CHART

1. Interface



2. Comparator



TRANSMISSION CHARACTERISTICS

(V_{DD}=5.0 V±10%, T_A=–30 to +70°C, 0 dBV=1.0 Vrms)

Parameter	Symbol	Pin name	Condition	Value			Unit
				Min	Typ	Max	
Transmit gain 1	T_{G1}	WBDI-TX	Input level=–9.0 dBV at 10 kHz Electronic volume setting=0.0 dB WBDS="H"	–1.0	0.0	1.0	dB
Transmit gain 2	T_{G2}	TSAT-TX	Input level=–21.0 dBV at 6 kHz Electronic volume setting=0.0 dB SATS="H"	–1.0	0.0	1.0	dB
Transmit gain 3	T_{G3}	AFINN-TX	Input level=–27.0 dBV at 1 kHz Electronic volume setting=0.0 dB Gain control amplifier setting=0.0 dB TAM="L"	7.0	9.0	11.0	dB
Transmit muting level	T_{MUTE}	AFINN-TX	Input level=–27.0 dBV at 1 kHz Electronic volume setting=0.0 dB Gain control amplifier setting=0.0 dB TAM="H" 0.05 to 3.0 kHz direct detection	45.0	–	–	dB
Transmission S/N	$T_{S/N}$	AFINN-TX	Input level=–27.0 dBV at 1 kHz Electronic volume setting=0.0 dB Gain control amplifier setting=0.0 dB TAM="L" Band: 0.05 to 20.0 kHz	40.0	–	–	dB
Transmission signal-to-distortion	$T_{S/D}$	AFINN-TX	Input level=–27.0 dBV at 1 kHz Electronic volume setting=0.0 dB Gain control amplifier setting=0.0 dB TAM="L" Band: 0.05 to 20.0 kHz	–	–	–40.0	dB
Receive gain 1	R_{G1}	DEM-AFOUT	Input level=–26.0 dBV at 1 kHz Electronic volume setting=0.0 dB Gain control amplifier setting=0.0 dB EXP1 strapped to EXP2 DTMFSS="L", RAM="L"	–1.0	0.0	1.0	dB
Receive muting level	R_{MUTE}	DEM-AFOUT	Input level=–18.0 dBV at 1 kHz Electronic volume setting=0.0 dB Gain control amplifier setting=0.0 dB EXP1 strapped to EXP2 DTMFSS="L", RAM="H" 0.05 to 3.0 kHz direct detection	45.0	–	–	dB
Receive S/N	$R_{S/N}$	DEM-AFOUT	Input level=–18.0 dBV at 1 kHz Electronic volume setting=0.0 dB Gain control amplifier setting=0.0 dB EXP1 strapped to EXP2 DTMFSS="L", RAM="L" Band: 0.05 to 20.0 kHz	45.0	–	–	dB
Receive signal-to-distortion	$R_{S/D}$	DEM-AFOUT	Input level=–18.0 dBV at 1 kHz Electronic volume setting=0.0 dB Gain control amplifier setting=0.0 dB EXP1 strapped to EXP2 DTMFSS="L", RAM="L" Band: 0.05 to 20.0 kHz	–	–	–40.0	dB

TRANSMISSION CHARACTERISTICS

(V_{DD}=5.0 V±10%, T_A=–30 to +70°C, 0 dBV=1.0 Vrms)

Parameter		Symbol	Pin name	Condition		Value			Unit
						Min	Typ	Max	
Transmitter	Transmission frequency characteristic 1 (Attenuation characteristic)	T_{F1}	AFINN-TX	Input level=–27.0 dBV at 1.0 kHz reference Electronic volume setting=0.0 dB Gain control amplifier setting=0.0 dB TAM="L"		See figure 1.			
	Transmission frequency characteristic 2 (Attenuation characteristic)	T_{F2}	TSAT-TX	Input level= –21.0 dBV at 1.0 kHz reference Electronic volume setting=0.0 dB SATS="H" FRQC="H"	Less than 6.00 kHz	–1.0	0.0	3.0	dB
					6.00 to 7.20 kHz	–1.0	0.0	5.0	dB
					8.80 to 17.6 kHz	3.0	–	–	dB
					17.6 to 60.0 kHz	9.0	–	–	dB
					60.0 kHz or more	35.0	–	–	dB
Receiver	Receive frequency characteristic 1 (Attenuation characteristic)	R_{F1}	DEM-AFOUT	Input level=–26.0 dBV at 1.0 kHz reference Electronic volume setting=0.0 dB Gain control amplifier setting=0.0 dB Strapped between EXP1 and EXP2 DTMFSS="L", RAM="L"		See figure 2.			
	Receive frequency characteristic 2 (Attenuation characteristic)	R_{F2}	DISC-CI	Input level= –29.0 dBV at 6 kHz reference Electronic volume setting=0.0 dB	Less than 5.4 kHz	10.0	–	–	dB
					5.4 to 5.8 kHz	3.0	–	–	dB
					5.87 to 5.97 kHz	–1.0	–	4.5	dB
					5.97 to 6.03 kHz	–1.0	–	2.0	dB
					6.03 to 6.13 kHz	–1.0	–	4.5	dB
					6.20 to 6.60 kHz	3.0	–	–	dB
					6.60 kHz or more	9.0	–	–	dB

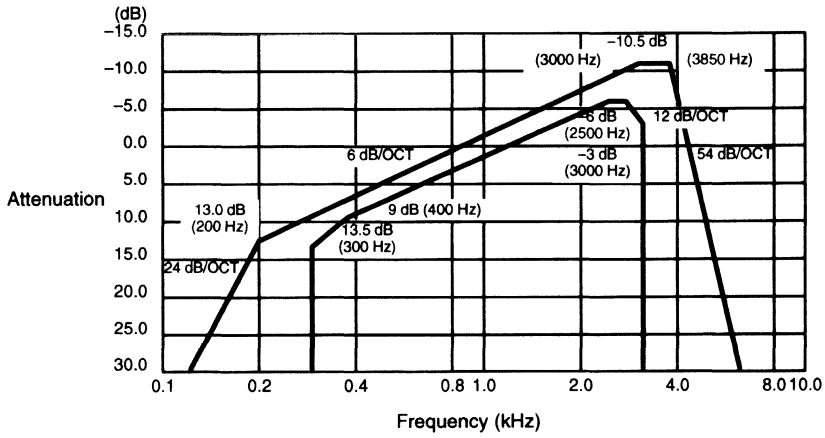


Figure 1 Transmitter frequency characteristic (AMPS/TACS)

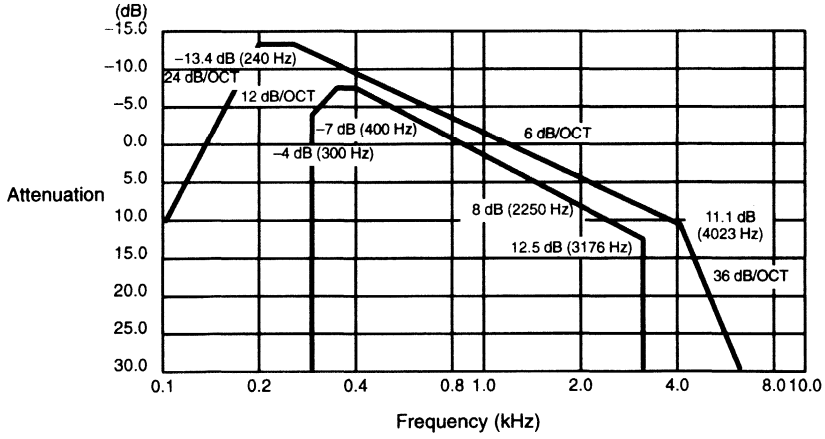


Figure 2 Receiver frequency characteristic (AMPS/TACS)

ELECTRONIC VOLUME AND DAC CHARACTERISTICS

(V_{DD}=5.0 V±10%, T_A=–30 to +70°C, 0 dBV=1.0 Vrms)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Electronic volume minimum step width 1	V_{STP1}	VR9	0.1	0.2	0.3	dB
Electronic volume minimum step width 2	V_{STP2}	VR2, VR3, VR4, VR5, VR6	0.1	0.2	0.3	dB
Electronic volume minimum step width 3	V_{STP3}	VR7, VR8	0.5	1.0	1.5	dB
Electronic volume minimum step width 4	V_{STP4}	VR10	0.4	0.7	1.0	dB
Electronic volume maximum variable width 1	V_{VR1}	VR9	2.6	3.0	3.4	dB
Electronic volume maximum variable width 2	V_{VR2}	VR2, VR3, VR4, VR5, VR6	5.4	6.2	7.0	dB
Electronic volume maximum vatiable width 3	V_{VR3}	VR7, VR8	14.2	15.0	15.8	dB
Electronic volume maximum variable width 4	V_{RV4}	VR10	20.9	21.7	22.5	dB
DAC minimum step width 1	V_{DA1}	DAS1="H"	10.0	20.0	30.0	mV
DAC minimum step width 2	V_{DA2}	DAS1="L"	2.0	4.0	6.0	mV

DTMF OUTPUT FREQUENCY

(V_{DD}=5.0 V±10%, T_A=–30 to +70°C, 0 dBV=1.0 Vrms)

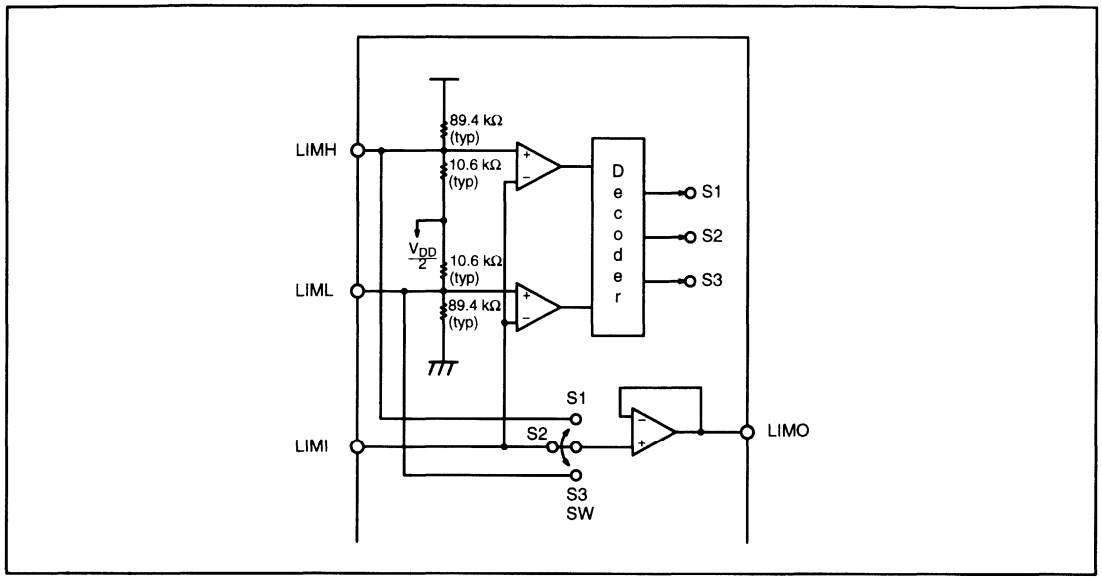
	Specified output frequency	Symbol	Actual output frequency	Error	Error standard	Note
High-group	1633 Hz	FH1	1634.0 Hz	+0.06%	±0.3%	FCLK=768 kHz
	1477 Hz	FH2	1476.9 Hz	–0.01%		
	1336 Hz	FH3	1338.0 Hz	+0.15%		
	1209 Hz	FH4	1207.5 Hz	–0.13%		
	1150 Hz	FH5	1149.7 Hz	–0.03%		
Low-group	941 Hz	FL1	941.2 Hz	+0.02%		
	852 Hz	FL2	853.3 Hz	+0.16%		
	770 Hz	FL3	769.5 Hz	–0.06%		
	697 Hz	FL4	698.2 Hz	+0.17%		

DTMF CHARACTERISTICS

(V_{DD}=5.0 V±10%, T_A=–30 to +70°C, 0 dBV=1.0 Vrms)

Parameter	Symbol	Pin name	Condition		Value			Unit
					Min	Typ	Max	
DTMF output level 1	A_{OT1}	DTMF2	1209 Hz output	V_{DD}=5.0 V	–13.3	–12.3	–11.3	dBV
				V_{DD}=5.0V±10%	–14.3	–12.3	–10.3	dBV
DTMF output level 2	A_{OT2}	TX	1209 Hz output Electronic volume setting=0.0 dB Gain control amplifier setting=0.0 dB DTMFTS="H"	V_{DD}=5.0 V	–13.8	–12.3	–10.8	dBV
				V_{DD}=5.0V±10%	–14.8	–12.3	–9.8	dBV
DTMF output level 3	A_{OT3}	AFOUT	1209 Hz output Electronic volume setting=0.0 dB AMP8 gain setting=–15.7 dB DTMFSS="H"	V_{DD}=5.0 V	–29.0	–28.0	–27.0	dBV
				V_{DD}=5.0V±10%	–30.0	–28.0	–26.0	dBV
Difference of level between high and low groups of DTMF1	D_{LH1}	DTMF2	High group level – low group level	FRQC="H"	–0.2	0.0	0.2	dB
				FRQC="L"	1.8	2.0	2.2	dB
Difference of level between high and low groups of DTMF2	D_{LH2}	TX	1633 Hz level – 697 Hz level Electronic volume setting=0.0 dB Gain control amplifier setting=0.0 dB DTMFTS="H", FRQC="H"		7.2	7.4	7.6	dB
DTMF distortion	T_{HN}	TX	Signal to noise ratio harmonic 697 Hz output		23.0	–	–	dB

LIMITER CIRCUIT

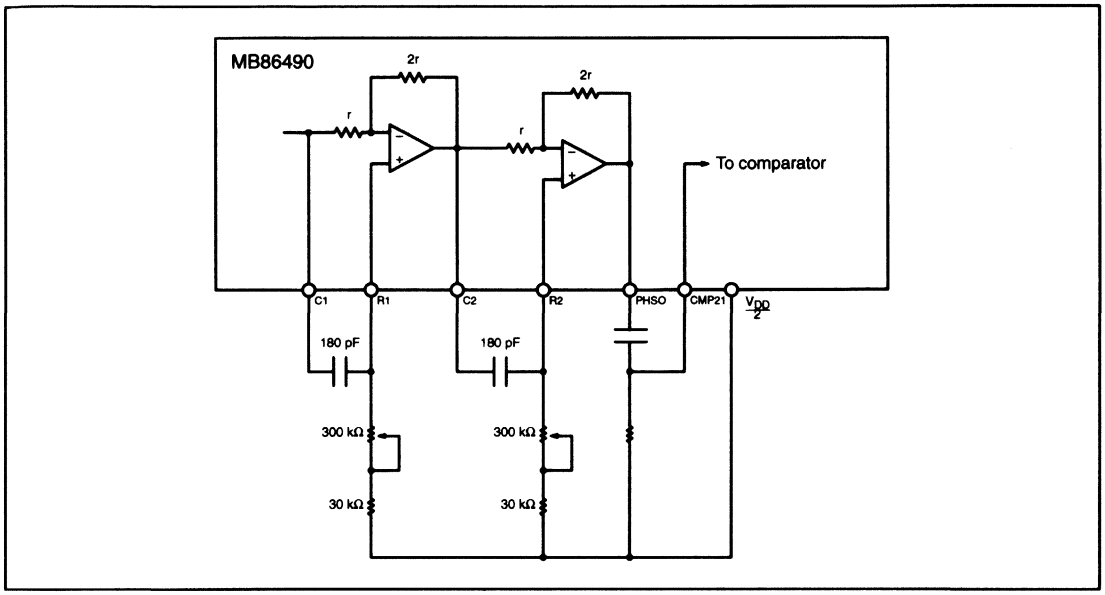


Input level	SW	LIMO output level
$V_{LIML} > V_{LIMI}$	S3	$V_{DD}/2-0.265$ V
$V_{LIML} \leq V_{LIMI} \leq V_{LIMH}$	S2	V_{LIMI} V
$V_{LIMH} < V_{LIMI}$	S1	$V_{DD}/2+0.265$ V

V_{DD}=5.0 V (typical)

PHASE SHIFTER CIRCUIT

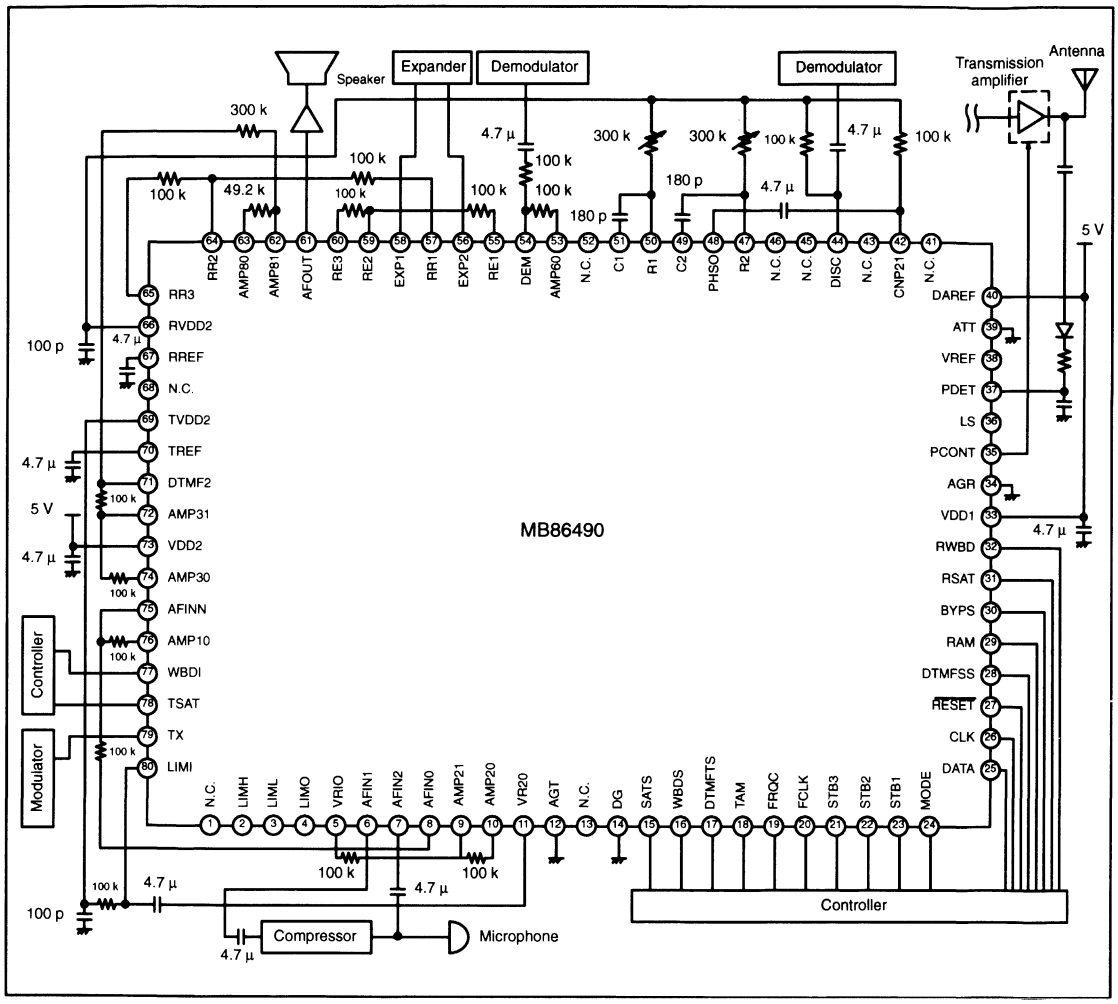
The phase shifter circuit uses an external controller to change the phase of a 6 kHz ± 30 Hz signal from to 180 degrees.



The operational amplifier changes the signal phase from 0 to 90 degrees per step.
The combined resistance from R1 and R2 to $V_{DD}/2$ should be at least 30 kΩ.

APPLICATION CIRCUIT

(For QFP80)



FUJITSU SEMICONDUCTOR
DATA SHEET

DS04–23505–1E

ASSP

FRONT–END LSI

MB54501

INTRODUCTION

The Fujitsu MB54501 includes a low-noise amplifier and a mixer, which are used for front end of mobile telecommunication systems.
Using Fujitsu's advanced technology, MB54501 achieves an Icc of 6.0mA (typ.).

ELECTRICAL CHARACTERISTICS

	Amplifier	Mixer
• Supply voltage	3V (typ.)	3V (typ.)
• Current consumption	3mA (typ.)	3mA (typ.)
• Input frequency	1.1GHz(max.)	1.1GHz(max.)
• Gain	14dB (typ.) *1	15dB (typ.) *2
• Noise figure	2.2dB (typ.) *1	5dB (SSB, typ.) *2
• 1dB compression point	–1dBm (typ.) *1	
• Input return loss	8dB (typ.) *1	
• Output return loss	10dB (typ.) *1	

*1 : Measured by the circuit of "measurement circuit example". (fin = 878MHz)

*2 : Measured by the circuit of "measurement circuit example". (IF = 90MHz)

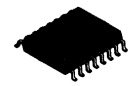
PACKAGE

- 16-pin Plastic Shrink Small Outline Package (Suffix: -PFV)

ABSOLUTE MAXIMUM RATINGS

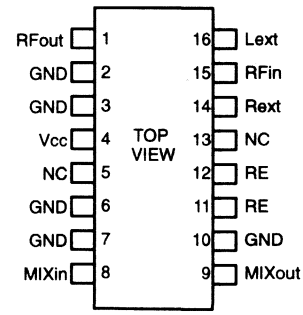
Parameters	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.5 to 7.0	V
Output Voltage	V_O	–0.5 to V_{CC}+0.5	V
Output Current	I_O	0 to 10	mA
Storage Temperature	T_{STG}	–55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



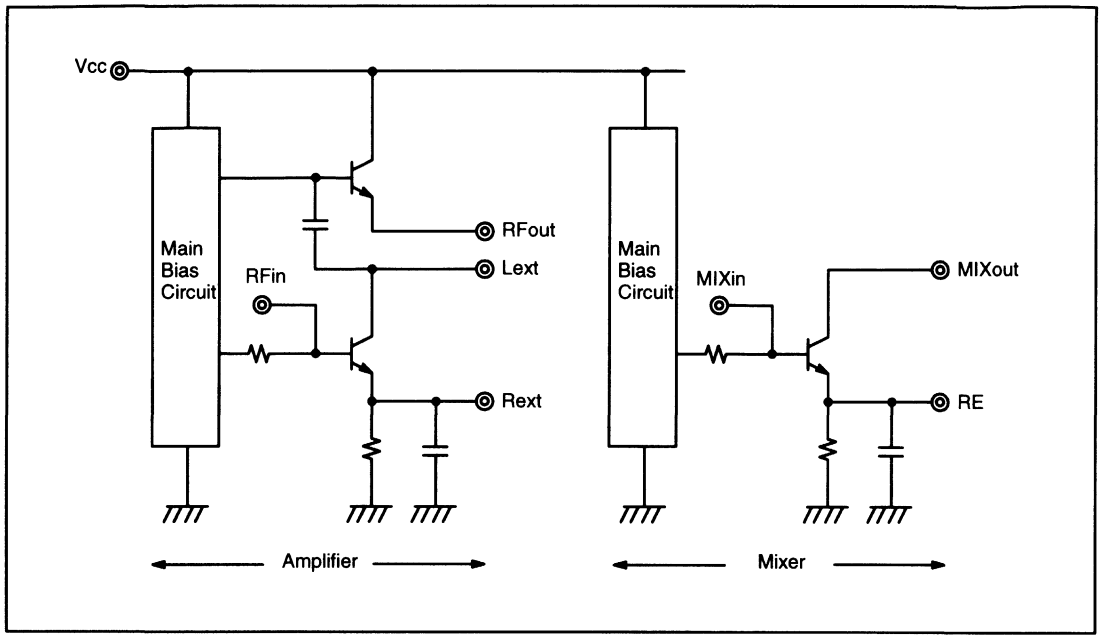
PLASTIC PACKAGE
FP-16P-M05

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

EQUIVALENT CIRCUIT



PIN DISCRIPTION

Pin No.	Pin Name	Description	Pin No.	Pin Name	Description
1	RFout	Amplifier output	9	MIXout	Mixer output
2	GND	Ground	10	GND	Ground
3	GND	Ground	11	RE	Emitter of a transistor for mixer
4	Vcc	Power supply	12		
5	NC	No connection	13	NC	No connection
6	GND	Ground	14	Rext	Emitter of a transistor for amplifier
7	GND	Ground	15	RFin	Amplifier input
8	MIXin	Mixer input	16	Lext	Amplifier load connection

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Supply Voltage	V_{CC}	2.7	3.0	5.5	V
Input Voltage	V_I	GND	–	V_{CC}	V
Operating Temperature	Ta	–40	–	+85	°C

Notes: To protect against damage by electrostatic discharge, note the following handling precautions:

- Store and transport devices in conductive containers.
- Use properly grounded workstations, tools, and equipment.
- Turn off power before inserting or removing this device into or from a socket.
- Protect leads with conductive sheet, when transporting a board mounted device.

ELECTRICAL CHARACTERISTICS

AMPLIFIER

(Vcc = +3.0V, Ta = 25°C)

Parameter	Symbol	Conditions	Target Value			Unit
			Min.	Typ.	Max.	
Supply Voltage	Vcc		2.7	3.0	5.5	V
Supply Current	Icc		–	3.0		mA
Operating Frequency	fin		–	878	1100	MHz
Gain	Gain		–	14	–	dB
Noise Figure	NF		–	2.2	–	dB
1dB Compression Point	P_{1dB}	Output	–	–1	–	dBm
Input Return Loss	RL_{IN}		–	8	–	dB
Output Return Loss	RL_{OUT}		–	10	–	dB

Remark: Electrical characterisics depend on external circuits (elements) or status of mounting.
The above characteristics are measured by the test circuit in the next page.

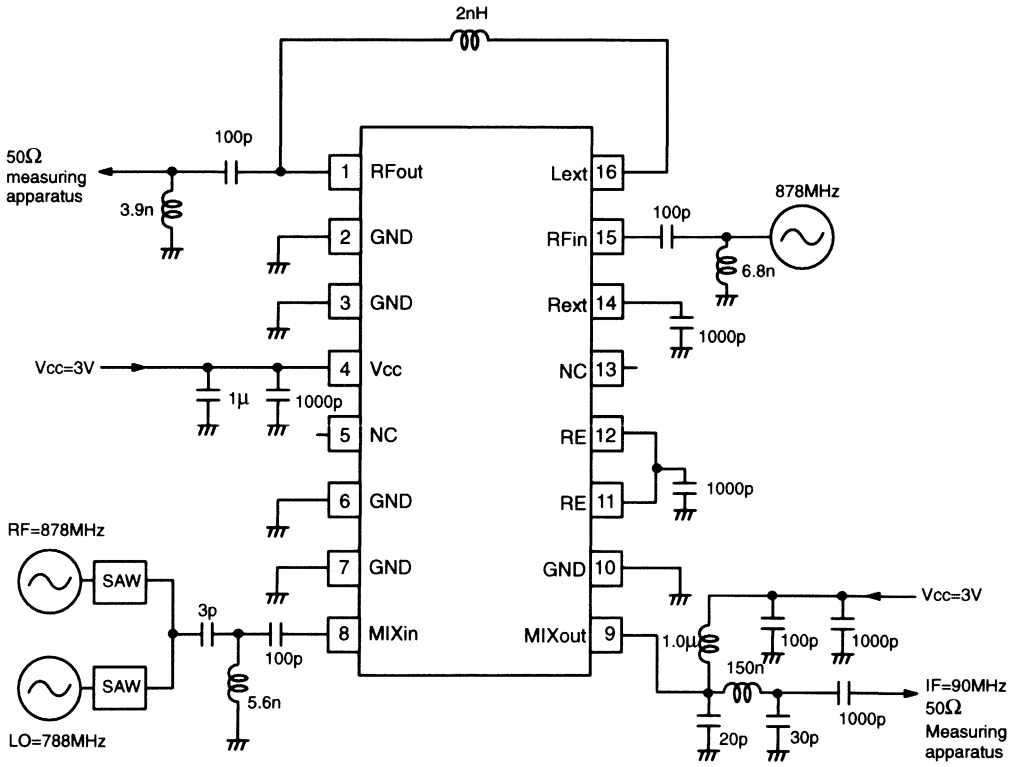
MIXER

(Vcc = +3.0V, Ta = 25°C)

Parameter	Symbol	Conditions		Target Value			Unit
				Min.	Typ.	Max.	
Supply Voltage	Vcc			2.7	3.0	5.5	V
Current Consumption	Icc			–	3.0	–	mA
Operating Frequency	fin			–	878	1100	MHz
Gain	S_{21}	Amplifier characteristics		–	9	–	dB
Conversion Gain	Gc	Mixer characteristics IF = 90MHz		–	15	–	dB
Noise Figure	NF		SSB	–	5	–	dB

Remark: Electrical characterisics depend on external circuits (elements) or status of mounting.
The above characteristics are measured by the test circuit in the next page.

MEASUREMENT CIRCUIT (EXAMPLE)



MEMO

FUJITSU SEMICONDUCTOR
DATA SHEET

DS04–23504–1E

ASSP

BIPOLAR

Transmission Mixer (1.1 GHz)

MB531

■ DESCRIPTION

The MB531 is a transmission mixer ideally suited for car telephones operating on AMPS, TACS and similar frequency bands.

Features include local buffer amp, double balanced mixer and emitter-follower circuit for high conversion gain and high isolation between Lo and Rf inputs.

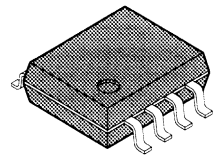
The latest silicon process technology is used to achieve a low power supply current of 13 mA.

■ FEATURES

- Wide input frequency range: up to 1.1 GHz (max)
- High conversion gain: 3.5 dB (typ) Lo: 110 MHz, –5 dBm
  RF: 800 MHz, IF output: 910 MHz
- High isolation: RF–Lo: –28 dB (typ): RF–IF: –13 dB (typ)
  Lo–RF: –37 dB (typ): Lo–IF: –23 dB (typ)

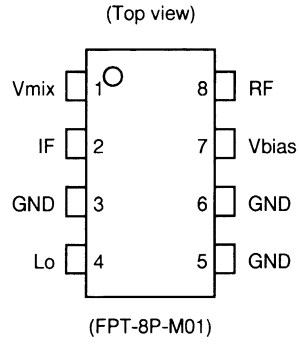
■ PACKAGE

8-pin Plastic SOP



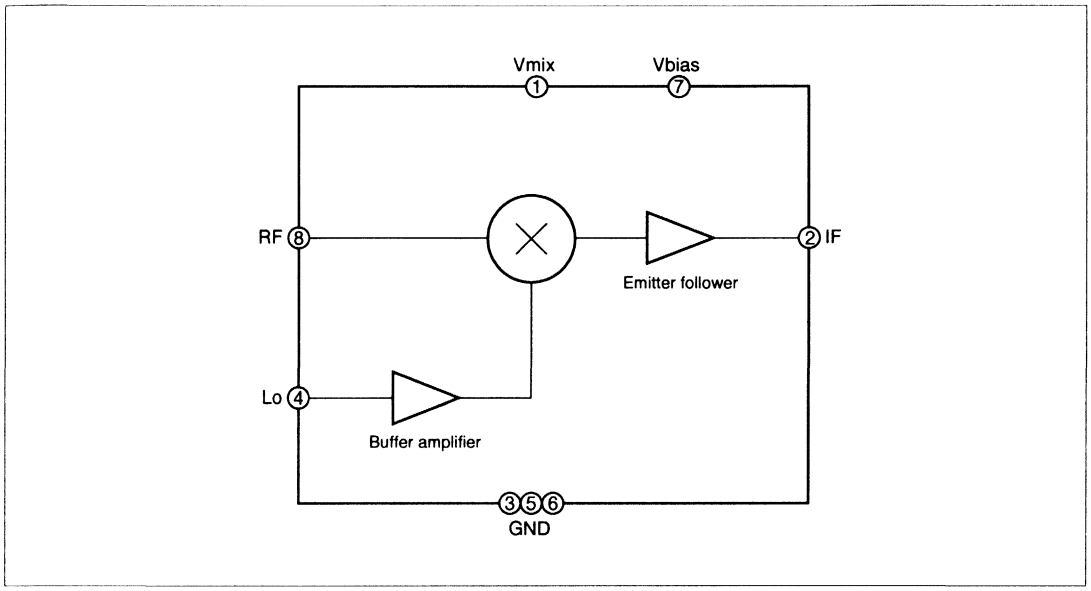
(FPT-8P-M01)

■ PIN ASSIGNMENT



Pin No.	Symbol	Pin description
1	Vmix	Power supply (for mixer circuit)
2	IF	IF output
3	GND	Ground
4	Lo	Lo signal input
5	GND	Ground
6	GND	Ground
7	Vbias	Power supply (for bias circuit)
8	RF	RF signal input

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Power supply voltage	V_{CC}	–0.5 to +7.0	V
Input voltage	V_{IN}	V_{CC}–3.5 to V_{CC}–2.5	V
Output current	I_{OUT}	10	mA
Storage temperature	Tstg	–55 to +125	°C

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Power supply voltage	V_{CC}	+4.5 to +5.0	V
Operating temperature	Ta	–40 to +85	°C

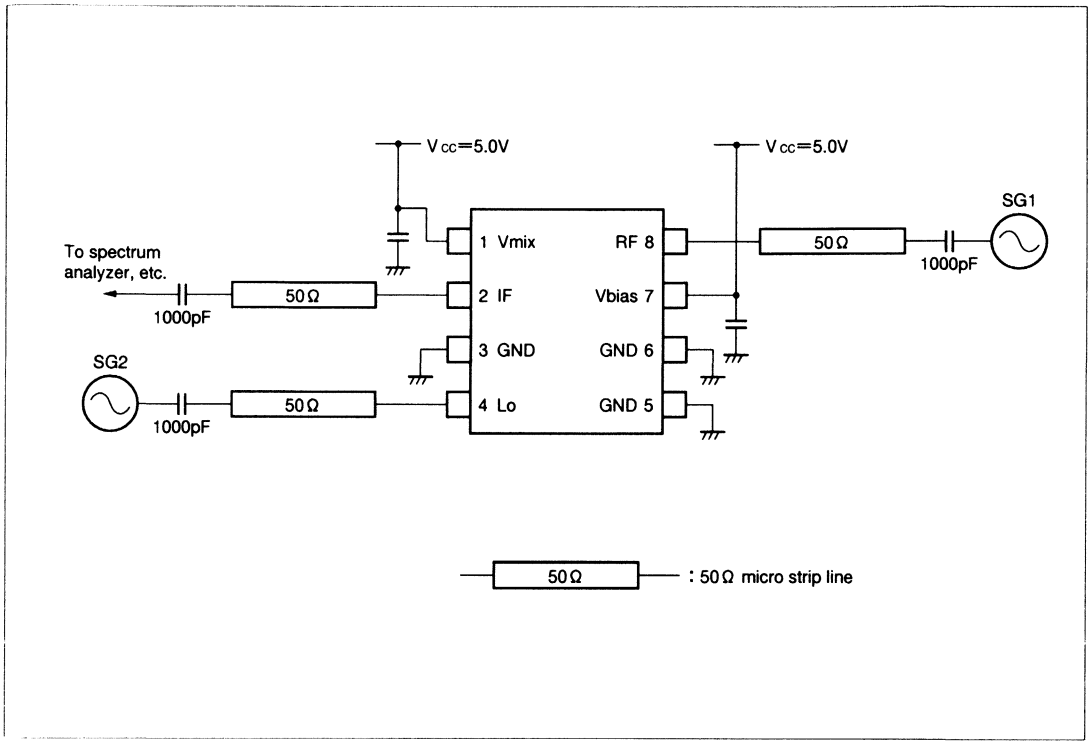
■ ELECTRICAL CHARACTERISTICS

(Vcc = 5.0V, Ta = +25°C)

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Power supply current	Icc	V_{mix} + V_{bias}	9.0	13.0	18.5	mA
Response frequency	f_{RF}	—	—	800	1100	MHz
	f_{LO}	Lo = −10 to 0 dBm	—	110	1100	MHz
Output frequency	f_{IF}	—	—	910	1100	MHz
Conversion gain	Gc	*	—	3.5	—	dB
Maximum output power	P_{OUT}		—	−7.0	—	dBm
Noise figure	NF	DSB measurement value *	—	13.5	—	dB
Third order intercept point	IP3	Input level *	—	−4	—	dBm
1 dB compression point	1dBCP	Output level *	—	−12	—	dBm
Crosstalk attenuation	$X_{RF→LO}$	*	—	−28	—	dB
	$X_{LO→RF}$		—	−37	—	dB
	$X_{RF→IF}$		—	−13	—	dB
	$X_{LO→IF}$		—	−23	—	dB
Open end voltage	V_{RF}	At Vcc = 5V. Pin function verification test (not a condition for operation)	1.5	2.0	2.5	V
	V_{LO}		1.5	2.0	2.5	V
	V_{IF}		2.7	3.2	3.7	V

*: Measurement conditions: RF = 800 MHz, Lo = 110 MHz, −5 dBm, IF = 910 MHz, Vcc = 5V, Ta = +25°C

■ MEASUREMENT CIRCUIT



■ ORDERING INFORMATION

Part Number	Package	Remarks
MB531PF	8-pin Plastic SOP (FPT-8P-M01)	

FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-23506-1E

ASSP
LOW NOISE AMPLIFIER (2 CIRCUITS)

MB54502

LOW NOISE AND CURRENT AMPLIFIER

INTRODUCTION

The Fujitsu MB54502 includes two independent amplifiers which are used for mobile telecommunication applications such as handy phones and car phones. Both of the amplifiers achieve low current consumption as well as the low noise performance. Using Fujitsu's advanced technology, MB54502 achieves an Icc of 2mA typ. respectively (total 4mA typ.).

ELECTRICAL CHARACTERISTICS

- Supply voltage 3V (typ.)
- Current consumption 2mA (typ.)
- Input frequency 1.1GHz(max.)
- Gain 14dB (typ.) *1
- Noise figure 2.2dB (typ.) *1
- 1dB compression point –6dBm (typ.) *1
- Frequency tolerance 2.5dB (typ.) *1
- Input return loss 8dB (typ.) *1
- Output return loss 8dB (typ.) *1

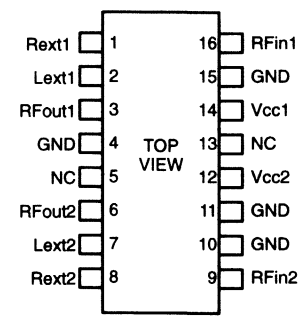
*1 : Measured by the circuit of "measurement circuit example". (fin = 820MHz)

PACKAGE

- 16-pin Plastic Shrink Small Outline Package (Suffix: -PFV)

PLASTIC PACKAGE
FP-16P-M05

PIN ASSIGNMENT



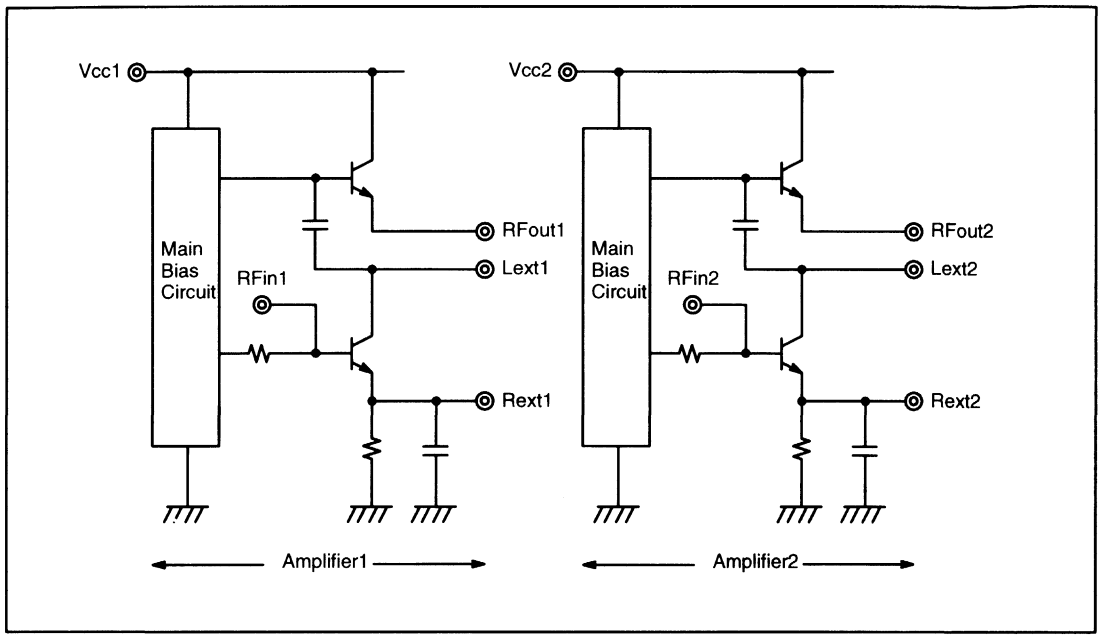
ABSOLUTE MAXIMUM RATINGS

Parameters	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.5 to 7.0	V
Output Voltage	V_O	–0.5 to V_{CC}+0.5	V
Output Current	I_O	0 to 10	mA
Storage Temperature	T_{STG}	–55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

EQUIVALENT CIRCUIT



PIN DISCRIPTION

Pin No.	Pin Name	Description	Pin No.	Pin Name	Description
1	Rext1	Emitter (amplifier 1)	9	RFin2	Input (amplifier 2)
2	Lext1	Load connection (amplifier 1)	10	GND	Ground
3	RFout1	Output (amplifier 1)	11	GND	Ground
4	GND	Ground	12	Vcc2	Power supply (amplifier 2)
5	NC	No connection	13	NC	No connection
6	RFout2	Output (amplifier 2)	14	Vcc1	Power supply (amplifier 1)
7	Lext2	Load connection (amplifier 2)	15	GND	Ground
8	Rext2	Emitter (amplifier 2)	16	RFin1	Input (amplifier 1)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Supply Voltage	Vcc	2.7	3.0	5.5	V
Input Voltage	V_I	GND	–	Vcc	V
Operating Temperature	Ta	–40	–	+85	°C

Notes: To protect against damage by electrostatic discharge, note the following handling precautions:

- Store and transport devices in conductive containers.
- Use properly grounded workstations, tools, and equipment.
- Turn off power before inserting or removing this device into or from a socket.
- Protect leads with conductive sheet, when transporting a board mounted device.

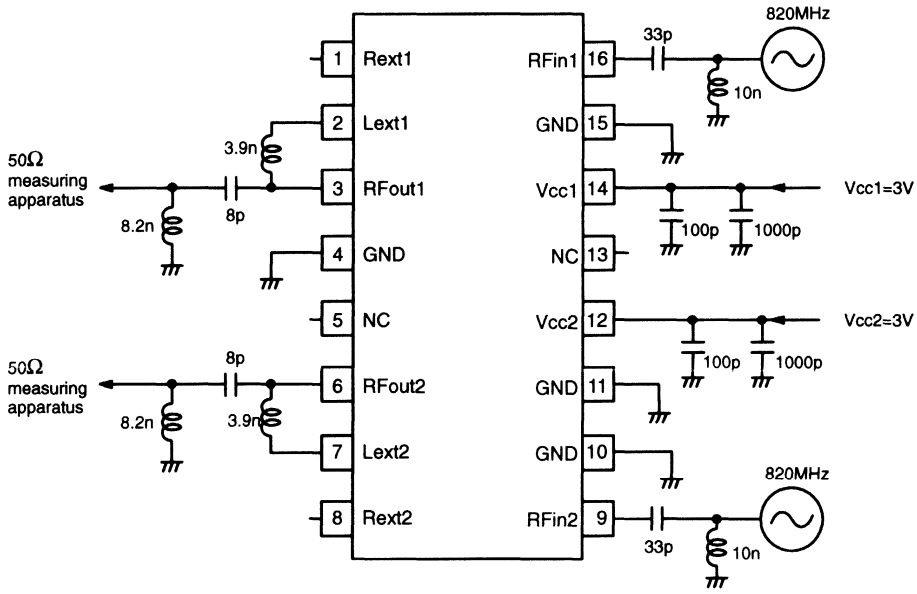
ELECTRICAL CHARACTERISTICS

(Vcc1 = +3.0V, Vcc2=0.0V, Ta = 25°C
or Vcc1 = 0.0V, Vcc2=+3.0V, Ta = 25°C)

Parameter	Symbol	Conditions	Target Value			Unit
			Min.	Typ.	Max.	
Supply Voltage	Vcc		2.7	3.0	5.5	V
Supply Current	Icc	1 amplifier active	–	2.0	–	mA
Operating Frequency	fin		–	820	1100	MHz
Gain	Gain		–	14	–	dB
Noise Figure	NF		–	2.2	–	dB
1dB Compression Point	P_{1dB}	Output	–	–6	–	dBm
Amplitude Tolerance	–	820 ± 50 MHz	–	2.5	–	dB
Input Return Loss	RL_{IN}		–	8	–	dB
Output Return Loss	RL_{OUT}		–	8	–	dB

Remark: Electrical characterisics depend on external circuits (elements) or status of mounting.
The above characteristics are measured by the test circuit in the next page.

MEASUREMENT CIRCUIT (EXAMPLE)



MEMO

FUJITSU SEMICONDUCTOR
DATA SHEET

DS04–23904–3E

ASSP

BIPOLAR

Low-Noise AMP for High-Frequency Bands (to 1.6 GHz)

MB539

■ DESCRIPTION

The MB539 is a low-noise amplifier IC (integrated circuit) for high-frequency bands, designed for use in mobile communications systems including portable phones.

The low-noise, high-gain features of the MB539 provide exceptional stability. The IC is capable of operating at frequencies as high as 1.6 GHz.

The latest FUJITSU process technology is used to achieve low power consumption of 9.0 mA (typ).

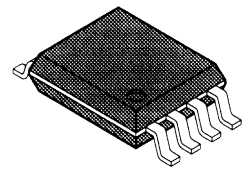
■ FEATURES

- Operating voltage : 5 V (typ.)
- Current consumption : 9.0 mA (typ.)
- Operating frequency : 1.6 GHz (max.)
- Gain : 11 dB
- Noise figure : 4 dB
- Maximum output power : –2 dBm
- 1 dB compression point : –17 dBm (input)
  : –7 dBm (output)
- Third order intercept point : –5 dBm (input)
  : 6 dBm (output)

} at f_{RF} = 1.6 GHz

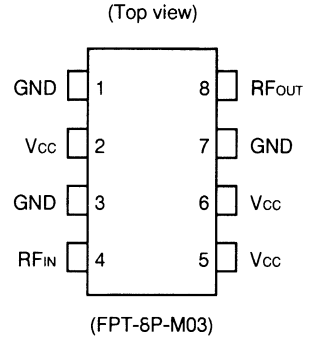
■ PACKAGE

8-pin Plastic SSOP



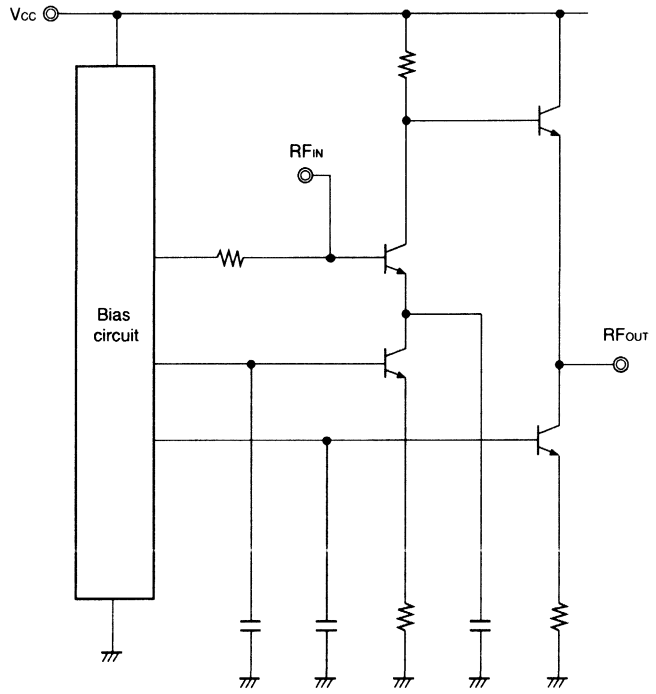
(FPT-8P-M03)

■ PIN ASSIGNMENT



Pin No.	Symbol	Pin description
1	GND	GND
2	Vcc	Power supply
3	GND	GND
4	RFIN	RF AMP input
5	Vcc	Power supply
6	Vcc	Power supply
7	GND	GND
8	RFOUT	RF AMP output

■ EQUIVALENT CIRCUIT DIAGRAM



(Total 9.0 mA)

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit	Remarks
Power supply voltage	V_{CC}	−0.5 to +7.0	V	
Output voltage	V_O	−0.5 to V_{CC}+0.5	V	
Input voltage	V_I	−0.5 to V_{CC}+0.5	V	
Output current	I_O	0 to 10	mA	
Storage temperature	Tstg	−55 to +125	°C	

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
Power supply voltage	V_{CC}	4.5	5.0	5.5	V	
Input voltage	V_I	GND	—	V_{CC}	V	
Operating Temperature	Ta	−40	—	+85	°C	

Note: The user should take full precautions to prevent accidental damage from static electricity.

- For storage or transport, place in a conductive case.
- Before handling, verify that all operators, fixtures and tools are free from electrification (grounded), and use an operating platform of grounded conductive sheeting.
- Always switch off the power before this device is inserted into or removed from sockets.
- When handling or transporting circuit boards in which this device is mounted, leads must be protected by conductive sheeting.

■ ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
Power supply voltage	V_{CC}	4.5	5.0	5.5	V	
Power supply current	I_{CC}	—	9.0	12.0	mA	V_{CC} = 5.0V
Operating frequency	fmax	—	1100	1600	MHz	

1. f_{RF} = 1100 MHz

(V_{CC} = 5.0V, Ta = +25°C)

Parameter	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
Gain	G_{ain}	—	16.0	—	dB	
Noise figure	NF	—	2.5	—	dB	
Maximum output power	P_{OUT}	—	0.0	—	dBm	
1 dB compression point	1dB CP	—	−19.0	—	dBm	Input
		—	−3.0	—	dBm	Output
Intercept point	IP_3	—	−8.0	—	dBm	Input
		—	8.0	—	dBm	Output
In-Out isolation	Iso	—	−25.0	—	dB	

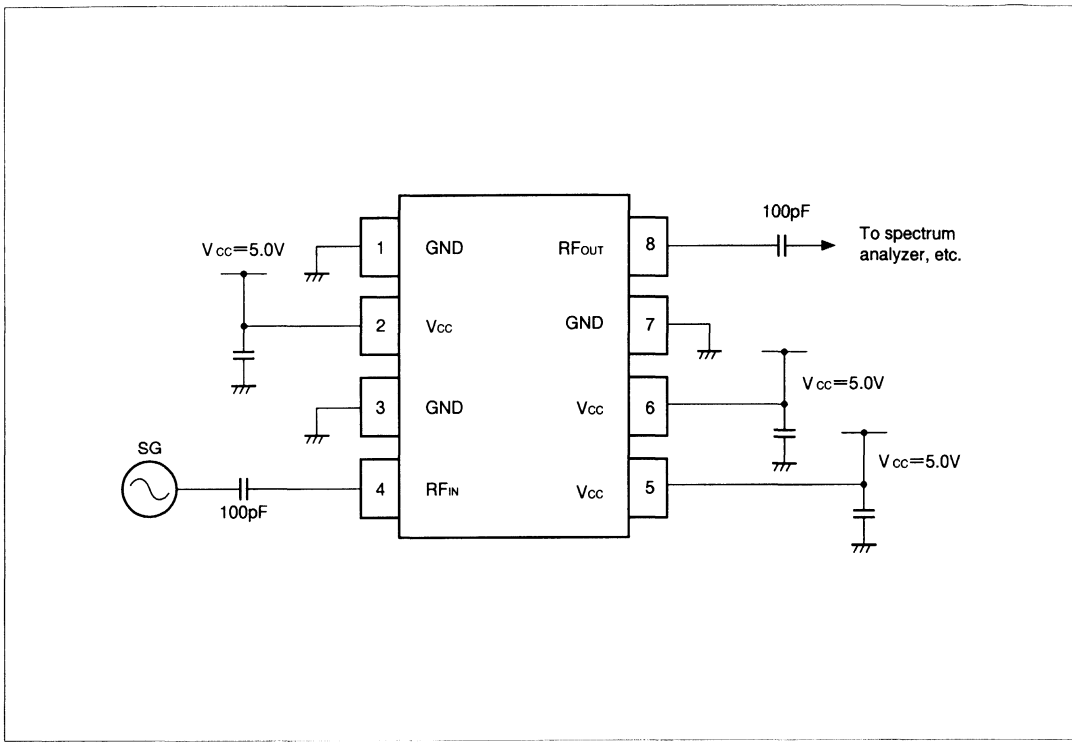
2. f_{RF} = 1600 MHz

(V_{CC} = 5.0V, Ta = +25°C)

Parameter	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
Gain	G_{ain}	—	11.0	—	dB	
Noise figure	NF	—	4.0	—	dB	
Maximum output power	P_{OUT}	—	−2.0	—	dBm	
1 dB compression point	1dB CP	—	−17.0	—	dBm	Input
		—	−7.0	—	dBm	Output
Intercept point	IP_3	—	−5.0	—	dBm	Input
		—	6.0	—	dBm	Output
In-Out isolation	Iso	—	−20.0	—	dB	

Note: • Electrical characteristics may vary depending on the use of external elements or mounting conditions.
• The above characteristics represent data obtained with the "■ MEASUREMENT CIRCUIT."

■ MEASUREMENT CIRCUIT



■ ORDERING INFORMATION

Part Number	Package	Remarks
MB539PFV	8-pin Plastic SSOP (FPT-8P-M03)	

FUJITSU SEMICONDUCTOR
DATA SHEET

DS04–23507–1E

ASSP

HIGH-POWER AMPLIFIER

MB54503

INTRODUCTION

The Fujitsu MB54503 is a high-power amplifier which is used for mobile telecommunication systems such as handy phones and car phones. This device is ideally suitable for power amplifier driver.
Using Fujitsu's advanced technology, MB54503 achieves an Icc of 26.0mA (typ.).

ELECTRICAL CHARACTERISTICS

- Supply voltage 3.6V (typ.)
- Current consumption 26mA (typ.)
- Input frequency 1.1GHz(max.)
- Gain 25dB (typ.) *1
- Output level (@Pin=–8dBm) +13dBm (typ.) *1
- Input return loss 14dB (typ.) *1
- Output return loss 6dB (typ.) *1

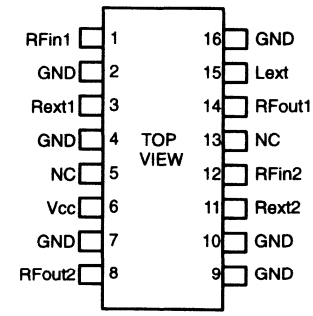
*1 : Measured by the circuit of "measurement circuit example". (fin = 933MHz)

PACKAGE

- 16-pin Plastic Shrink Small Outline Package (Suffix: -PFV)

PLASTIC PACKAGE
FP-16P-M05

PIN ASSIGNMENT



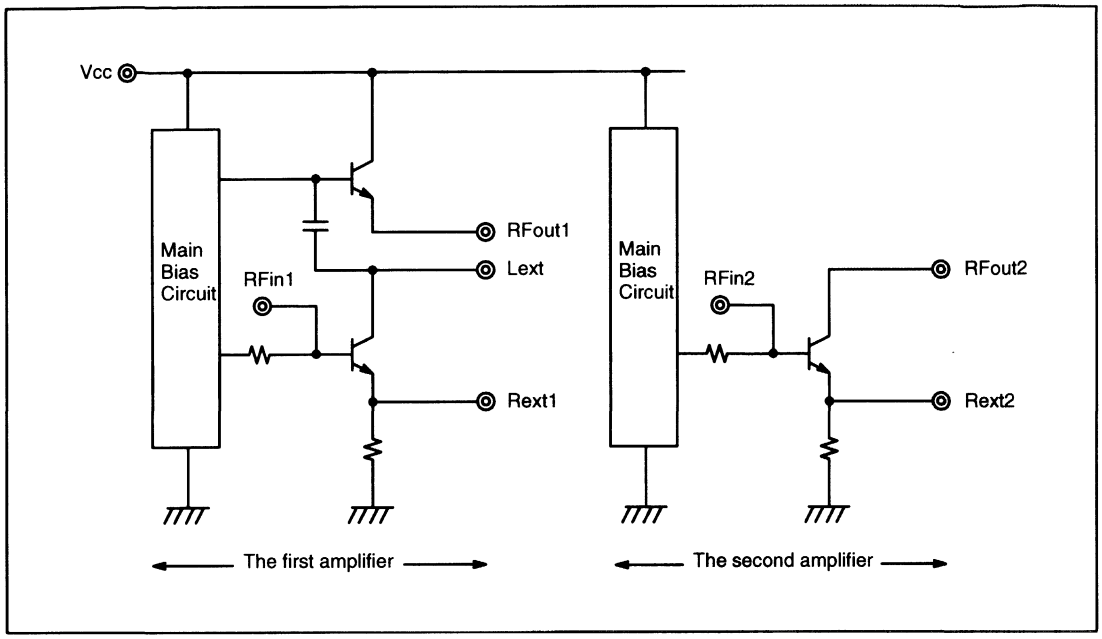
ABSOLUTE MAXIMUM RATINGS

Parameters	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.5 to 7.0	V
Output Voltage	V_O	–0.5 to V_{CC}+0.5	V
Output Current	I_O	0 to 10	mA
Storage Temperature	T_{STG}	–55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

EQUIVALENT CIRCUIT



PIN DISCRIPTION

Pin No.	Pin Name	Description	Pin No.	Pin Name	Description
1	RFin1	The first amplier input	9	GND	Ground
2	GND	Ground	10	GND	Ground
3	Rext1	Emitter for the first amplifier	11	Rext2	Emitter for the second amplifier
4	GND	Ground	12	RFin2	The second amplier input
5	NC	No connection	13	NC	No connection
6	Vcc	Power supply	14	RFout1	The first amplifier output
7	GND	Ground	15	Lext	Load connecting for the first amplifier
8	RFout2	The second amplifier output	16	GND	Ground

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Supply Voltage	Vcc	2.7	3.6	5.0	V
Input Voltage	V_I	GND	–	Vcc	V
Operating Temperature	Ta	–40	–	+85	°C

Notes: To protect against damage by electrostatic discharge, note the following handling precautions:

- Store and transport devices in conductive containers.
- Use properly grounded workstations, tools, and equipment.
- Turn off power before inserting or removing this device into or from a socket.
- Protect leads with conductive sheet, when transporting a board mounted device.

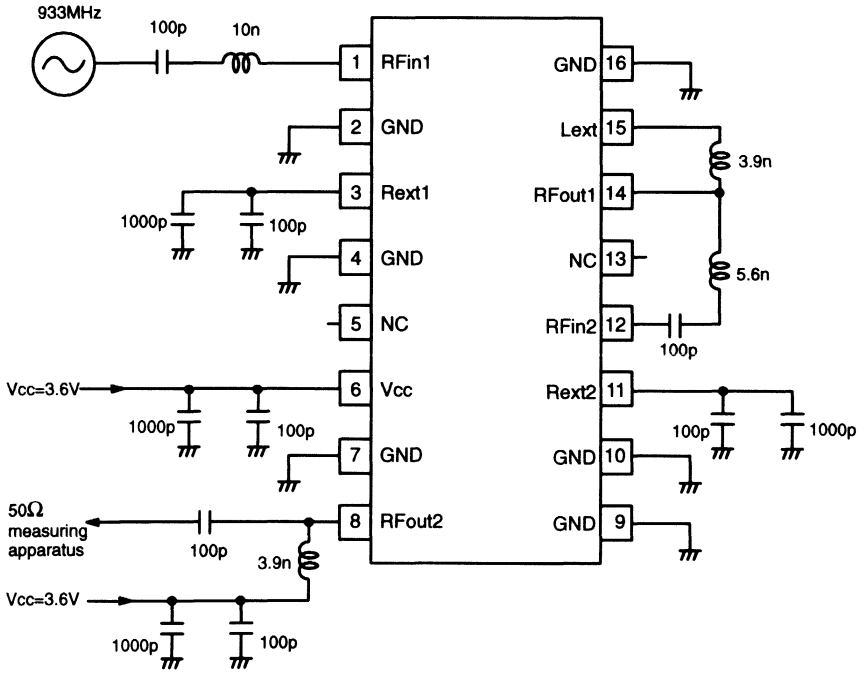
ELECTRICAL CHARACTERISTICS

(Vcc = +3.6V, Ta = 25°C)

Parameter	Symbol	Conditions	Target Value			Unit
			Min.	Typ.	Max.	
Supply Voltage	Vcc		2.7	3.6	5.0	V
Supply Current	Icc		–	26	–	mA
Operating Frequency	fin		–	933	1100	MHz
Gain	Gain		–	25	–	dB
Output Power	Pout	Pin = –8dBm	–	+13	–	dBm
Input Return Loss	RLIN		–	14	–	dB
Output Return Loss	RLOUT		–	6	–	dB

Remark: Electrical characterisics depend on external circuits (elements) or status of mounting.
The above characteristics are measured by the test circuit in the next page.

MEASUREMENT CIRCUIT (EXAMPLE)



MEMO

FUJITSU SEMICONDUCTOR
DATA SHEET

DS04–23509–1E

ASSP for Telephone

BIPOLAR

Quadrature Modulator IC

(With 1.0 GHz Up-converter)

MB54609

■ DESCRIPTION

The MB54609 is an intermediate-frequency (IF) quadrature modulator IC incorporating a 1.0-GHz up-converter optimized for use in digital mobile telecommunication systems such as GSM and PDC (Personal Digital Cellular).

The MB54609 incorporates a quadrature modulator for IF modulation, a transmission up-convert mixer, and a F/F type phase shifter as well, capable of handing IFs in a broad band.

In addition, the MB54609 operates at a low power supply voltage of 3.0 V and a low power supply current of 18 mA (both as typical values), contributing to saving the power consumption of the device.

■ FEATURES

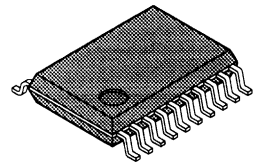
- Incorporating a high-performance transmission mixer covering the entire frequency band of up to 800 MHz used for PDC services (Maximum output frequency of 1.1 GHz)
  Maximum output frequency: 1.1 GHz, Output level: −9 dBm (typical)

- Externally connecting the quadrature modulator with the transmission mixer, allowing a bandpass filter (BPF) to be inserted in between
  The quadrature modulator output can drive a 50 Ω load.

(Continued)

■ PACKAGE

20-pin Plastic SSOP

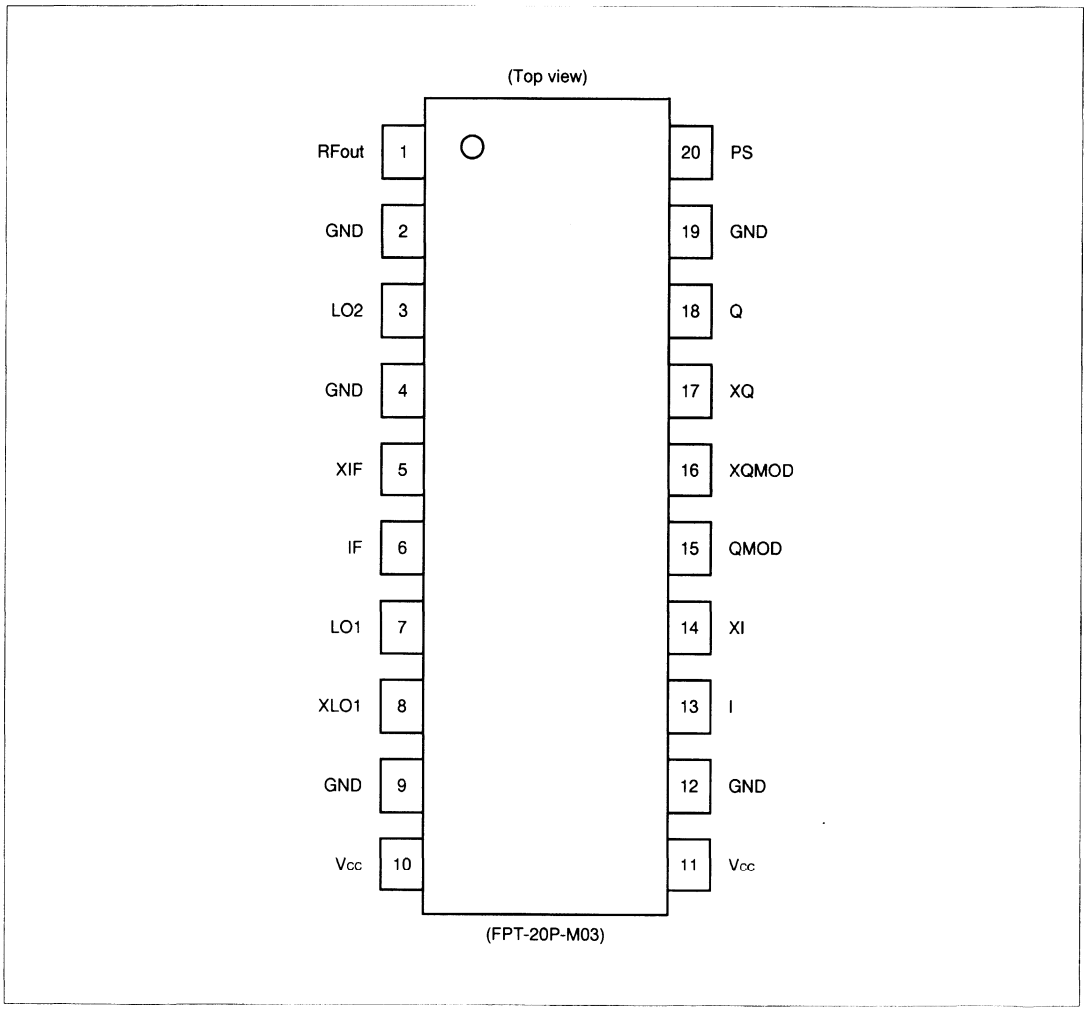


(FPT-20P-M03)

(Continued)

- Flip-flop phase shifter capable of handling intermediate frequencies in the broad band (100 to 800 MHz)
- Operation at low voltage: 2.7 to 3.0 to 3.3 V
- Low current consumption
  During operating: 18.0 mA (typical)
  In power save mode: 0.6 mA (typical)
- Operating temperature range: Ta = −20 to +85°C

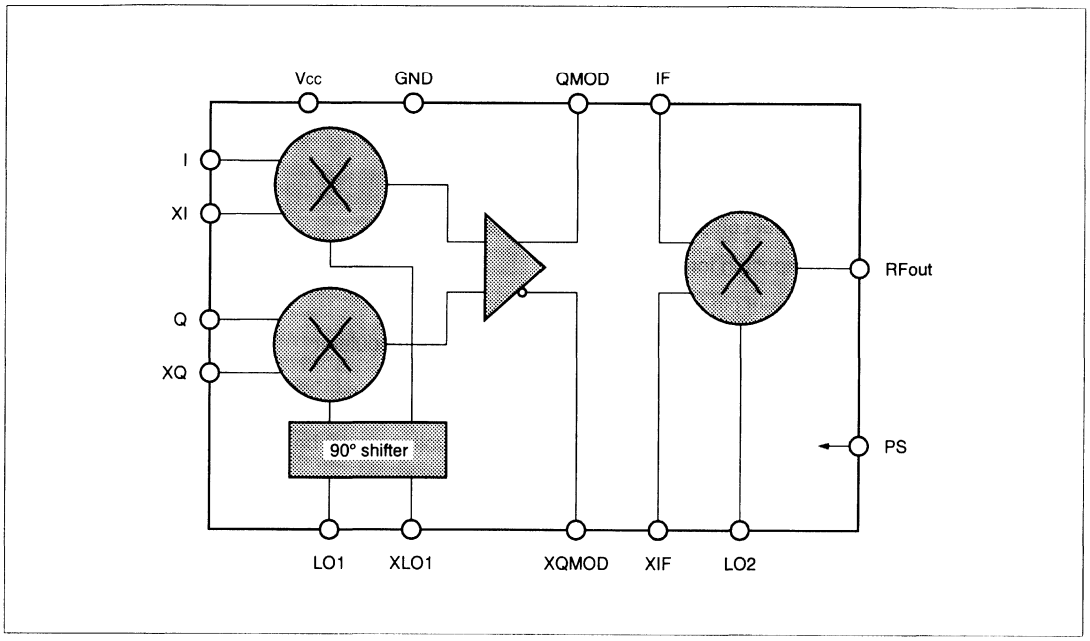
■ PIN ASSIGNMENT



■ PIN DESCRIPTION

Pin no.	Pin name	Function	
1	RFout	Up-converter output pin	
2	GND	GND pin	
3	LO2	LO input pin for mixer	
4	GND	GND pin	
5	XIF	IF input complementary pin for mixer	
6	IF	IF input pin for mixer	
7	LO1	LO input pin for quadrature modulator	
8	XLO1	LO input complementary pin for quadrature modulator	
9	GND	GND pin	
10	Vcc	Power supply pin	Power supply voltage must be applied to both pins.
11	Vcc	Power supply pin	
12	GND	GND pin	
13	I	Baseband input (I) pin	
14	XI	Baseband input (I) complementary pin	
15	QMOD	Quadrature modulator IF output pin	
16	XQMOD	Quadrature modulator IF output complementary pin	
17	XQ	Baseband input (Q) complementary pin	
18	Q	Baseband input (Q) pin	
19	GND	GND pin	
20	PS	Power save mode control pin	

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Remarks
Power supply voltage	V_{CC}	−0.5 to 5.0	V	
Output voltage	V_O	−0.5 to V_{CC} + 0.5	V	
Input voltage	V_I	−0.5 to V_{CC} + 0.5	V	
Open collector applied voltage	V_{OC}	V_{CC} ± 0.3 (−0.5 to 5.0)	V	RFout pin Do not leave this pin open.
Output current	I_O	±10	mA	
Storage temperature	Tstg	−55 to +125	°C	

Note: Although the MB54609 contains an antistatic element to prevent electrostatic breakdown and the circuitry has been improved in electrostatic protection, observe the following precautions when handling the device:

- When storing or carrying the device, put it in a conductive case.
- Before handling the device, check that the jigs and tools to be used have been uncharged (grounded) as well as yourself. Use a conductive sheet on the working bench.
- Before fitting the device into or removing it from the socket, turn the power supply off.
- When handling (such as transporting) the MB54609 mounted board, protect the leads with a conductive sheet.

Precaution: Exceeding any of the above absolute maximum ratings may cause permanent damage to the LSI. For normal operation, the device should be used under the recommended operating conditions. Exceeding any of the recommended conditions may adversely affect LSI reliability.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
Power supply voltage	V_{CC}	2.7	3.0	3.3	V	
Input voltage	V_I	GND	—	V_{CC}	V	
Open collector applied voltage	V_{OC}	V_{CC} – 0.2	—	V_{CC} + 0.2	V	RFout pin. Do not leave this pin open.
Operating temperature	Ta	–20	—	+85	°C	

■ ELECTRICAL CHARACTERISTICS

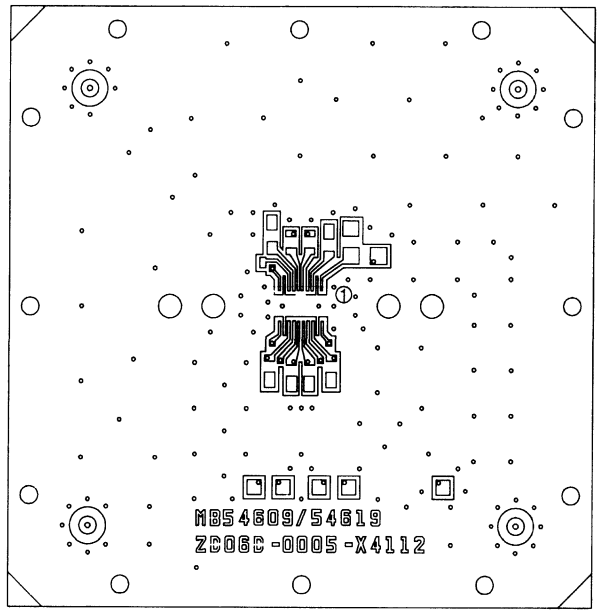
(V_{CC} = 3.0 V, Ta = +25°C)

Parameter		Symbol	Value			Unit	Remarks	
			Min.	Typ.	Max.			
Power supply current		I_{CC}	—	18.0	23.5	mA	DC current (Input with no AC signal)	
Power supply current in power save mode		I_{CCPS}	—	0.6	0.9	mA	DC current (Input with no AC signal)	
Shifter input LO1	Operating band	f_{LO1}	100	400	800	MHz		
	Input level	P_{LO1}	–15	—	–5	dBm		
Baseband input	Operating band	f_{BB}	DC	—	10	MHz		
	Input amplitude	V_{BB}	—	—	1.2	Vpp		
	Offset voltage	V_{OS}	1.5	1.6	1.7	V	External offset voltage value	
	Offset current	I_{OS}	—	3.0	—	μA	Input Imp. converted value = 533 kΩ	
Mixer input LO2	Operating band	f_{LO2}	—	750	1100	MHz		
	Input level	P_{LO2}	—	—	0	dBm		
Mixer output RFout	Operating band	f_{RF}	—	950	1100	MHz	$f_{RF} = f_{LO2} \pm f_{LO1}/2$	
	Output level	P_{RF}	—	–9	—	dBm	—	f_{LO1} = 400 MHz (–15 dBm) f_{LO2} = 750 MHz (–5 dBm) f_{RF} = 950 MHz output QMOD/Mix direct connection V_{BB} = 1 Vpp
Modulation precision	Amplitude deviation	A_{ERR}	—	1.3	—	%	RMS value	
	Phase deviation	P_{ERR}	—	0.82	—	deg.	RMS value	
	Vector error	V_{ERR}	—	1.9	—	%	RMS value	
Carrier suppression		CS	—	–40	–30	dBc	With external offset unadjusted	

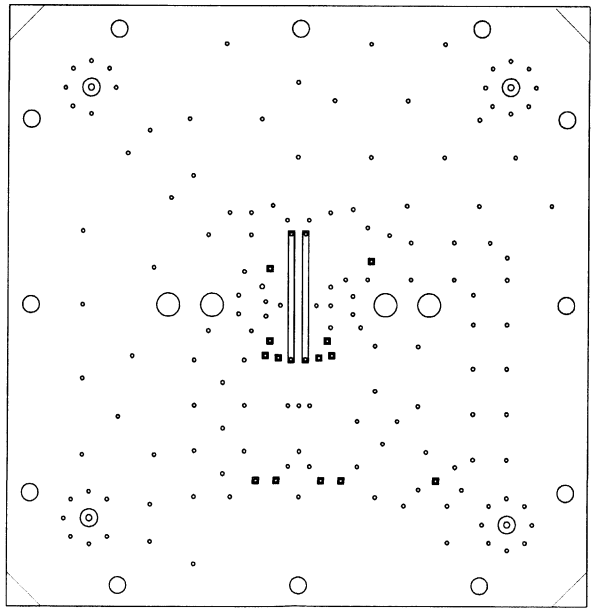
■ EVALUATION BOARD (Reference Example)

- Material: BT resin BT-HL870 (Dielectric constant [1 MHz] = 3.4 to 3.6)
- Thickness: 4 layers, 1.6 mm (Copper thickness: External layer = 18 μm, Internal layer = 70 μm)
- Plating: electroless gold plating

- **Layer 1 (front surface)**



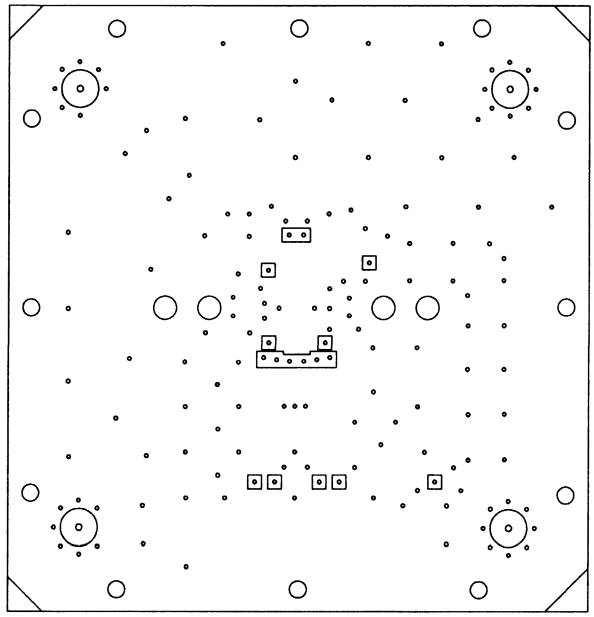
- **Layer 2**



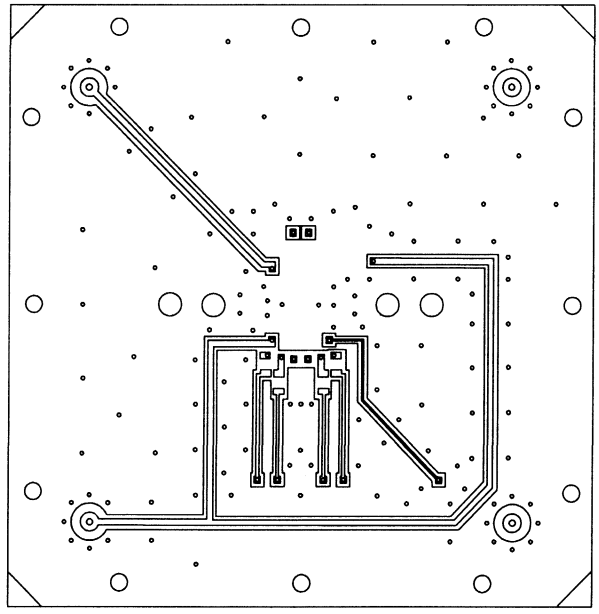
(Continued)

(Continued)

- **Layer 3**



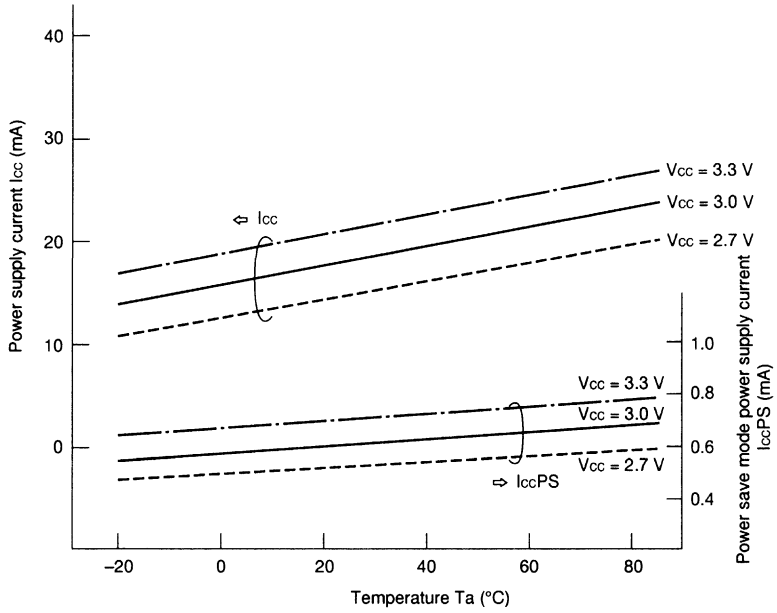
- **Layer 4 (rear surface)**



■ MEASUREMENT DATA (Reference Values)

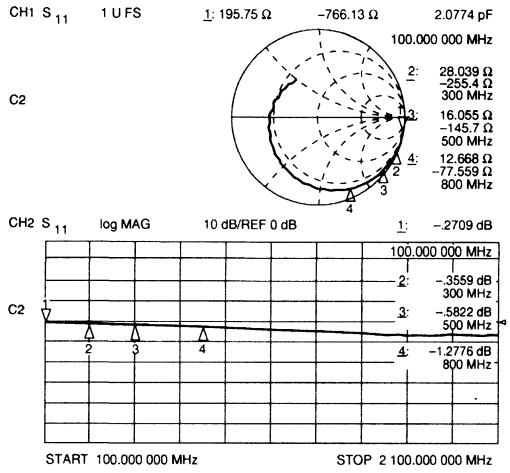
* Application-common characteristics

• **DC characteristics (test circuit 1)**
@ Input with no AC signal

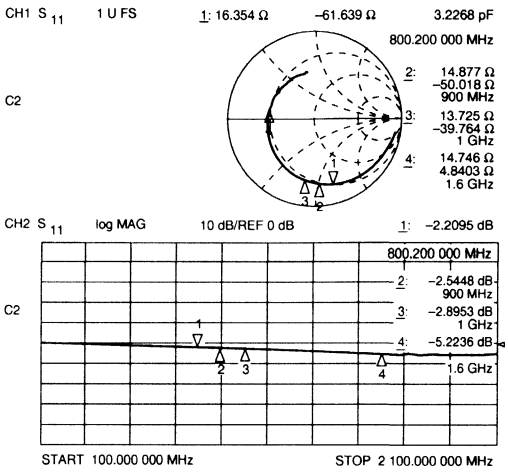


- **Input impedance (Only IC: test circuit 4)**
  @ Impedance from IC pin end

- **LO1**

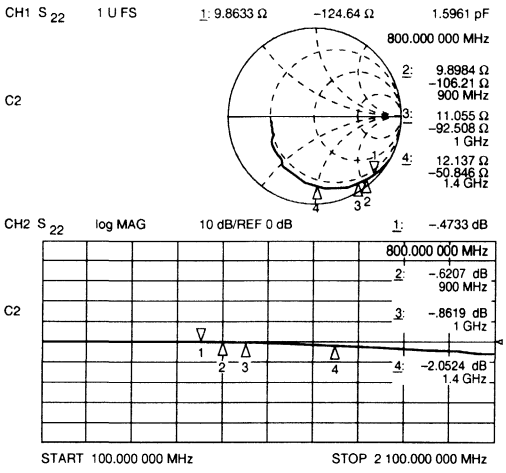


- **LO2**



- **Output impedance (Only IC: test circuit 4)**
  @ Impedance from IC pin end

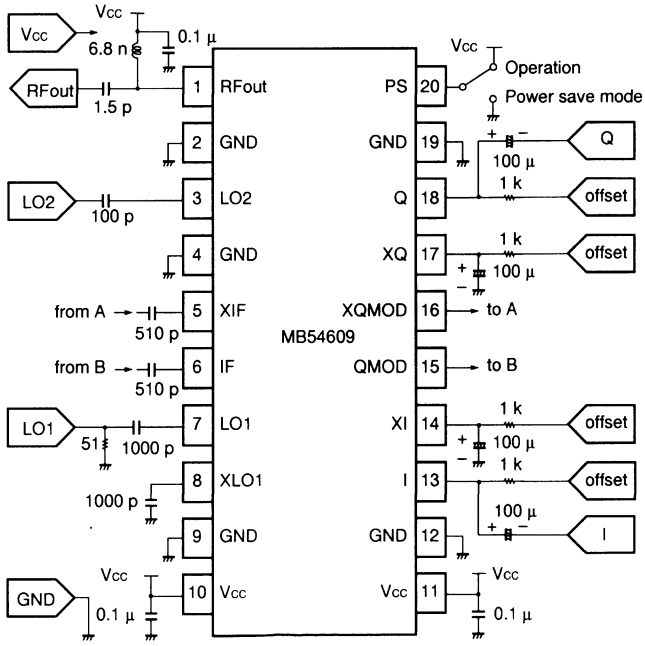
- **RFout**



■ 800-MHz PDC APPLICATION MEASUREMENT DATA (Reference Values)

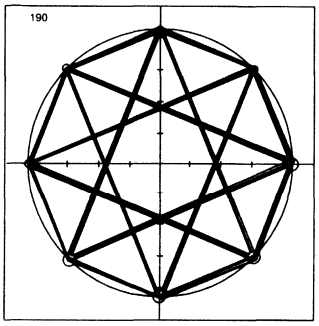
Parameter	Symbol	Measurement result	Unit	Condition	Test circuit
Baseband input signal	f_{BB}	42	kbps	π/4DQPSK, Root-Nyquist filter (α = 0.5)	—
	V_{BB}	1.0	Vpp	Single-end input	—
Shifter input signal LO1	f_{LO1}	400	MHz	—	—
	P_{LO1}	−15	dBm	—	—
Mixer input signal LO2	f_{LO2}	750	MHz	—	—
	P_{LO2}	−5	dBm	—	—
Mixer output signal RFout	f_{RF}	950	MHz	$f_{RF} = f_{LO2} + f_{LO1}/2$	—
	P_{RF}	−8.4	dBm	SSB value	1
Return loss	RL_{LO1}	−17	dB	f_{LO1} = 400 MHz	3
	RL_{LO2}	−2	dB	f_{LO2} = 750 MHz	
	RL_{RF}	−12	dB	f_{RF} = 950 MHz	
Modulation precision	A_{ERR}	1.3	%	RMS Magnitude Error	2
	P_{ERR}	0.82	deg.	RMS Phase Error	
	V_{ERR}	1.9	%	RMS Vector Error	
Carrier suppression	CS	−34.5	dBc	—	2

- **External circuit constants (with the IC mounted on the evaluation board)**

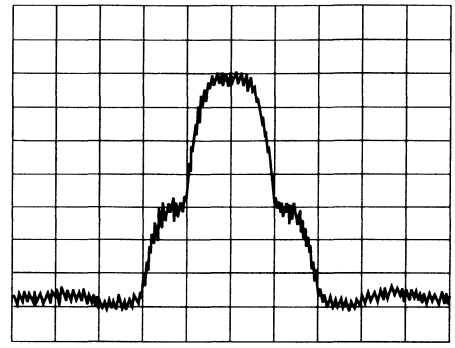


- **Modulation precision and output spectrum (test circuit 2)**
  @ Baseband signal: π/4 DQPSK, 42 kbps, 1.0 Vpp, PN 15, Root-Nyquist filter α = 0.5
  Input signals: LO1 = 400 MHz, –15 dBm; LO2 = 750 MHz, –5 dBm
  Output signal: RFout = 950 MHz

- **Modulation precision**



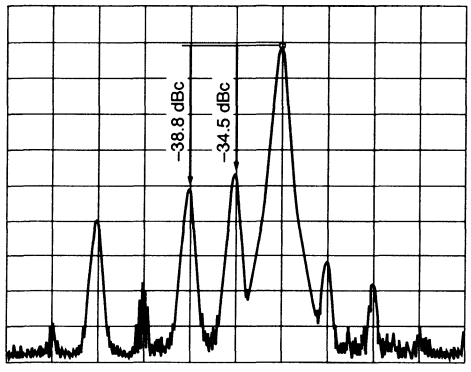
- **Output spectrum**



CENTER = 950 MHz
SPAN = 200 kHz
RBW = 3 kHz VBW = 100 Hz SWP = 3 s
ATT = 10 dB
REF = 0 dBm 10 dB/div.

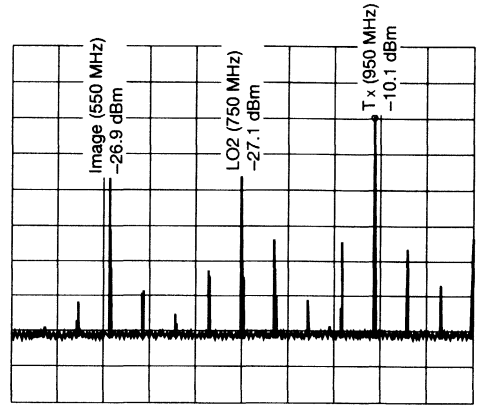
- **Spectrum (test circuit 2)**
  @ Baseband signal: π/4 DQPSK, 42 kbps, 1.0 Vpp, 0000, Root-Nyquist filter α = 0.5
  Input signals: LO1 = 400 MHz, –15 dBm; LO2 = 750 MHz, –5 dBm
  Output signal: RFout = 950 MHz

- **Span = 240 kHz**



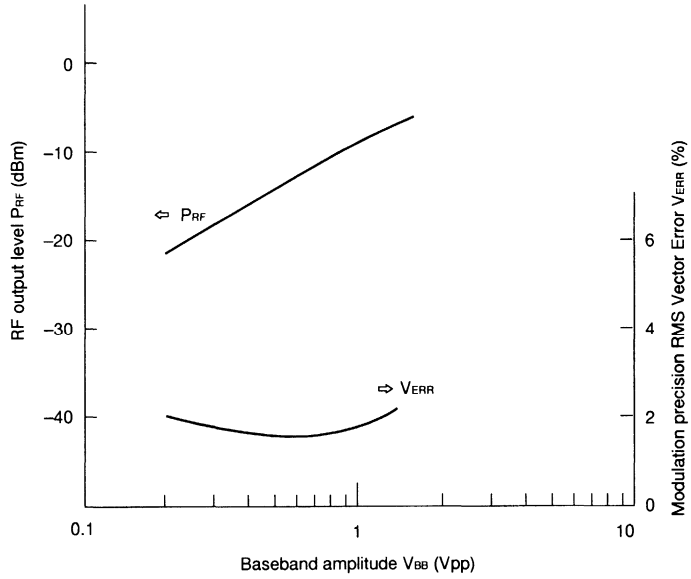
CENTER = 950 MHz
SPAN = 26.2 kHz
RBW = 300 Hz VBW = 300 Hz SWP = 1.3 s
ATT = 10 dB
REF = 0 dBm 10 dB/div.

- **Span = 700 MHz**



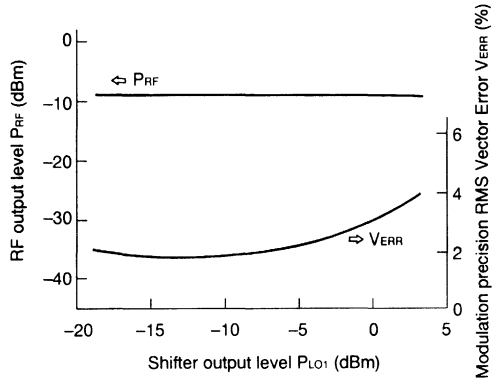
CENTER = 750 MHz
SPAN = 700 MHz
RBW = 1 MHz VBW = 3 kHz SWP = 1.1 s
ATT = 10 dB
REF = 10 dBm 10 dB/div.

- **RF output level dependent on baseband amplitude (P_{RF}: test circuit 1, Modulation precision: test circuit 2)**
  @ Baseband signal of test circuit 2: π/4 DQPSK, 42 kbps, 1.0 Vpp, PN 15, Root-Nyquist filter α = 0.5
  Input signals of test circuits 1 and 2: LO1 = 400 MHz, –15 dBm; LO2 = 750 MHz, –5 dBm
  Output signals of test circuits 1 and 2: RFout = 950 MHz

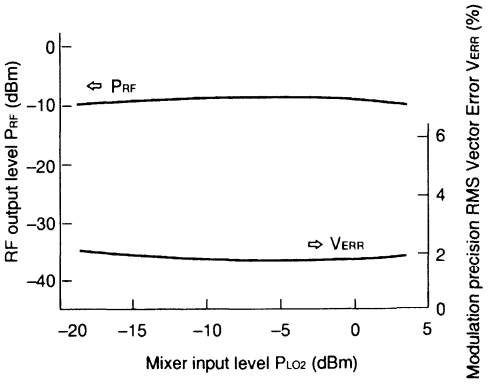


- **RF output level dependent on LO1 and LO2 input levels (P_{RF}: test circuit 1, Modulation precision: test circuit 2)**
  @ Baseband signal of test circuit 2: π/4 DQPSK, 42 kbps, 1.0 Vpp, PN 15, Root-Nyquist filter α = 0.5
  Input signals of test circuits 1 and 2: LO1 = 400 MHz, –15 dBm; LO2 = 750 MHz, –5 dBm
  Output signals of test circuits 1 and 2: RFout = 950 MHz

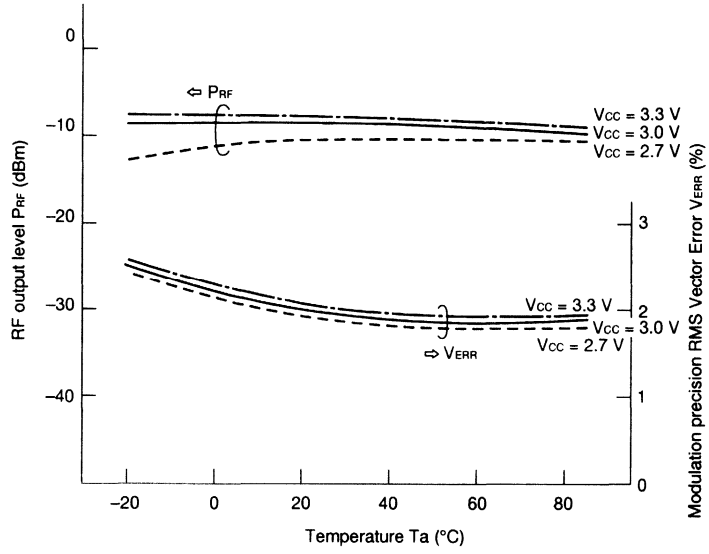
- **RF output level dependent on LO1 input level (@P_{LO2} = –5 dBm)**



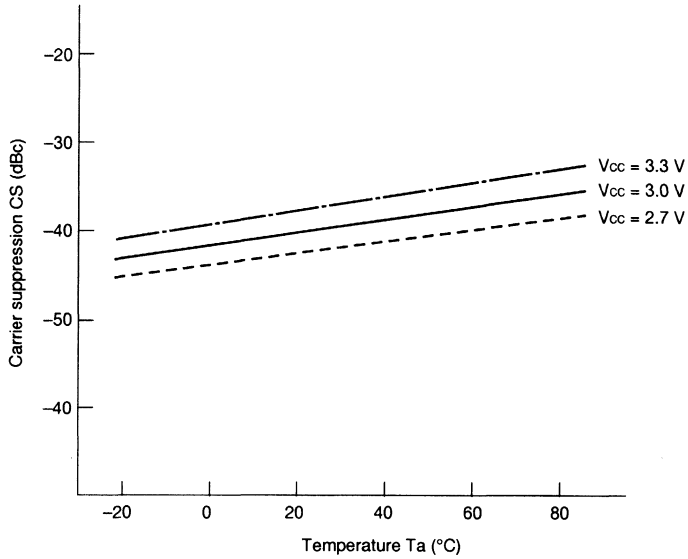
- **RF output level dependent on LO2 input level (@P_{LO1} = –15 dBm)**



• **RF output level dependent on temperature (P_{RF}: test circuit 1, Modulation precision: test circuit 2)**
@ Baseband signal of test circuit 2: π/4 DQPSK, 42 kbps, 1.0 Vpp, PN 15, Root-Nyquist filter α = 0.5
Input signals of test circuits 1 and 2: LO1 = 400 MHz, –15 dBm; LO2 = 750 MHz, –5 dBm
Output signals of test circuits 1 and 2: RFout = 950 MHz

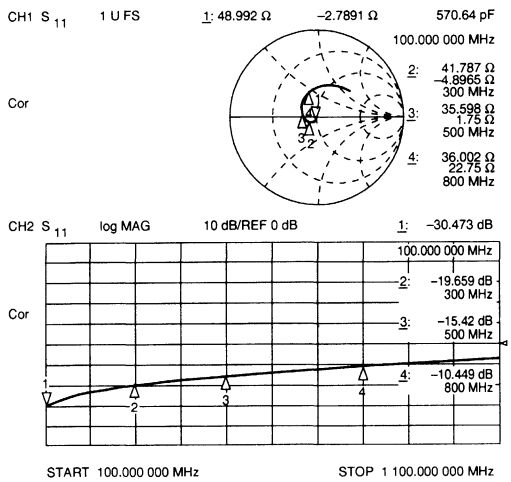


• **Carrier suppression dependent on temperature (test circuit 2)**
@ Baseband signal: π/4 DQPSK, 42 kbps, 1.0 Vpp, 0000, Root-Nyquist filter α = 0.5
Input signals: LO1 = 400 MHz, –15 dBm; LO2 = 750 MHz, –5 dBm
Output signal: RFout = 950 MHz

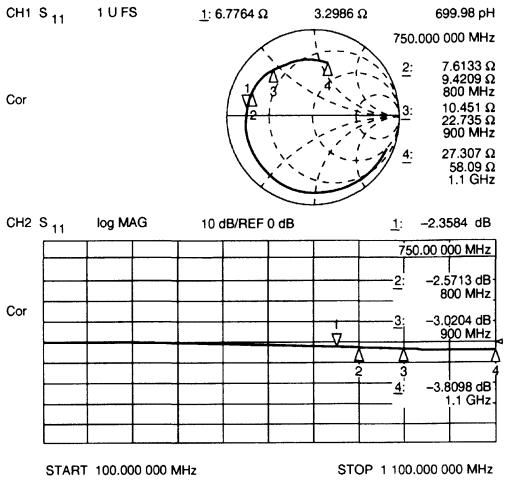


- **Input impedance (with components mounted: test circuit 3)**
  @ Impedance including external components and evaluation board

- **LO1**

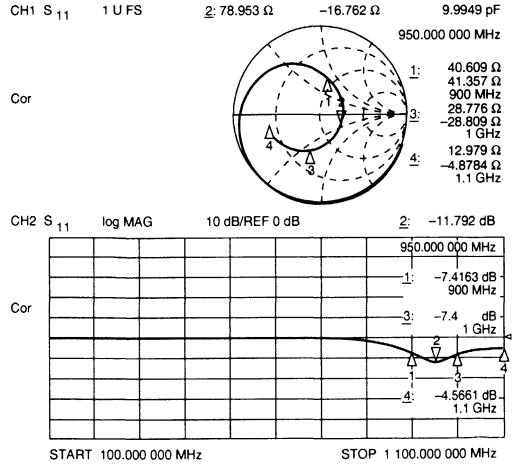


- **LO2**



- **Output impedance (with components mounted: test circuit 3)**
  @ Impedance including external components and evaluation board

- **RFout**

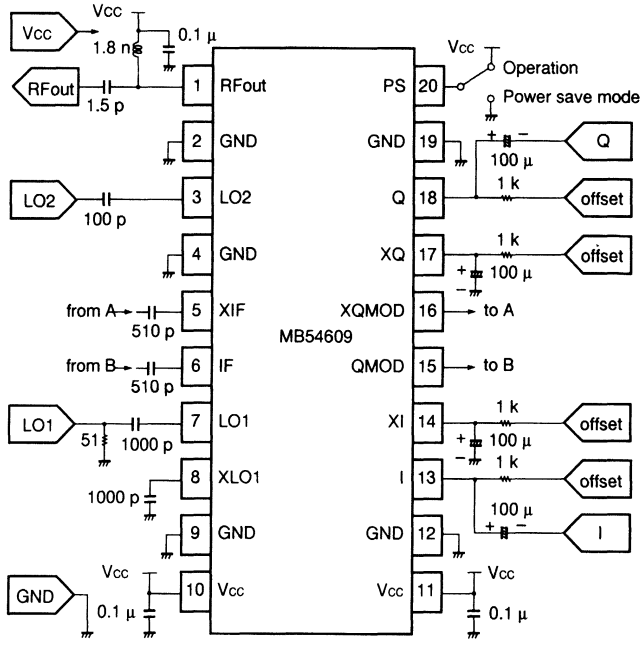


■ 1.5-GHz PDC APPLICATION MEASUREMENT DATA (Reference Values)

• **Measurement results**

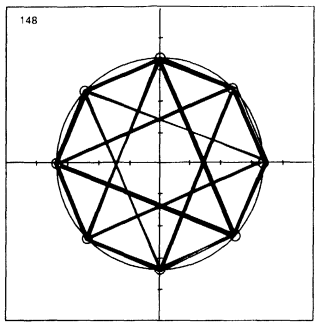
Parameter	Symbol	Measurement result	Unit	Condition	Test circuit
Baseband input signal	f_{BB}	42	kbps	π/4 DQPSK, Root-Nyquist filter (α = 0.5)	—
	V_{BB}	1.0	Vpp	Single-end input	—
Shifter input signal LO1	f_{LO1}	356	MHz	—	—
	P_{LO1}	−5	dBm	—	—
Mixer input signal LO2	f_{LO2}	1619	MHz	—	—
	P_{LO2}	−5	dBm	—	—
Mixer output signal RFout	f_{RF}	1441	MHz	$f_{RF} = f_{LO2} + f_{LO1}/2$	—
	P_{RF}	−13.4	dBm	SSB value	1
Return loss	RL_{LO1}	−18	dB	f_{LO1} = 356 MHz	3
	RL_{LO2}	−6	dB	f_{LO2} = 1619 MHz	
	RL_{RF}	−14	dB	f_{RF} = 1441 MHz	
Modulation precision	A_{ERR}	1.6	%	RMS magnitude error	2
	P_{ERR}	0.90	deg.	RMS phase error	
	V_{ERR}	2.2	%	RMS vector error	
Carrier suppression	CS	−39.0	dBc	—	2

• **External circuit constants (with the IC mounted on the evaluation board)**



- **Modulation precision and output spectrum (test circuit 2)**
  @ Baseband signal: π/4 DQPSK, 42 kbps, 1.0 Vpp, PN 15, Root-Nyquist filter α = 0.5
  Input signals: LO1 = 356 MHz, –5 dBm; LO2 = 1619 MHz, –5 dBm
  Output signal: RFout = 1441 MHz

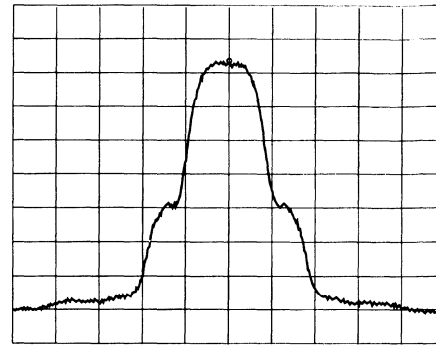
- **Modulation precision**



RMS Vector	Error =	2.243%
Peak Vector	Error =	4.552%
RMS Magnitude	Error =	1.597%
Peak Magnitude	Error =	3.756%
RMS Phase	Error =	0.902 degs
Peak Phase	Error =	–1.977 degs
Carrier Freq	Offset =	–1.454e+03 Hz
Carrier Phase	Offset =	7.417 degs
Carrier Leak	=	–33.001 dB
Bias Vector	=	(1.839, 1.275)%
Gravity Center	=	(–1.295, 0.833)%

VG: 7.000e-02 V/Div
Baseband Filter: RtNyq (0.500) Rectangle Len = 64 OSR = 4.761905

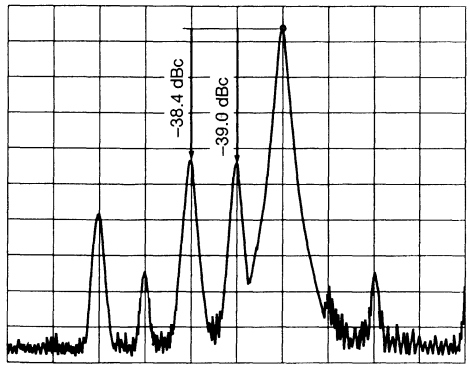
- **Output spectrum**



CENTER = 1441 MHz
SPAN = 200 kHz
RBW = 3 kHz VBW = 3 kHz SWP = 100 ms AVG = 128
ATT = 10 dB
REF = –10 dBm 10 dB/div.

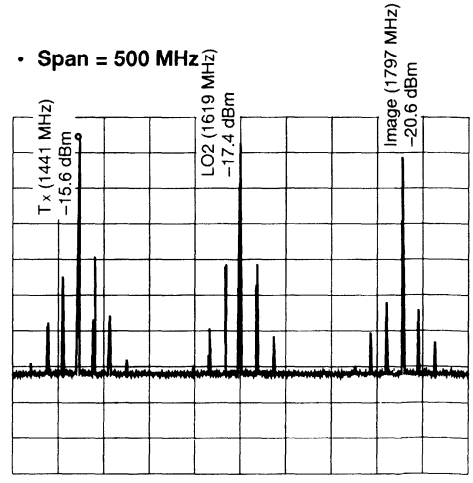
- **Spectrum (test circuit 2)**
  @ Baseband signal: π/4 DQPSK, 42 kbps, 1.0 Vpp, 0000, Root-Nyquist filter α = 0.5
  Input signals: LO1 = 356 MHz, –5 dBm; LO2 = 1619 MHz, –5 dBm
  Output signal: RFout = 1441 MHz

- **Span = 26.2 kHz**



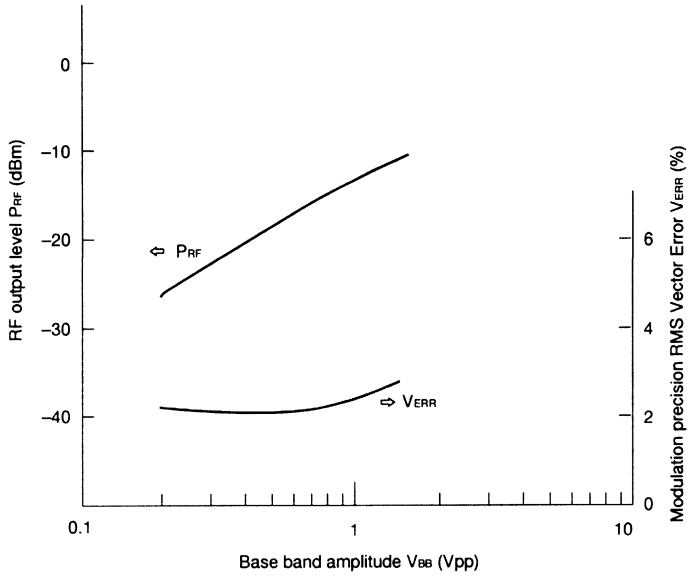
CENTER = 1441 MHz
SPAN = 26.2 kHz
RBW = 300 Hz VBW = 100 Hz SWP = 4 s
ATT = 10 dB
REF = –10 dBm 10 dB/div.

- **Span = 500 MHz**



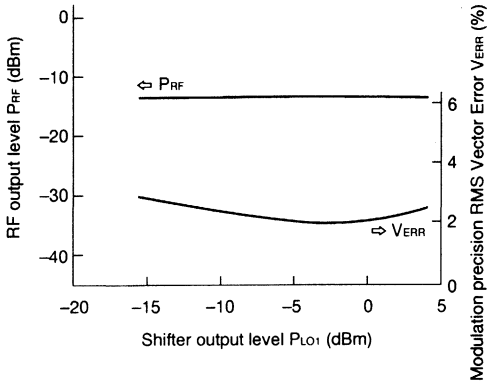
CENTER = 1619 MHz
SPAN = 500 MHz
RBW = 1 MHz VBW = 1 kHz SWP = 3 s
ATT = 10 dB
REF = –10 dBm 10 dB/div.

- **RF output level dependent on baseband amplitude (P_{RF}: test circuit 1, Modulation precision: test circuit 2)**
  @ Baseband signal of test circuit 2: π/4 DQPSK, 42 kbps, 1.0 Vpp, PN 15, Root-Nyquist filter α = 0.5
  Input signals of test circuits 1 and 2: LO1 = 356 MHz, –5 dBm; LO2 = 1619 MHz, –5 dBm
  Output signals of test circuits 1 and 2: RFout = 1441 MHz

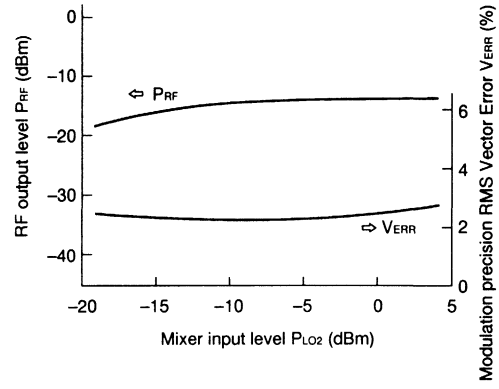


- **RF output level dependent on LO1 and LO2 input levels (P_{RF}: test circuit 1, Modulation precision: test circuit 2)**
  @ Baseband signal of test circuit 2: π/4 DQPSK, 42 kbps, 1.0 Vpp, PN 15, Root-Nyquist filter α = 0.5
  Input signals of test circuits 1 and 2: LO1 = 356 MHz, –5 dBm; LO2 = 1619 MHz, –5 dBm
  Output signals of test circuits 1 and 2: RFout = 1441 MHz

- **RF output level dependent on LO1 input level (@P_{LO2} = –5 dBm)**

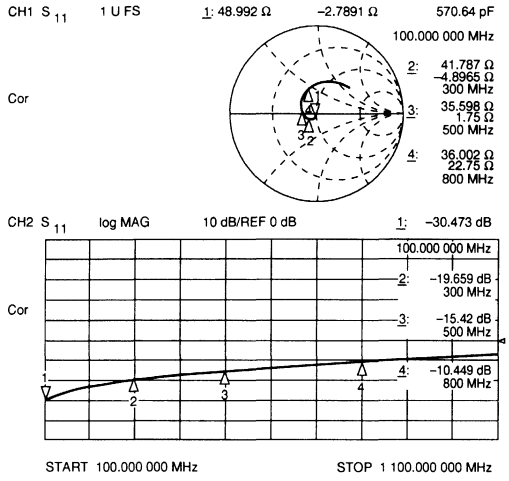


- **RF output level dependent on LO2 input level (@P_{LO1} = –5 dBm)**

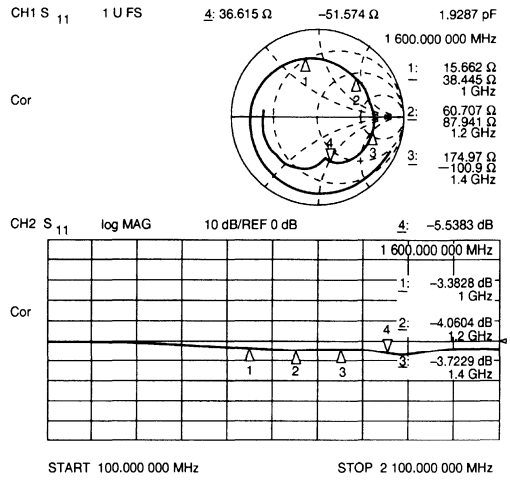


- **Input impedance (with components mounted: test circuit 3)**
  @ Impedance including external components and evaluation board

- **LO1**

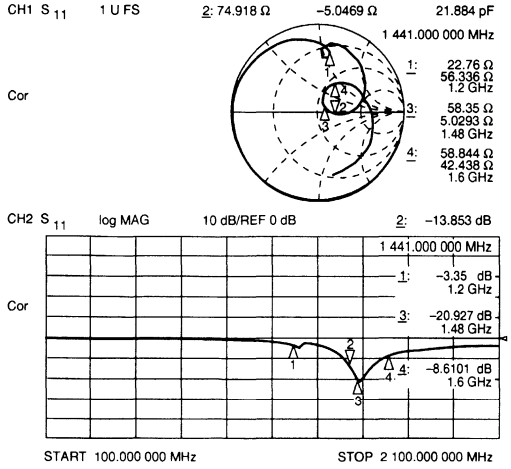


- **LO2**



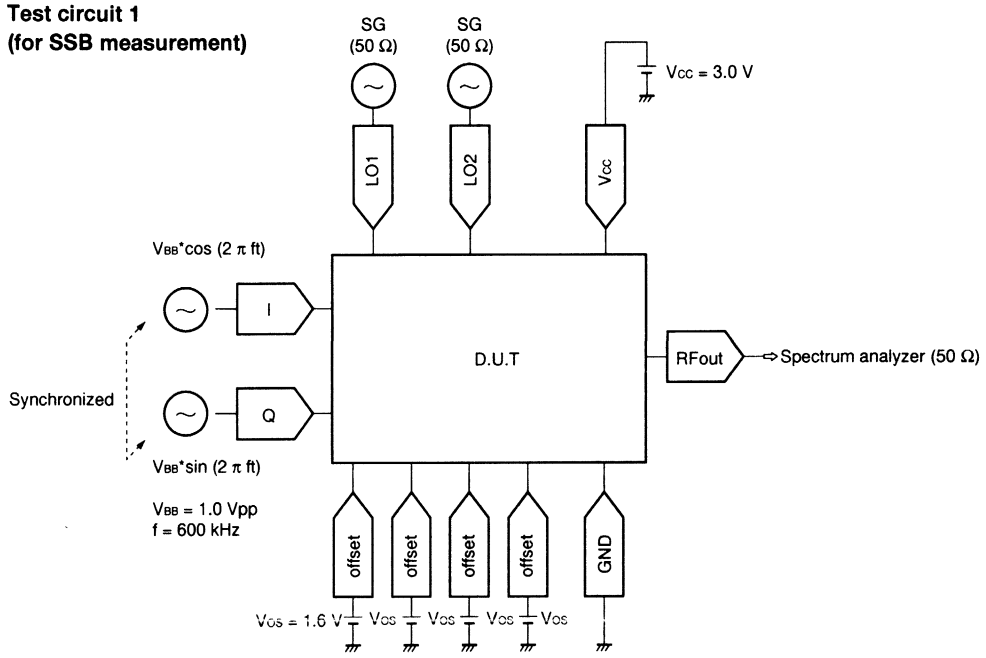
- **Output impedance (with components mounted: test circuit 3)**
  @ Impedance including external components and evaluation board

- **RFout**

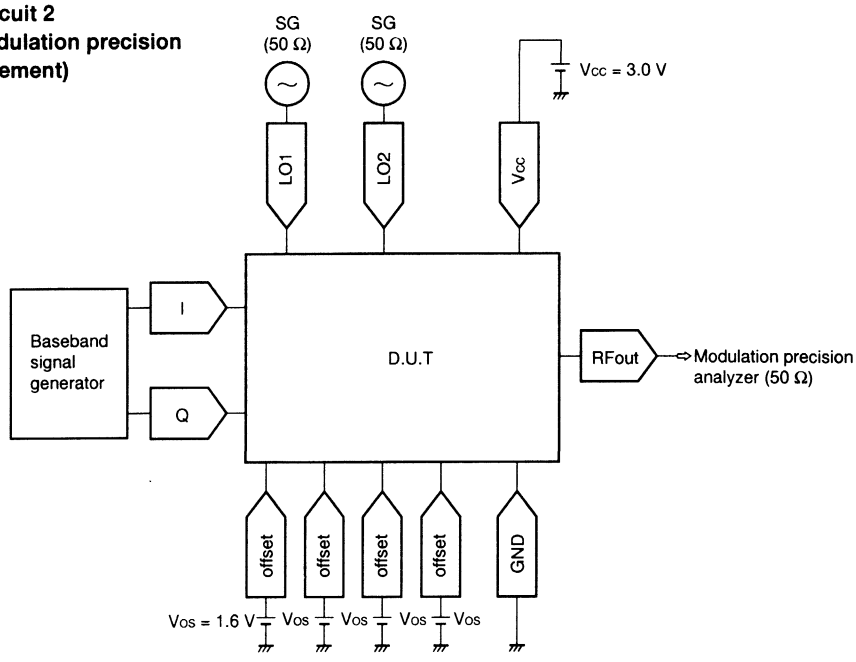


■ TEST CIRCUITS (Reference Examples)

• **Test circuit 1**
(for SSB measurement)



• **Test circuit 2**
(for modulation precision measurement)



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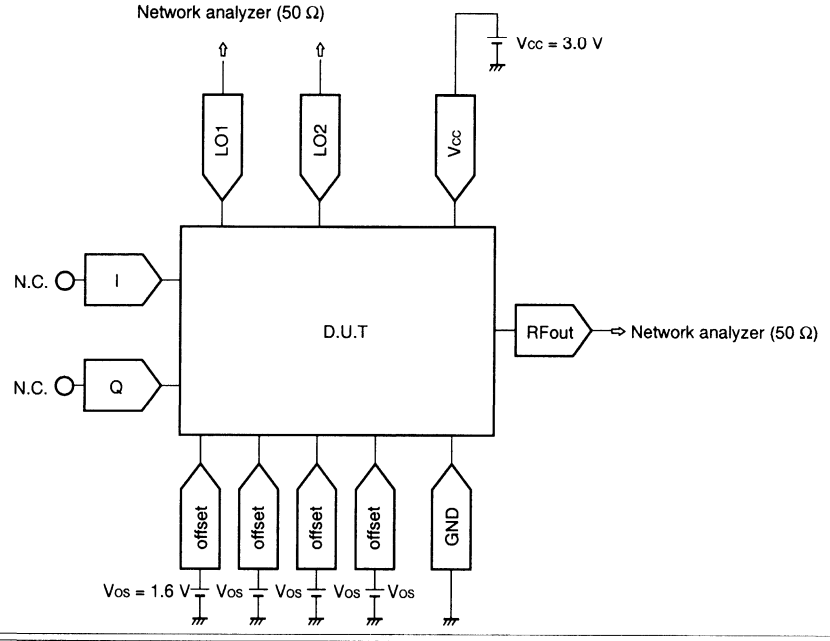
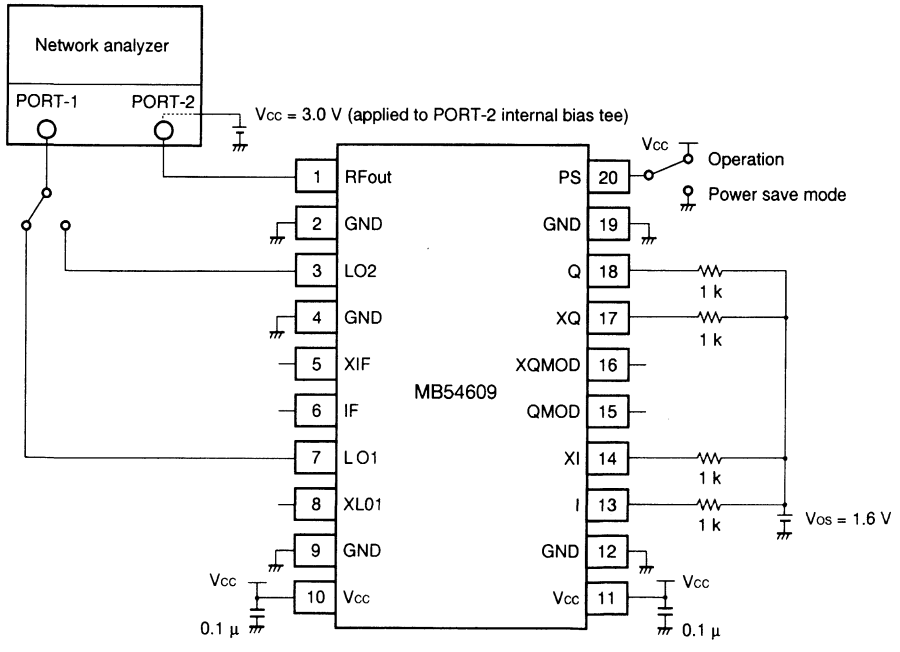
(Continued)

- **Test circuit 3 (for impedance measurement with components mounted)**



- **Test circuit 4 (for measurement of impedance of only IC)**



■ ORDERING INFORMATION

Part number	Package	Remarks
MB54609PFV	20-pin Plastic SSOP (FPT-20P-M03)	

MEMO

FUJITSU SEMICONDUCTOR
DATA SHEET

DS04–21400–3E

ASSP

COMPANDOR IC

MB3120

■ DESCRUPTION

The Fujitsu MB3120 is a compandor IC to expand dynamic range at transmission/reception systems and to improve the tone quality by means of restricting noise.

Two function are loaded on one IC, the one is the compressor which has the 2/1 ratio of input/output ratio by logarithm, and the expandor which has the 1/2 ratio of input/output ratio by logarithm.

The MB3120 is encapsulated in a small package, this enables high density mounting.

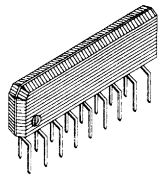
The MB3120 is well suitable for a mobile radio system like as cellular radio, MCA and handy telephone set.

■ FEATURS

- Wide power supply voltage range (3.2 V to 10.0 V)
- Low power supply current
- On-chip both compressor and expandor
- Wide dynamic range
- Less external elements
- Inhibit function with compression/expantion ratio of one
- Equipped with mute function which cut off the output signal
- 16-pin Flat Package
  17-pin Zig-zag In-line Package

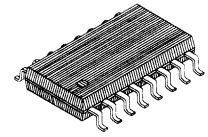
■ PACKAGE

PLASTIC PACKAGE



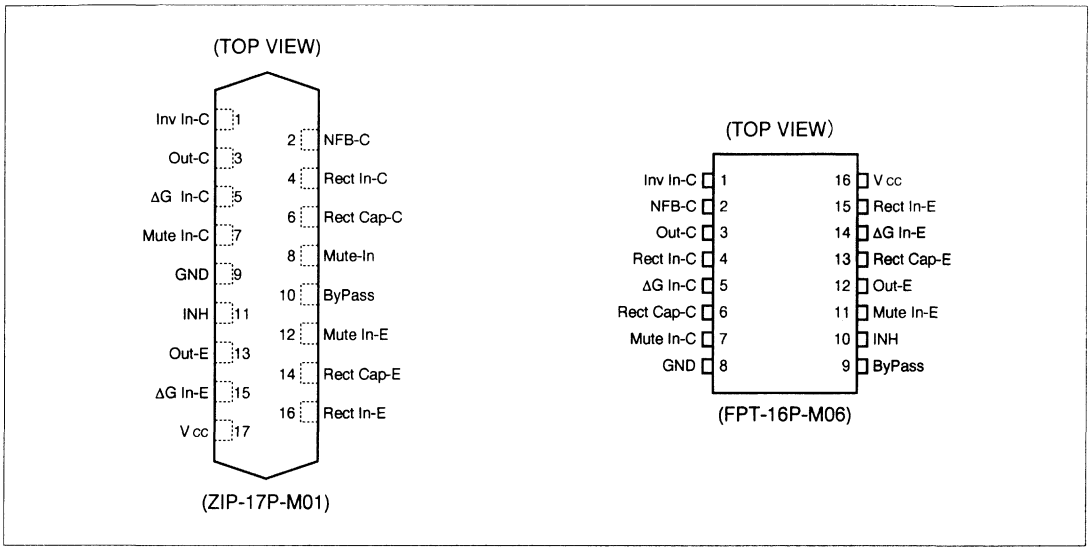
ZIP-17P-M01

PLASTIC PACKAGE

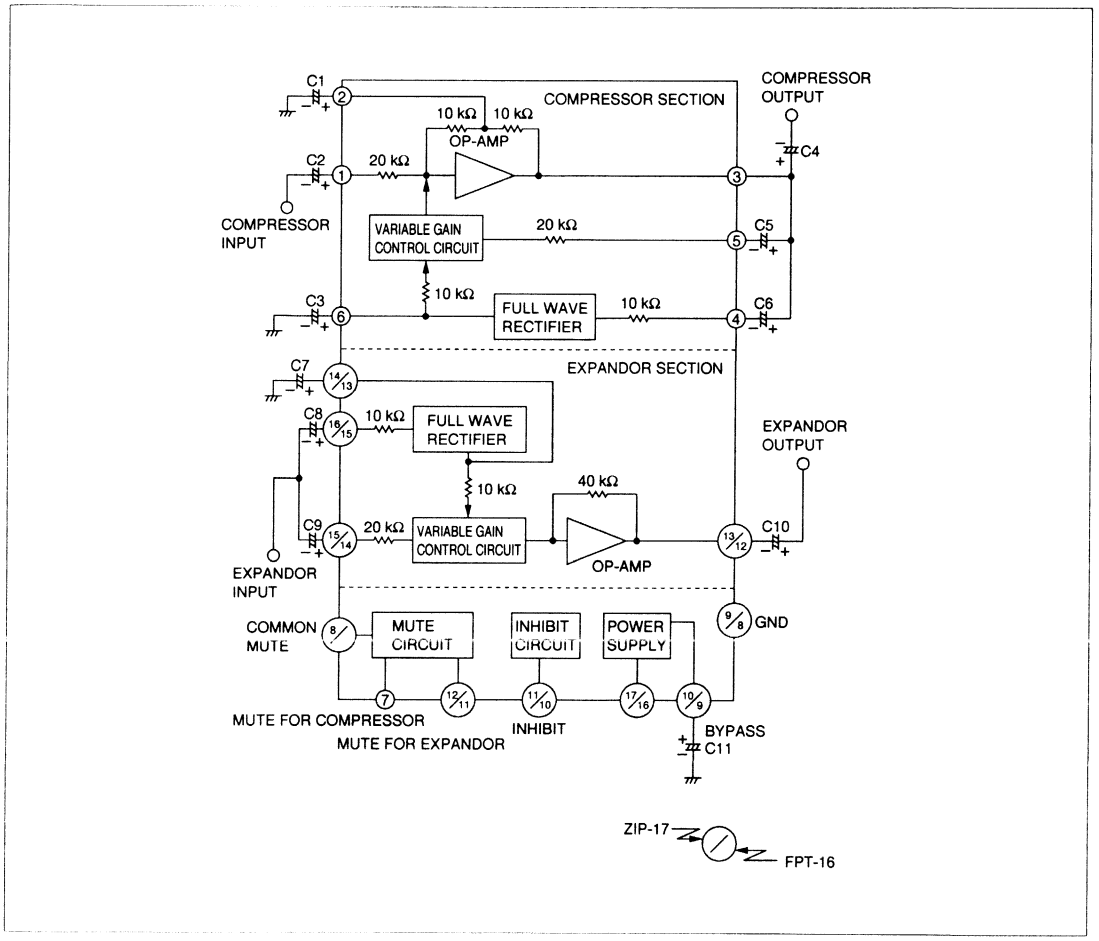


FPT-16P-M06

■ PIN ASSIGNEMENT



■ BLOCK DIAGRAM



■ BLOCK DESCRIPTIONS

C_1: C_1 determines the low cut off frequency of compressor section.

$$fc = \frac{1}{2\pi R \cdot C_1}$$

R is on chip feed back resistor (10 kΩ typ.)

C_2, C_8, C_9: Input coupling condenser

C_3, C_7: Smooth capacitor of full wave rectifier. Atack time and recovery time are determined by C_3 and C_7.

Time constant T_C can be calculated.

T_C (ms) ≅ 10 × C_3 (μF)

C_4, C_{10}: Output coupling condenser

C_5, C_6: Coupling condenser for internal feed back of compressor section.

C_{11}: Ripple filter condenser

■ ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	12	V
Mute Control Voltage	V_{MUTE}	5*	V
Inhibit Control Voltage	V_{INH}		
Power Dissipation	P_D	560	mW
Operating Temperature	Ta	−20 to +75	°C
Storage Temperature	Tstg	−55 to +125	°C

*: This value takes V_{CC} when V_{CC} is less than 5 V.

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Power Supply Voltage	V_{CC}	3.2	—	10	V
Operating Temperature	Ta	−20	—	75	°C

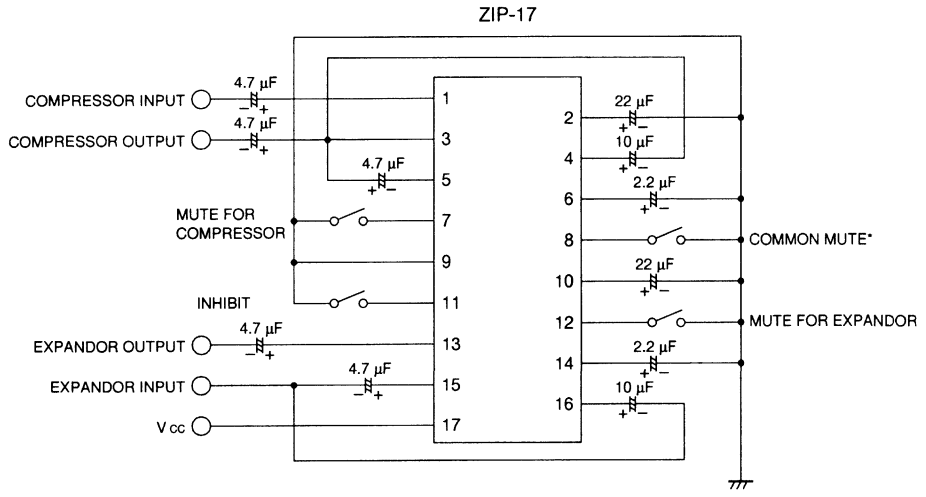
■ ELECTRICAL CHARACTERISTICS

(V_{CC} = 8 V, Ta = 25°C, f = 1 kHz, R_L = 10 kΩ)

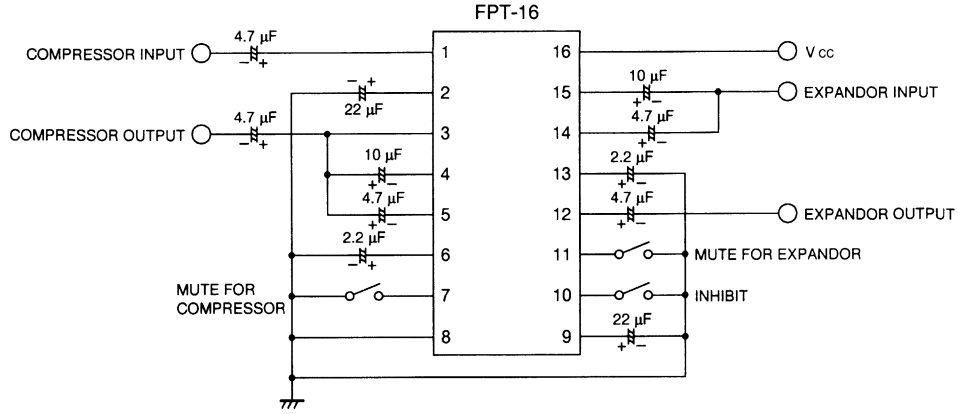
Parameter		Symbol	Condition	Value			Unit
				Min.	Typ.	Max.	
Power Supply Current		I_{CC}	—	—	3.0	4.5	mA
Compressor	Input Resistance	R_{INC}	—	14	20	—	kΩ
	Input Reference Level	V_{OC0}	V_{IN} = –6 dBm	–10.5	–9.0	–7.5	dBm
			V_{IN} = –6 dBm, Ta = –20 to 75°C*2	–2.5	0	2.5	dB
	Output Level*1	V_{OC1}	V_{IN} = –20 dB	–10.5	–10.0	–9.5	dB
		V_{OC2}	V_{IN} = –40 dB	–20.7	–20.0	–19.3	dB
		V_{OC3}	V_{IN} = –60 dB	–31.5	–30.0	–29.0	dB
			V_{IN} = –60 dB, Ta = –20 to 75°C*2	–4.0	0	3.0	dB
		V_{OC4}	V_{IN} = –80 dB	—	–40.0	—	dB
Expandor	Input Resistance	R_{INE}	—	4.7	6.7	—	kΩ
	Input Reference Level	V_{OE0}	V_{IN} = –9 dBm	–1.5	0	1.5	dBm
			V_{IN} = –9 dBm, Ta = –20 to 75°C*2	–2.5	0	2.5	dB
	Output Level*1	V_{OE1}	V_{IN} = –10 dB	–20.5	–20.0	–19.5	dB
		V_{OE2}	V_{IN} = –20 dB	–40.7	–40.0	–39.3	dB
		V_{OE3}	V_{IN} = –30 dB	–61.0	–60.0	–58.5	dB
			V_{IN} = –30 dB, Ta = –20 to 75°C*2	–3.0	0	4.5	dB
		V_{OE4}	V_{IN} = –40 dB	—	–80.0	—	dB
Compandor	Total Harmonic Distortion	THD	V_O = 0 dBm	—	0.5	2.0	%
	Output Noise Voltage	V_{ON}	BW = 100 Hz to 5 kHz	—	—	–80.0	dBm
	Voltage Gain	A_V	V_{IN} = –6 dBm	4.5	6.0	7.5	dB
	Gain Deviation 1	ΔA_{V1}	V_{IN} = –6 dBm, Ta = –20 to 75°C*2	–3.0	0	3.0	dB
	Gain Deviation 2	ΔA_{V2}	f = 200 Hz to 5 kHz, V_O = 0 dBm	–0.5	0	0.5	dB
	Voltage Gain at Inhibit	A_{VINH}	V_{IN} = –6 dBm, V_{ININH} = 0.4 V	4.5	6.0	7.5	dB
Compressor Mute Attenuation*3		V_{OCMUTE}	V_{IN} = –6 dBm, $V_{INCMUTE}$ = 2.7 V	—	–50	—	dBm
Expandor Mute Attenuation*3		V_{OEMUTE}	V_{IN} = –9 dBm, $V_{INEMUTE}$ = 2.7 V	—	–70	—	dBm
High-level Control Voltage for Mute and Inhibit Pins*3		V_{IH}	—	2.7	—	—	V
Low-level Control Voltage for Mute and Inhibit Pins*3		V_{IL}	—	—	—	0.4	V

*1: Measured at input reference level of 0 dB.
*2: Gain deviation with temperature when output level of 25°C is specified ad 0 dB.
*3: As for Zip-17 pin, both compressor and expandor circuit enter mute function depending on 8 pin input.

■ TYPICAL CONNECTION EXAMPLE



*: Both the mute of Compressor and Expandor can be controlled by this terminal.

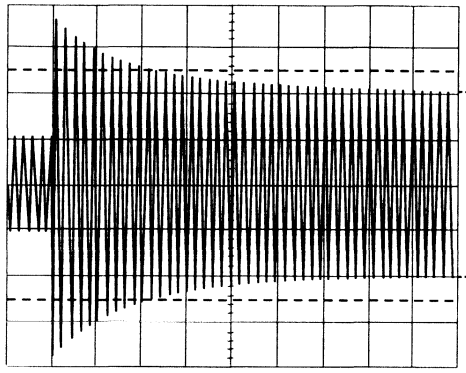


■ OUTPUT TRANSITION RESPONSE CHARACTERISTICS

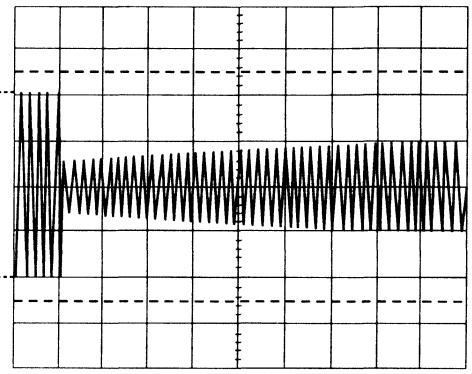
Condition: V_{CC} = 8 V, f = 1 kHz, R_L = 10 kΩ, Mute OFF, INH OFF, Typ. connection

COMPRESSOR (Y: 0.2 V/div, X: 5 msec/div)

V_{IN} = −18 dBm → −6 dBm (V_O = −15 dBm → −9 dBm)

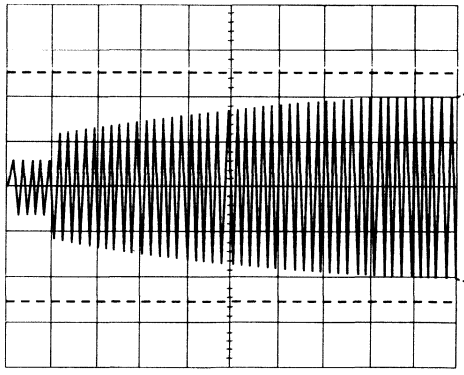


V_{IN} = −6 dBm → −18 dBm (V_O = −9 dBm → −15 dBm)

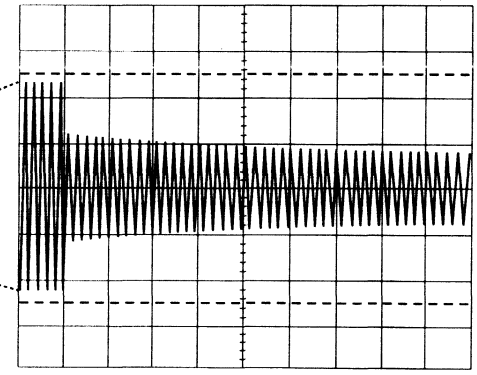


EXPANDOR (Y: 0.5 V/div, X: 5 msec/div)

V_{IN} = −15 dBm → −9 dBm (V_O = −12 dBm → 0 dBm)

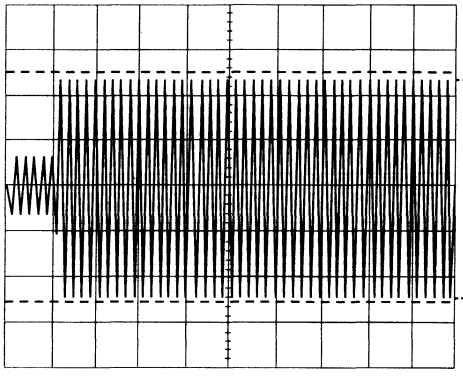


V_{IN} = −9 dBm → −15 dBm (V_O = 0 dBm → −12 dBm)

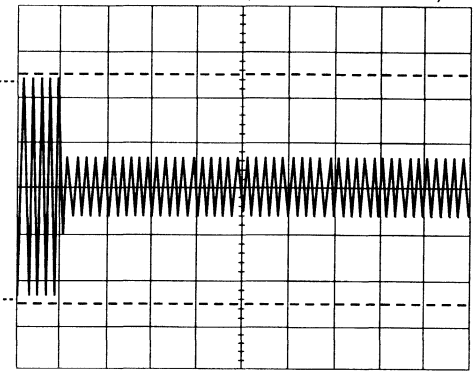


COMPANDOR (Y: 0.5 V/div, X: 5 msec/div)

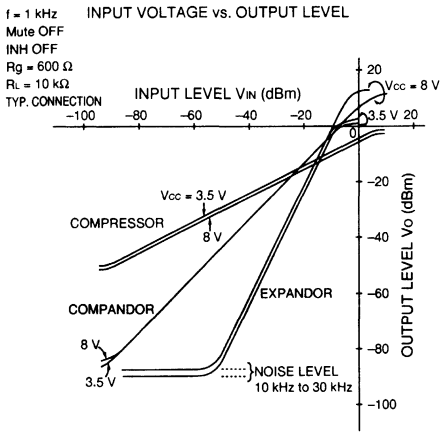
V_{IN} = −18 dBm → −6 dBm (V_O = −12 dBm → 0 dBm)

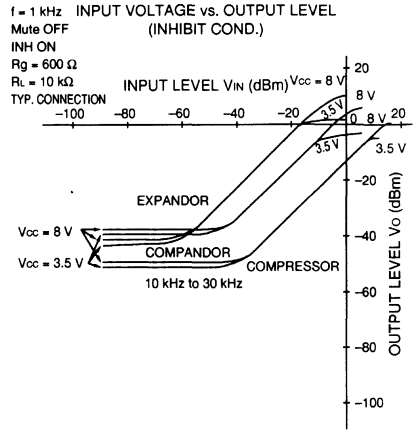


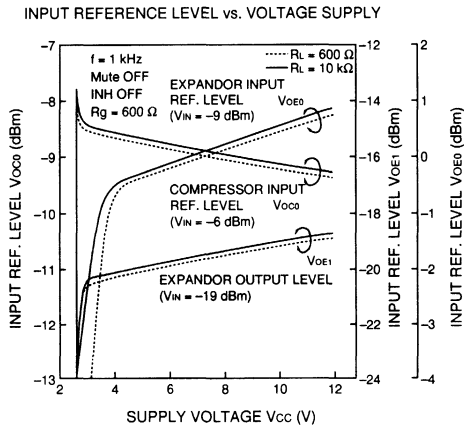
V_{IN} = −6 dBm → −18 dBm (V_O = 0 dBm → −12 dBm)

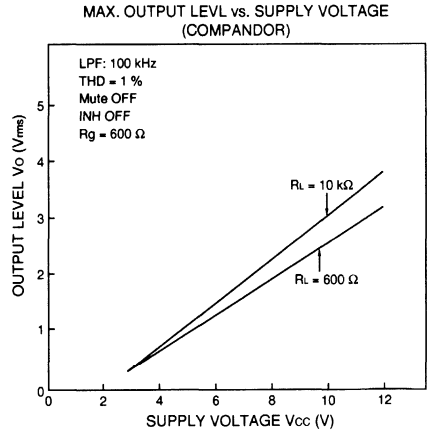


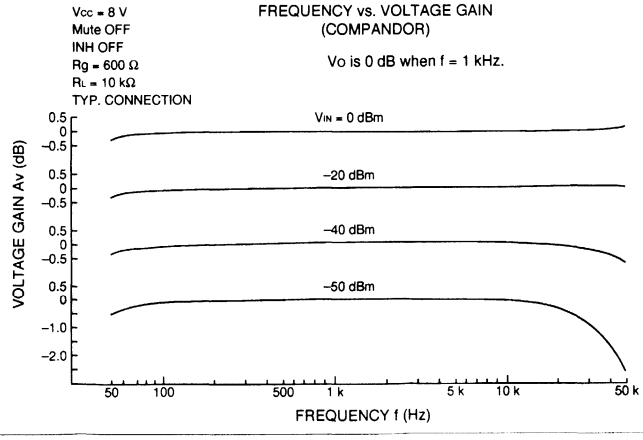
■ TYPICAL CHARACTERISTICS CURVES











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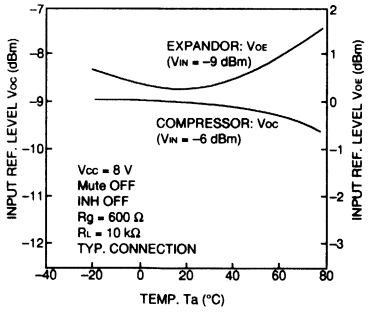
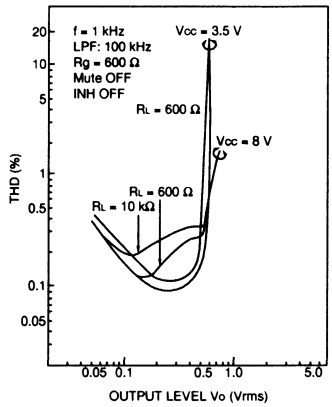
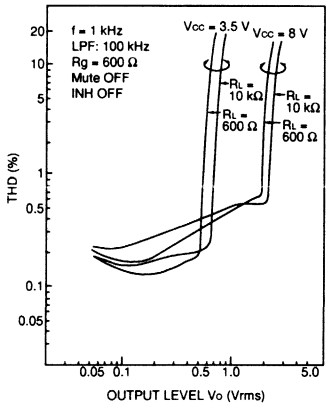
INPUT REFERENCE LEVEL vs. TEMPERATURE



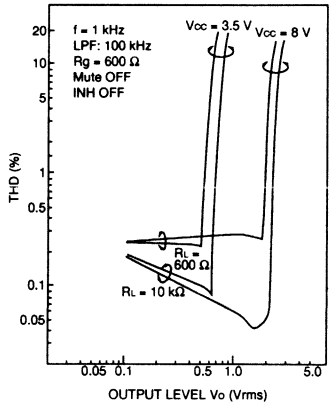
OUTPUT LEVEL vs. TOTAL HARMONIC DISTORTION (COMPRESSOR)



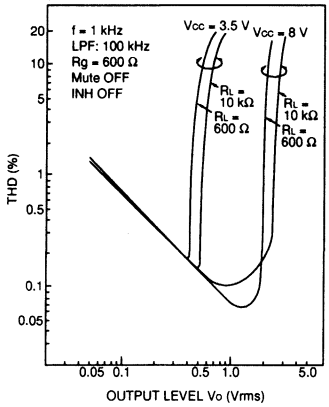
OUTPUT LEVEL vs. TOTAL HARMONIC DISTORTION (EXPANDOR)



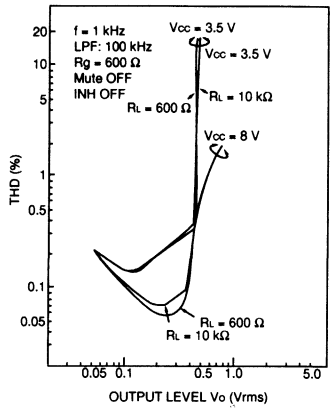
OUTPUT LEVEL vs. TOTAL HARMONIC DISTORTION (COMPANDOR)



OUTPUT LEVEL vs. TOTAL HARMONIC DISTORITON (EXPANDOR INHIBIT COND.)



OUTPUT LEVEL vs. TOTAL HARMONIC DISTORITON (COMPRESSOR INHIBIT COND.)



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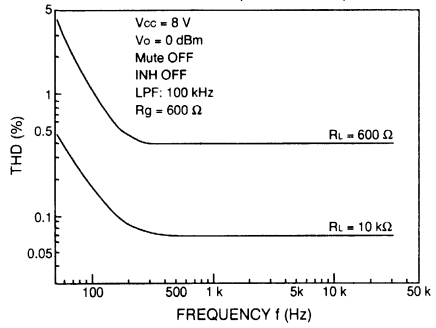
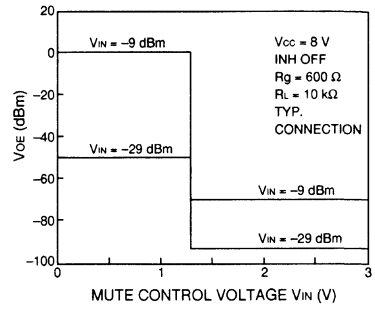
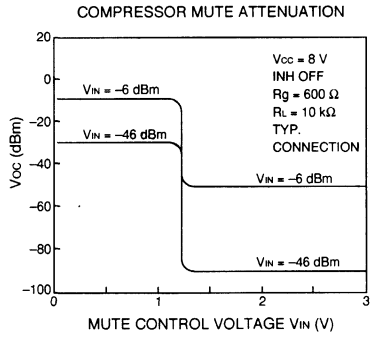
FREQUENCY vs. TOTAL HARMONIC DISTORTION (COMPANDOR)



EXPANDOR MUTE ATTENUATION



COMPRESSOR MUTE ATTENUATION



FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-23901-6E

ASSP

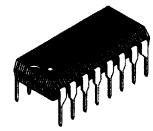
1200 BPS MSK MODEM

MB87002

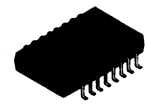
1200 BPS MSK (Minimum Shift Keying) MODEM

The MB87002 is a 1200-bps CMOS minimum shift keying (MSK) single-chip modem for multichannel access (MCA) and radio communication application.
Its operation at low supply voltages and low power consumption is especially suitable for portable application.

- Data rate: 1200-bps
- Low power consumption (20 mW with 5 V power supply)
- Low supply voltage operation: 3.0 to 5.5 V (5 V typical)
- On-chip crystal oscillator: 3.6864 MHz
- Switched-capacitor filter (SCF)
- Selectable timing regenerator pull-in characteristic (within 15 bits for high-speed, and within 25 bits for low-speed operation)
- Low external component count
- TTL compatible inputs and outputs



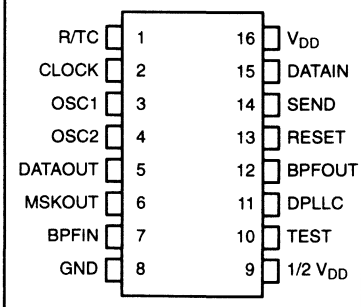
PLASTIC PACKAGE
(DIP-16P-M03)



PLASTIC PACKAGE
(FPT-16P-M03)

PIN ASSIGNMENT

(TOP VIEW)



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See NOTE)

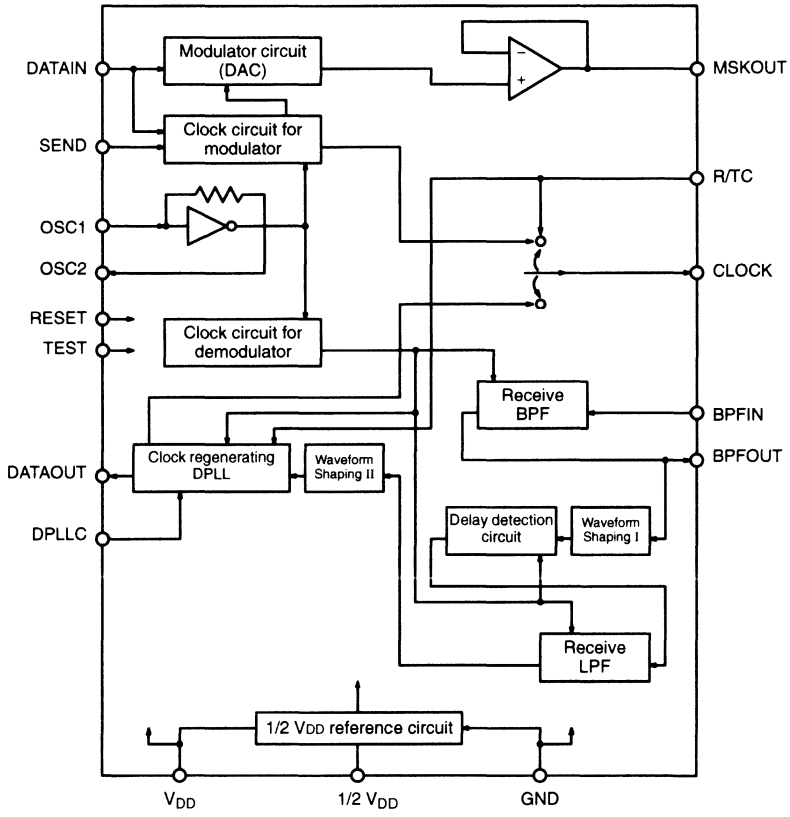
Parameter	Symbol	Pin name	Value			Unit
			Min	Typ	Max	
Power Supply Voltage	V_{DD}	V_{DD}	GND – 0.3	–	7	V
Input Voltage	V_{IN}	All input pins	GND – 0.3	–	V_{DD} + 0.3	V
Output Voltage	V_{OUT}	All output pins	GND – 0.3	–	V_{DD} + 0.3	V
Output Current	I_{OUT}	All output pins	–10	–	10	mA
Storage Temperature	T_{STG}	–	–55	–	125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN DESCRIPTIONS

Pin No.	Symbol	I/O	Functional descriptions
1	R/TC	I	Transmit–receive clock output control. When pulled high, the 1.2 kHz transmit clock is output from the CLOCK pin and DATAOUT becomes low. When pulled low, the 1.2 kHz receive clock is output from the CLOCK pin.
2	CLOCK	O	Transmit–receive clock output pin. When R/TC pin is pulled high, 1.2 kHz transmit clock is output. When R/TC pin is pulled low, the 1.2 kHz receive clock is output.
3	OSC1	I	Pin for external crystal (3.6864 MHz) connection.
4	OSC2	O	Pin for external crystal (3.6864 MHz) connection.
5	DATAOUT	O	Regenerated data output signal.
6	MSKOUT	O	Modulated signal output pin. $V_{DD}/2$ is output when the RESET pin is pulled low.
7	BPFIN	I	Demodulated signal input to the receive band–pass filter (BPF).
8	GND	–	Ground
9	1/2 V_{DD}	O	$V_{DD}/2$ reference voltage output
10	TEST	I	Test function control signal input. In the normal mode, this pin is pulled high or left open. In the test mode, it is pulled low. In the test mode, the BPF IN pin directly accepts Waveform Shaping I and receive LPF input signals, and the DATA IN pin directly accepts Waveform Shaping II input signals. In this mode, the delay detection circuit signal is output from BPFOUT and the receive LPF signal is output from MSKOUT.
11	DPLLC	I	DPLL pull–in time control signal input. When pulled low, high–speed operation is selected. When pulled high, low–speed operation is selected.
12	BPFOUT	O	Receive BPF output pin.
13	RESET	I	Device reset signal input. A low on this pin resets all circuits. Pulled high or left open to enable device operation.
14	SEND	I	Data transmit enable. With the reset high or open, transmit signals are output when this pin is pulled low to high.
15	DATAIN	I	Transmit data input to the receive BPF.
16	V_{DD}	–	Supply voltage pin (+3.0 to +5.5 V).

MB87002 BLOCK DIAGRAM



FUNCTION DESCRIPTION

The timing generating section generates the clock signals required by the modulator and demodulator. The basic clock is generated by an internal oscillator and external crystal (3.6864 MHz).
Modulator uses a programmable DAC with a 6 bit resistor string. The MSKOUT output is 1200 Hz for input 1 and 1800 Hz for input 0 synchronized with transmit clock. Before the transmit signal is output, a fixed level of 1/2 V_{DD} is output by pulling the SEND pin low.
The demodulator is composed of a band–pass filter (BPF), a delay detection circuit, a low–pass filter (LPF), and a digital phase–locked loop (DPLL). The BPF removes noise components from the 1,200 Hz and 1,800 Hz receive signals from the BPFIN pin and consists of a 10th–order Chebyshev switched–capacitor filter (SCF). The delay detection circuit, after conversion of the BPF output from analog to digital in the waveform shaping circuit, regenerates data by delay detection. The noise components in the regenerated data are removed by the LPF. The LPF is a third–order Butterworth filter and removes noise components of 800 Hz or higher. The DPLL extracts the receive clock from the regenerated data. The regenerated data is output from the DATAOUT pin synchronized with the receive clock. The DPLL has a tendency to degrade the bit error rate when the pull–in time is shortened. This IC allows users to choose between two pull–in times. When the DPLLC pin is pulled low, the high–speed mode is selected. When pulled high, the low–speed mode is selected.
The on–chip 1/2 V_{DD} circuit supplies the reference voltage required by BPF, LPF, and waveform shaping circuits and reduces external circuitry and component count.

NOTE: Devices consisting of mixed analog and digital signal processing circuits are usually difficult to test. The MB87002 incorporates a test circuit which simplifiers independent testing of the BPF, delay detection circuit, LPF, and DPLL.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Pin name	Value			Unit
			Min	Typ	Max	
Power Supply Voltage	V_{DD}	V_{DD}	3.0	5.0	5.5	V
Input Voltage	V_{IN}	All input pins	0	–	V_{DD}	V
OSC1 Pin Load Capacitance	C_{OSC1}	OSC1	25	–	50	pF
OSC2 Pin Load Capacitance	C_{OSC2}	OSC2	25	–	50	pF
Analog Output Load Resistance	R_{MO}	MSKOUT	10	–	–	kΩ
Analog Output Load Capacitance	C_{MO}	MSKOUT	–	–	30	pF
Operating Temperature	T_A	–	–30	–	70	°C

ELECTRICAL CHARACTERISTICS

DC characteristics (V_{DD} = 4.5 to 5.5 V)

T_A = 25°C

Parameter	Symbol	Pin name	Condition	Value			Unit
				Min	Typ	Max	
Power Supply Current	I_{DD}	V_{DD}		–	4	8	mA
Digital Input Low Voltage	V_{IL}	RESET, SEND, DATAIN, DPLLC, R/TC, TEST		0	–	0.8	V
Digital Input High Voltage	V_{IH}	RESET, SEND, DATAIN, DPLLC, R/TC, TEST		2.2	–	V_{DD}	V
Digital Input Low Current	I_{IL}	SEND, DATAIN, DPLLC, R/TC	V_{IN} = GND	–10	–	0	µA
Digital Input High Current	I_{IH}	RESET, SEND, DATAIN, DPLLC, R/TC, TEST	V_{IN} = V_{DD}	0	–	10	µA
Pull–up Resistance	R_{PLU}	RESET, TEST		25	50	100	kΩ
Digital Output Low Voltage	V_{OL}	DATAOUT, CLOCK	I_{OL} = 2.0 mA	0	–	0.4	V
Digital Output High Voltage	V_{OH}	DATAOUT, CLOCK	I_{OH} = 1.0 mA	2.4	–	V_{DD}	V
Oscillator Frequency	OSC_{IN}	OSC1, OSC2		–	3.6864	–	MHz
Analog Input Resistance 1	R_{AIN1}	BPFIN	Input pin–1/2 V_{DD}	50	100	200	kΩ
Analog input Voltage 1	V_{AIN1}	BPFIN		0.5	–	2.5	V_{P-P}
Analog Output Voltage 1	A_{OUT1}	MSKOUT	Operation	0.8	1.0	1.2	V_{P-P}
			Offset voltage in operation	1/2 V_{DD} –0.3	1/2 V_{DD}	1/2 V_{DD} +0.3	V
			RESET = Low	1/2 V_{DD} –0.3	1/2 V_{DD}	1/2 V_{DD} +0.3	V
Receive BPF Absolute Gain	ABS_1	–	Input frequency 1500 Hz	–1.0	0	1.0	dB
Receive BPF Frequency Characteristics	F_1	–	0–300 Hz 900–1200 Hz 1200–1800 Hz 1800–2100 Hz 3000–5000 Hz Reference frequency 1500 Hz	– –3.5 –1.0 –3.5 – 	– – – – – 	–40.0 – – – –30.0 	dB dB dB dB dB
Receive LPF Cutoff Frequency	F_0	–	3 dB down	–	800	–	Hz
Receive LPF Absolute Gain	ABS_2	–	0 Hz < Input frequency ≤ 300 Hz	–	–6.0	–	dB

DC characteristics (V_{DD} = 3.0 to 4.5 V)

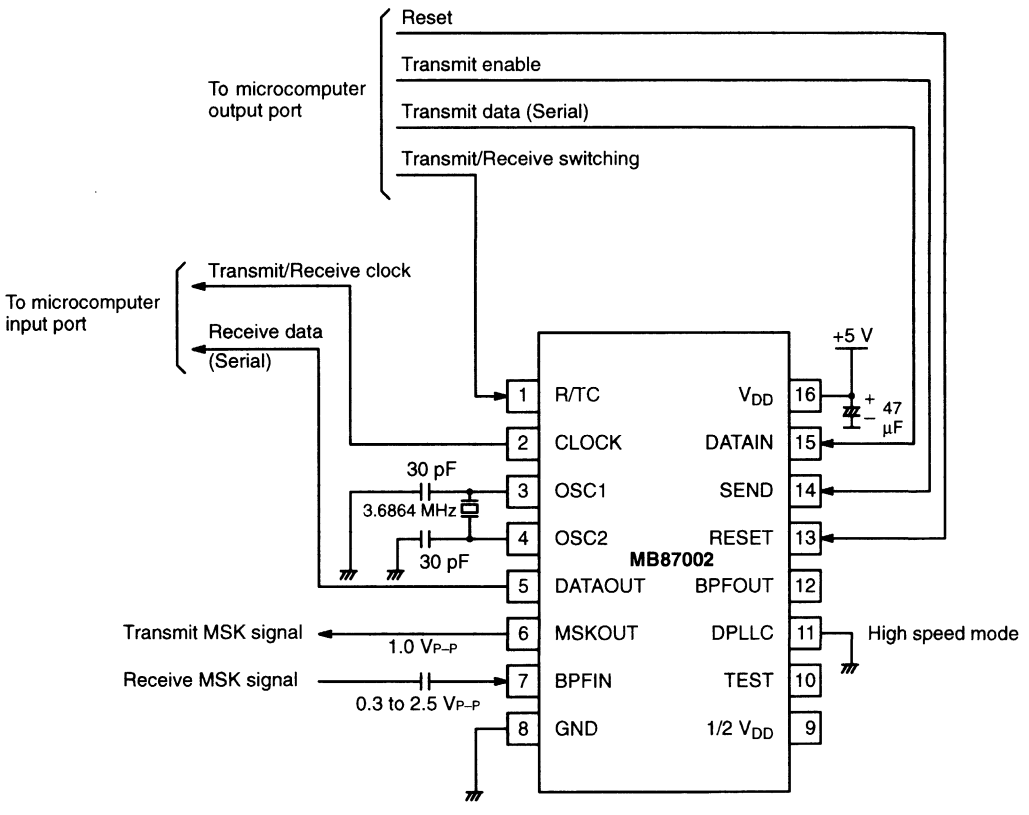
T_A = 25°C

Parameter	Symbol	Pin name	Condition	Value			Unit
				Min	Typ	Max	
Power Supply Current	I_{DD}	V_{DD}		–	–	8	mA
Digital Input Low Voltage	V_{IL}	RESET, SEND, DATAIN, DPLLC, R/TC, TEST		0	–	0.6	V
Digital Input High Voltage	V_{IH}	RESET, SEND, DATAIN, DPLLC, R/TC, TEST		2.2	–	V_{DD}	V
Digital Input Low Current	I_{IL}	SEND, DATAIN, DPLLC, R/TC	V_{IN} = GND	–10	–	0	µA
Digital Input High Current	I_{IH}	RESET, SEND, DATAIN, DPLLC, R/TC, TEST	V_{IN} = V_{DD}	0	–	10	µA
Pull–up Resistance	R_{PLU}	RESET, TEST		25	50	100	kΩ
Digital Output Low Voltage	V_{OL}	DATAOUT, CLOCK	I_{OL} = 0.5 mA	0	–	0.4	V
Digital Output High Voltage	V_{OH}	DATAOUT, CLOCK	I_{OH} = 0.5 mA	2.4	–	V_{DD}	V
Oscillator Frequency	OSC_{IN}	OSC1, OSC2		–	3.6864	–	MHz
Analog Input Resistance 1	R_{AIN1}	BPFIN	Input pin–1/2 V_{DD}	50	100	200	kΩ
Analog Input Voltage 1	V_{AIN1}	BPFIN		0.5	–	V_{DD} – 2.0	V_{P-P}
Analog Output Voltage 1	A_{OUT1}	MSKOUT	Operation	V_{DD}x0.16	V_{DD}x0.2	V_{DD}x0.24	V_{P-P}
			Offset voltage in operation	1/2 V_{DD} –0.3	1/2 V_{DD}	1/2 V_{DD} +0.3	V
			RESET = Low	1/2 V_{DD} –0.3	1/2 V_{DD}	1/2 V_{DD} +0.3	V
Receive BPF Absolute Gain	ABS_1	–	Input frequency 1500 Hz	–2.0	0	2.0	dB
Receive BPF Frequency Characteristics	F_1	–	0–300 Hz 900–1200 Hz 1200–1800 Hz 1800–2100 Hz 3000–5000 Hz Reference frequency 1500 Hz	– –3.5 –1.0 –3.5 – 	– – – – – 	–30.0 – – – –25.0 	dB dB dB dB dB
Receive LPF Cutoff Frequency	F_0	–	3 dB down	–	800	–	Hz
Receive LPF Absolute Gain	ABS_2	–	0 Hz < Input frequency ≤ 300 Hz	–	–6.0	–	dB

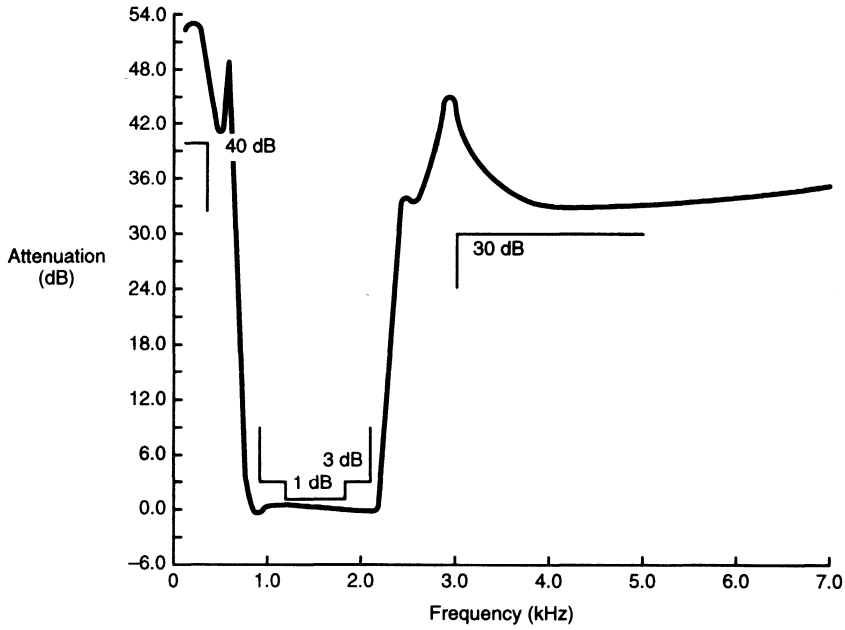
AC characteristics (V_{DD} = 3.0 to 5.5 V)

Parameter	Symbol	Pin name	Condition	Value			Unit
				Min	Typ	Max	
Transmit Clock Delay Time 1	t_{dRCH}	CLOCK	R/TC = "H"	0	150	417	µs
Transmit Clock Delay Time 2	t_{dSCH}	CLOCK	R/TC = "H"	417	570	834	µs
Transmit Clock Delay Time 3	t_{dSCL}	CLOCK	R/TC = "H"	0	150	417	µs
Transmit Clock High Width	t_{wHC1}	CLOCK	R/TC = "H"	390	417	444	µs
Transmit Clock Low Width	t_{wLC1}	CLOCK	R/TC = "H"	390	417	444	µs
SEND Setup Time	t_{SSC}	SEND	R/TC = "H"	1	–	–	µs
SEND Hold Time	t_{hSC}	SEND	R/TC = "H"	1	–	–	µs
DATAIN Setup Time	t_{SDC}	DATAIN	R/TC = "H"	1	–	–	µs
DATAIN Hold Time	t_{hDC}	DATAIN	R/TC = "H"	1	–	–	µs
MSKOUT Output Delay Time 1	t_{dCM1}	MSKOUT	R/TC = "H"	–	–	10	µs
MSKOUT Output Delay Time 2	t_{dCM2}	MSKOUT	R/TC = "H"	–	–	10	µs
BPFIN Invalid Time	t_{dRB}	BPFIN		0	–	10	ms
Pull–in Bit Number	N	–	R/TC = "L", DPLLC = "L", BPFIN: No noise	–	–	15	bit
Demodulator Delay Time	t_{dBD}	DATAOUT	R/TC = "L", DPLLC = "L", N ≥ 15 BPFIN: No noise	1483	1900	2317	µs
DATAOUT Timing	t_{dCD}	DATAOUT	R/TC = "L"	–1	–	1	µs
Receive Clock High Width	t_{wHC2}	CLOCK	R/TC = "L", DPLLC = "L", N ≥ 15 BPFIN: No noise	338	417	496	µs
Receive Clock Low Width	t_{wLC2}	CLOCK	R/TC = "L", DPLLC = "L", N ≥ 15 BPFIN: No noise	338	417	496	µs
RESET Low Width	t_{wLR}	RESET		20	–	–	µs
MSKOUT Output Delay Time 3	t_{dRM}	MSKOUT		0	–	10	µs
Transmit Clock Delay Time 4	t_{dTC4}	CLOCK		0	–	2	µs
Receive Clock Delay Time 1	t_{dRC1}	CLOCK		0	–	2	µs

TYPICAL CONNECTION EXAMPLE

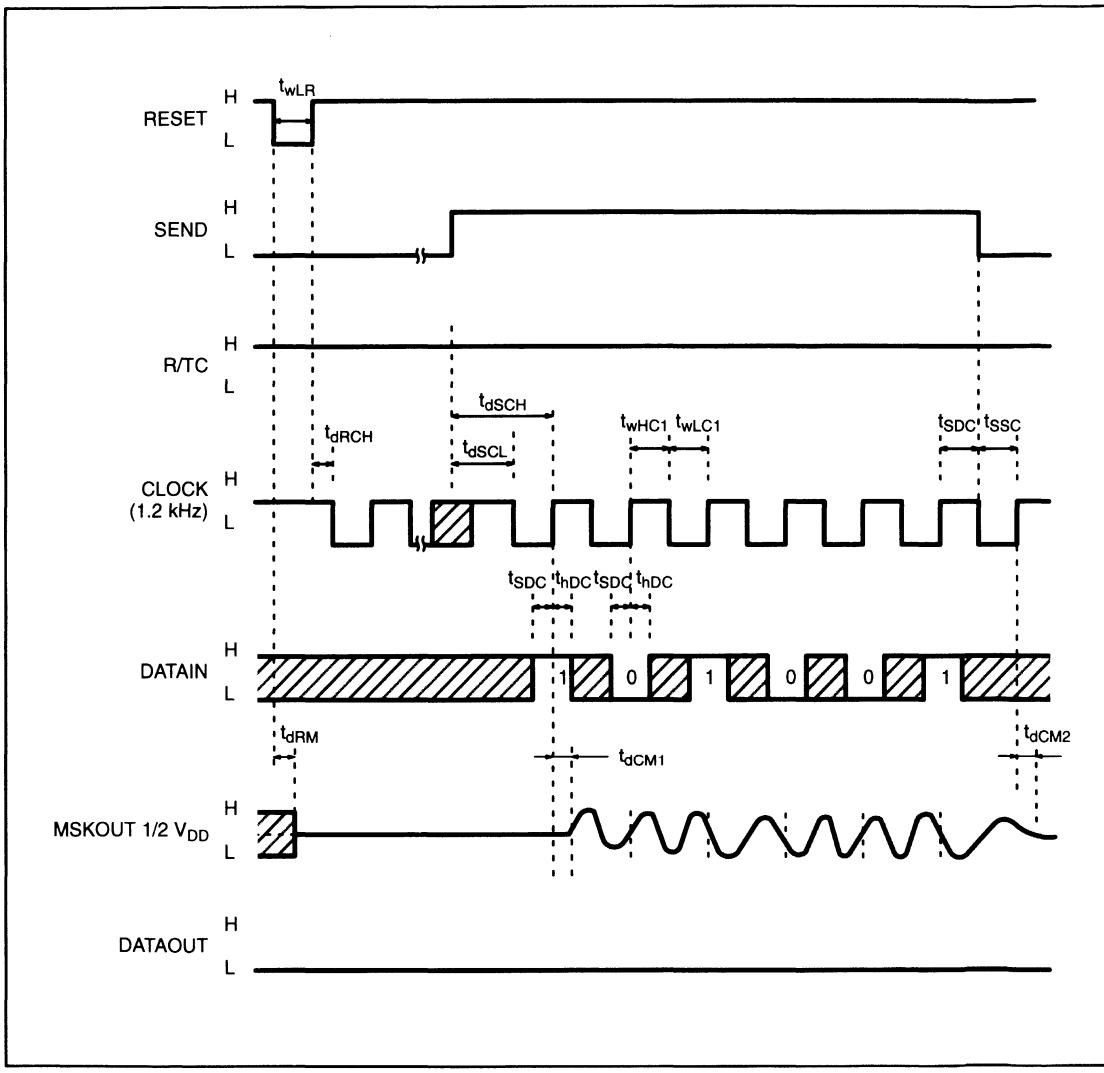


BPF FREQUENCY CHARACTERISTICS



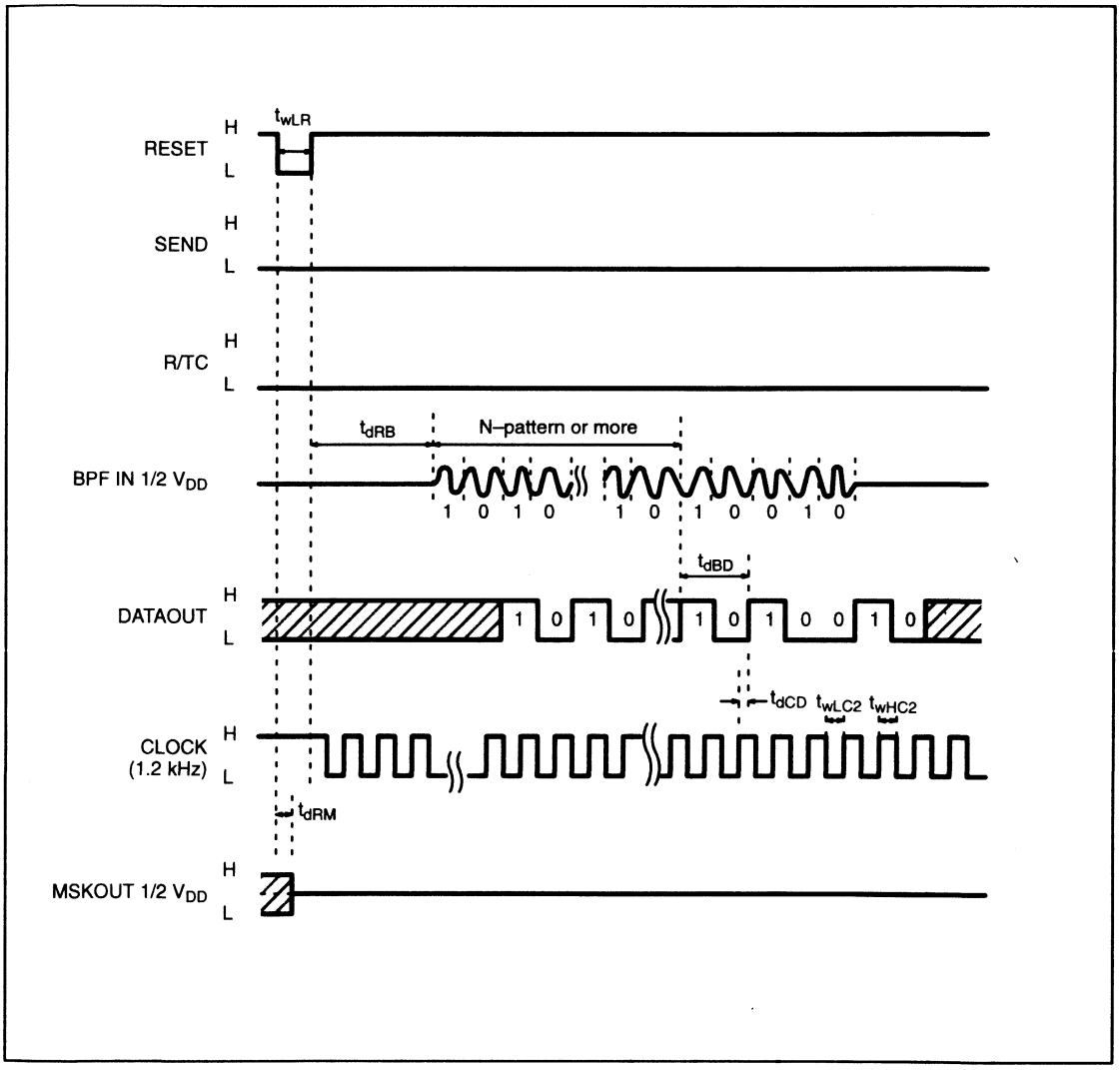
TIMING CHART

Modulator timing chart (TEST pin = High or Open)



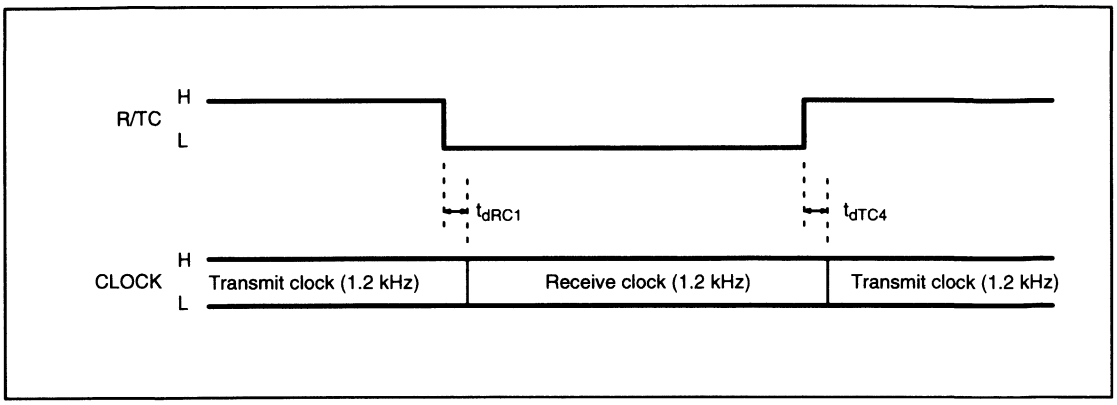
NOTE: 1. SEND pin is pulled high after low–to–high transition of the RESET pin, or open.
2. DATAIN signal is read at the rising edge of the CLOCK.
3. When SEND pin changes from low to high, the CLOCK pin is pulled high once. Then 1.2 kHz clock is output.
4. When R/TC pin is pulled high, DATAOUT pin outputs low.
5. After power was applied, RESET pin must be set to low to rest all circuits before use.

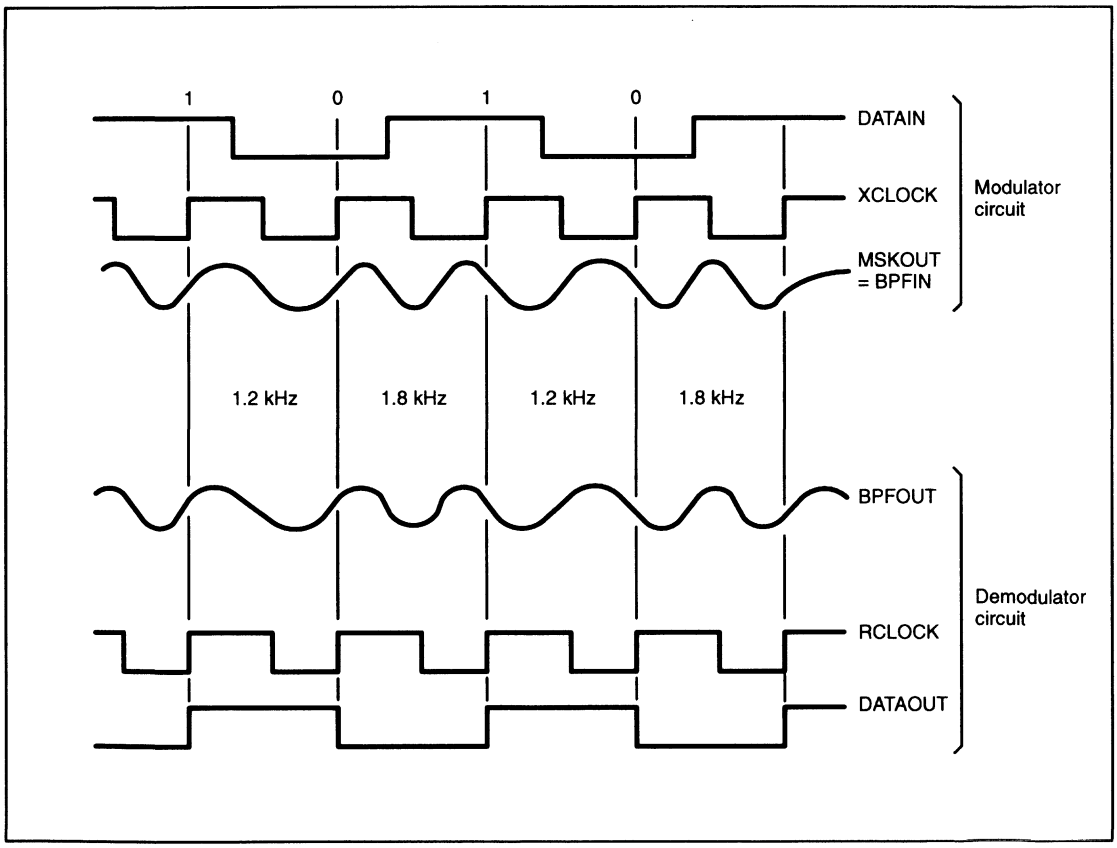
Demodulator timing chart (TEST pin = High or Open)



NOTE: 1. DATAOUT is output synchronized with the rising edge of the CLOCK.
2. When demodulator section is used, SEND pin must be set to high or low. When SEND pin is set to low, MSKOUT is fixed to 1/2 V_{DD}.
3. When power is first applied, RESET pin must be set to low to reset all circuits before use.

Clock output timing chart





3 PBX Products

FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-24100-4E

ASSP

PCM CODERS/DECODERS

MB6021A/MB6022A

■ DESCRIPTION

The Fujitsu CMOS MB6020A series consists of both μ-law and A-law single-chip coder/decoder (CODEC) filter ICs for either synchronous-only or synchronous/asynchronous operation. These monolithic, single-channel, voice-frequency CODECs incorporate both transmit and receive circuitries that are used for pulse coded modulation (PCM) systems.

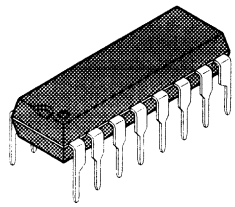
■ FEATURES

- Transmit high-pass and low-pass filters
- Receive low-pass filter with SinX/X Correction
- Anti-aliasing filter
- Conforms to CCITT and AT & T specifications
- Synchronous and asynchronous operation
- Serial data rates of 64 kHz to 3.152 MHz
- PLL circuits serve as an internal clock generator
- Internal voltage reference
- Internal auto-zero circuit
- TTL-compatible digital interface
- Input gain adjust amplifier

(Continued)

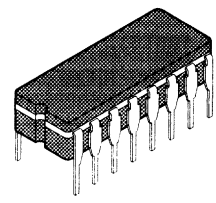
■ PACKAGE

Plastic DIP, 16 pin



(DIP-16P-M03)

Ceramic DIP, 16 pin

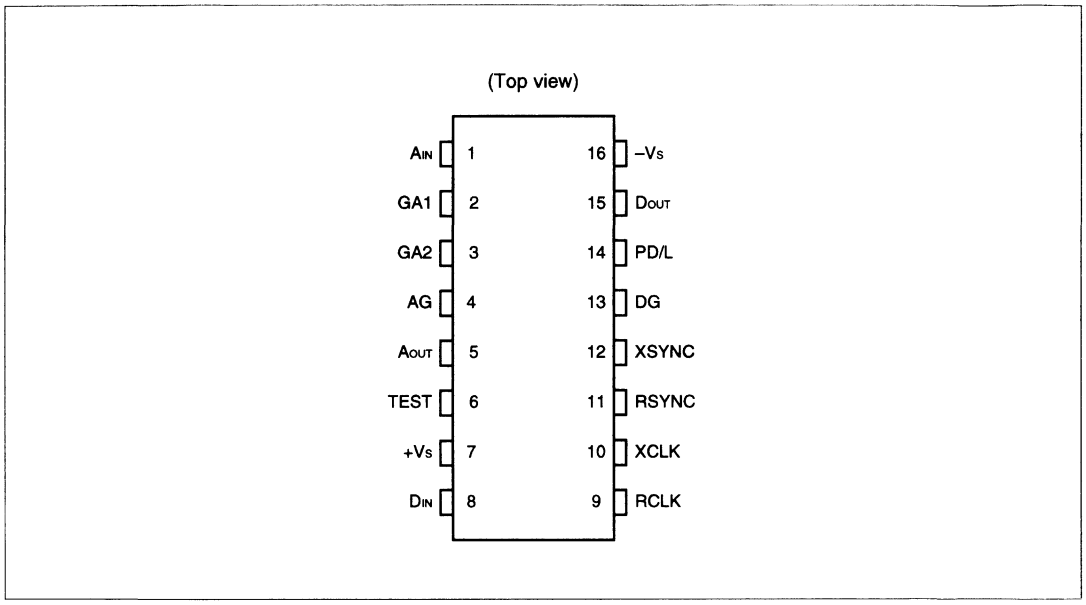


(DIP-16C-C04)

(Continued)

- Pin selectable on-chip analog loopback
- μ-law: MB6021A
  A-law: MB6022A
- Package and Ordering Information: 16-pin plastic DIP package
  Order as MB6021AP and MB6022AP

■ PIN ASSIGNMENT



■ PIN DESCRIPTION

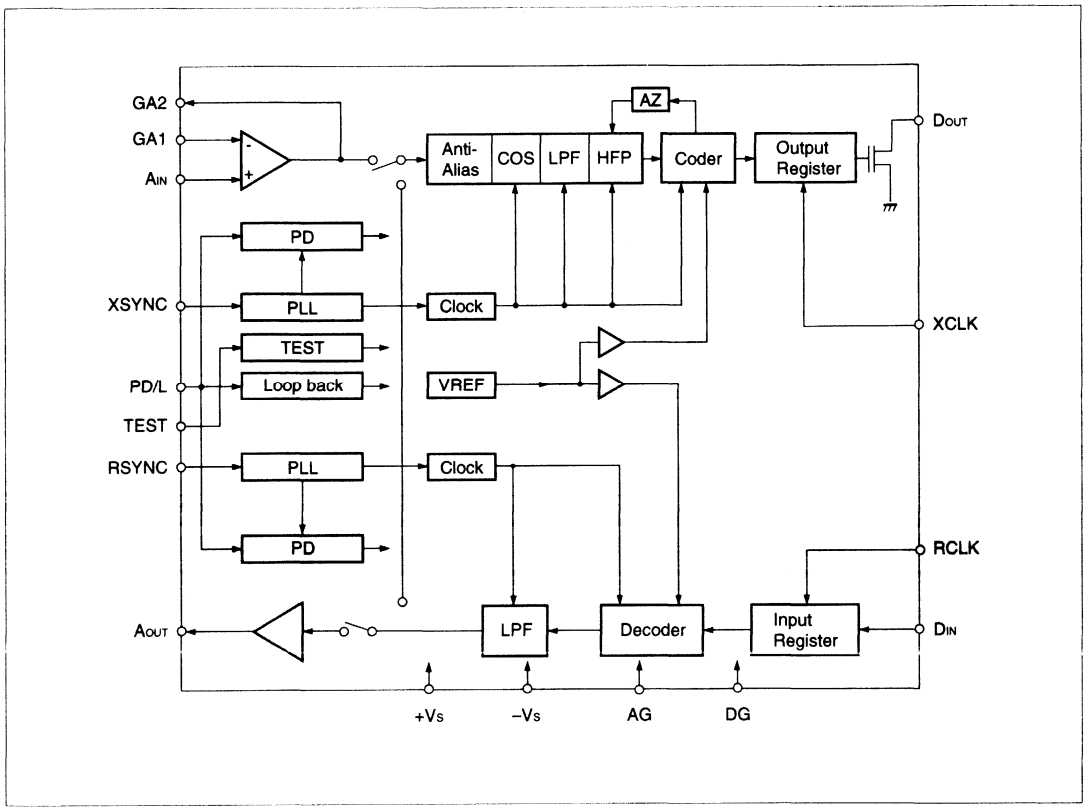
Pin No.	Pin Name	Description
1	A_{IN}	**Analog Input** This is an input pin for analog signals to be filtered and coded.
2 3	GA1 GA2	**Gain Adjust1** **Gain Adjust2** These pins are provided for adjusting the gain of the Transmit Section. GA1 and GA2 are the inverted input and output of the amplifier, respectively. GA2 can drive a load impedance of 10 to 20 kΩ and 50 pF or less.
4	AG	**Analog Ground** All analog signals are referenced to this pin.
5	A_{OUT}	**Analog Output** This pin outputs the decoded and filtered analog signals. It can drive a load impedance of 3 kΩ or greater, and 100 pF or less. This output is forced to AG level in the Analog Loopback Mode and Power-down Mode.
6	TEST	**Test** If this pin is at the TTL low level or left open, normal operating mode is selected. If it is connected to–Vs, the TEST mode is selected. In TEST mode, A_{IN} is internally connected to the coder input and its output is available on the D_{OUT} pin. Decoder output is available on the A_{OUT} pin. Applied voltage should not exceed 2.0 V.
7	+Vs	**Positive Voltage Supply:** +5 V ± 5%
8	D_{IN}	**Digital Input** This is a TTL-compatible input to the decoder and accepts an eight-bit data word into the shift register on the falling edge of RCLK.
9	RCLK	**Receive Clock** This TTL-compatible input defines the bit rate on the receive PCM highway. The device can operate with bit rates of 64 kHz to 3.152 MHz. The digital PCM codes accepted on the falling edge of the clock.
10	XCLK	**Transmit Clock** This TTL-compatible input defines the bit rate on the transmit PCM highway. The device can operate with bit rates of 64 kHz to 3.152 MHz. The digital PCM codes are shifted out of the digital output (D_{OUT}) pin on the rising edge of the XCLK.
11	RSYNC	**Receive Synchronization Clock** This TTL-compatible input defines the beginning of the recieve time slot on the receive PCM highway. It must be synchronized with RCLK. The clock rate is typically 8 kHz and its duration can be equal to or more than one RCLK cycle.
12	XSYNC	**Transmit Synchronization Clock** This TTL-compatible input defines the beginning of the transmit time slot on the transmit PCM highway. It must be synchronized with XCLK. The clock rate is typically 8 kHz and its duration can be equal to or more than one XCLK cycle.
13	DG	**Digital Ground** All digital signals are referenced to this pin.

(Continued)

(Continued)

Pin No.	Pin Name	Description
14	PD/L	**Power-down/Analog Loopback** This three-level input is provided for the selection of the Power-down Mode or Analog Loopback Mode. If this pin is at the TTL high level, the normal operation is selected. If this pin is at the TTL low level, the device is powered down regardless of the synchronization clocks. If this pin is connected to–Vs, the Analog Loopback Mode is selected. In this mode, the output of the receive filter is internally connected to the input of the transmit filter and AOUT is forced to AG level.
15	DOUT	**Digital Output** This is a TTL-compatible open-drain output. A pull-up resistor with greater than 0.5 kΩ must be connected to +Vs. PCM digital codes are shifted out of the device on the rising edges of XCLK in a serial format. This output goes into high-impedance state when eight bits are shifted out of the output shift register.
16	–Vs	**Positive Voltage Supply:** –5 V ± 5%

■ BLOCK DIAGRAM



■ FUNCTIONAL DESCRIPTION

Figure 1 shows a simplifed block diagram of MB6021A and MB6022A.

The Transmit Section in the upper-half of the block diagram is comprised of an input gain amplifier, an anti-aliasing filter (Anti-Alias), a band-pass filter (COS, LPT, and HPF), and a compressing coder(Coder). An auto-zero circuit (AZ) is also included in this section. The Receive Section in the lower half of the block diagram is comprised of an expanding decoder (Decoder) and a low-pass filter (LPF).

Transmit Section

The Transmit Section receives analog signals that are input to an operational amplifier to provide gain adjustment. The signal from the op amp is transmitted to a second-order analog anti-aliasing filter (Anti-Alias). This filter provides attenuation of 40 dB (typical) at the 256 kHz effective clock frequency of the switched capacitor cosine filter (COS). From the cosine filter, the signals enter a fifth-order low-pass filter (LPF) clocked at 128 kHz. From the LPF, the signals pass into a third-order high-pass filter (HPF) clocked at 128 kHz. The resulting band-pass characteristics meet both the D3/D4 specification and the CCIT G. 712 recommendation. The output of the high-pass filter is then sampled by the coder (Coder) at 8 kHz. This coder transforms the analog signals into 8-bit words using compression law. The encoded PCM data is then output serially from the Output Register at a frequency determined by the external clock, 64 kHz to 3.152 MHz. An auto-zero circuit (AZ) is utilized for DC offset correction.

Receive Section

The Receive Section's Input Register filter smooths the decoded signals and corrects for SinX/X attenuation caused by the 8 kHz sample and hold operation. The decoder reconstructs the analog signals from the PCM data using expansion law. The output from the decoder is transmitted to a fifth-order low-pass filter (LPF). This LPF smooths the decoded signals and corrects them for the SinX/X attenuation due to the 8 kHz sampling and holding operation.

Internal Clocks

Two independent phase locked loops (PLLs) generate internal clocks for the Transmit and Receive Sections from the respective synchronization clocks (XSYNC and RSYNC).

■ OPERATING MODES

Analog Loopback Mode

The Analog Loopback Mode allows all decoding and coding functions to be exercised without using the analog input (A_{IN}) and analog output (A_{OUT}). In this mode, a digital input signal is decoded and internally routed to the transmit filters. The output is available from the digital output (D_{OUT}). The analog output (A_{OUT}) is forced to the analog ground (AG) level. The Analog Loopback Mode is selected by connecting the PD/L input to the negative supply voltage (−Vs).

Power-down Mode

Two Power-down Modes are provided. The Transmit and Receive Sections independently go into power-down operation in the absence of the respective synchronization clocks (XSYNC and RSYNC). If the external power down input (PD/L) is connected to a TTL low level, both the Transmit and Receive Sections are powered down regardless of the synchronization clocks. During power-down operation, A_{OUT} is forced to the level of AG, and D_{OUT} goes into a high-impedance state.

Test Mode

In the Test Mode the TEST pin is connected to −Vs. The Test Mode allows independent evaluation of the coder and decoder. In this mode, A_{IN} is internally connected to the input of the coder and its output is available on the D_{OUT} pin. The output of the decoder is made available on the A_{OUT} pin.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Pin No.	Symbol	Rating		Unit
			Min.	Max.	
Positive supply voltage	7	$+V_S$	−0.3	7	V
Negative supply voltage	16	$-V_S$	−7	0.3	V
Test	6	TEST	$-V_S$	$+V_S$	V
Analog input voltage	1	V_{AIN}	$-V_S - 0.3$	$+V_S + 0.3$	V
Digital input voltage	8, 9, 10, 11, 12	V_{DIN1}	−0.3	$+V_S + 0.3$	V
Digital input voltage	6, 14	V_{DIN2}	$-V_S - 0.3$	$+V_S + 0.3$	V
Storage temperature	—	Tstg	−55	150	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Pin No.	Symbol	Value			Unit
			Min.	Typ.	Max.	
Positive supply voltage	7	$+V_S$	+4.75	+5.0	+5.25	V
Negative supply voltage	16	$-V_S$	−5.25	−5.0	−4.75	V
Digital output load resistance	15	R_{DL}	0.5	—	—	kΩ
Digital output load capacitance	15	C_{DL}	—	—	144	pF
Analog output load resistance	5	R_L	3	—	—	kΩ
Analog output load capacitance	5	C_L	—	—	100	pF
Operating temperature	—	T_{OP}	0	25	70	°C

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

Recommended operating conditions unless otherwise noted.

Parameter	Symbol	Pin No.	Conditions	Value			Unit
				Min.	Typ.	Max.	
Positive supply current	$+I_{VS}$	7	Operating	—	7.0	10.0	mA
Negative supply current	$-I_{VS}$	16	Operating	−10.0	−5.0	—	mA
Positive supply current power down mode	$+I_{VSST}$	7	XSYNC= RSYNC=V_{IL} SYNC=V_{IL}	—	1.0	2.0	mA
			PD/L = V_{IL}	—	0.3	1.0	mA
Negative supply current power down mode	$-I_{VSST}$	16	XSYNC= RSYNC=V_{IL} SYNC=V_{IL}	−0.5	−0.1	—	mA
			PD/L = V_{IL}	−0.5	−0.1	—	mA
Digital input high voltage	V_{IH}	8, 9, 10, 11, 12, 14		2.0	—	+VS	V
Digital input low voltage	V_{IL}	8, 9, 10, 11,12,14		0	—	0.8	V
Digital input high current	I_{IH}	8, 9, 10, 11, 12, 14		—	—	10	μA
Digital input low current	I_{IL}	8, 9, 10, 11,12,14		−10	—	—	μA
Digital input capacitance	C_{DIN1}	8, 9, 10, 11,12,14		—	—	10	pF
Digital input capacitance	C_{DIN2}	—		—	—	20	pF
Digital output low voltage	V_{OL1}	15	R_{DL}=0.5 kΩ $+I_{OL}$ =0.4 mA	—	—	0.4	V
Digital output leakage current	I_{LO}	15		—	—	10	μA
Digital output capacitance	C_{DOUT}	15		—	—	12	pF
Analog input offset voltage	A_{INOFF}	1		−200	0	200	mV
Analog input resistance	R_{AIN}	1		300	—	—	kΩ
Analog input capacitance	C_{AIN}	1		—	—	10	pF
Analog output offset voltage	A_{OUTOFF}	5		−150	—	150	mV
Analog output resistance	R_{AOUT}	5		—	10	30	Ω
Pull down current	I_{PLD}	6	V_{IN} =+0.2 V	0	—	80	μA

2. AC Characteristics

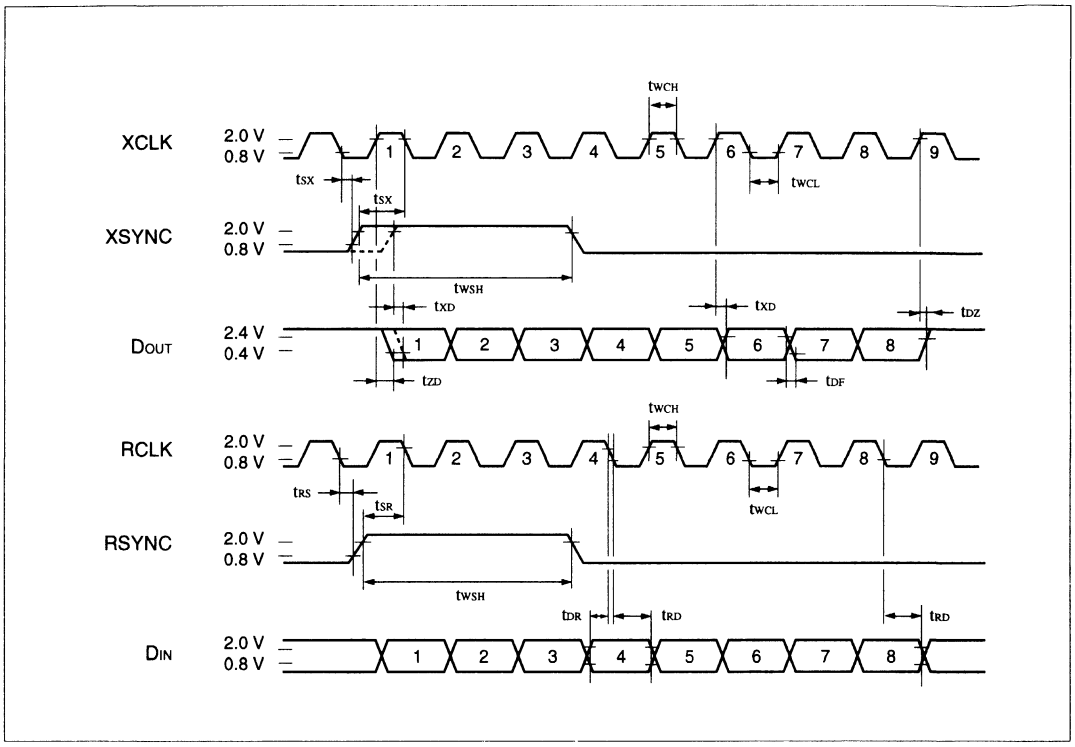
Recommended operating conditions unless otherwise noted.

Parameter	Symbol	Pin No.	Conditions	Value			Unit
				Min.	Typ.	Max.	
Digital input rise time	t_r	8, 9, 10, 11, 12	0.8V → 2.0V	—	—	50	ns
Digital input fall time	t_f	8, 9, 10, 11, 12	2.0V → 0.8V	—	—	50	ns
Shift clock frequency	F_C	9, 10	—	64	—	3152	kHz
Shift clock high width	t_{WCH}	9, 10	V_{IH} = 2.0 V	140	—	—	ns
Shift clock low width	t_{WCL}	9, 10	V_{IL} = 0.8 V	140	—	—	ns
Synchronization frequency	F_S	11, 12	—	—	8	—	kHz
Synchronization high width	t_{WSH}	11,12	V_{IH} = 2.0 V	1/F_C F_C:MHz	—	117	µA
XSYNC to XCLK delay	t_{SX}	10,12	—	100	—	—	ns
XCLK to XSYNC delay	t_{XS}	10,12	—	50	—	—	ns
RSYNC to RCLK delay	t_{SR}	9, 11	—	100	—	—	ns
RCLK to RSYNC delay	t_{RS}	9, 11	—	50	—	—	ns
RCLK to D_{IN} delay	t_{RD}	8,9	—	50	—	—	ns
D_{IN} to RCLK delay	t_{DR}	8,9	—	50	—	—	ns
XCLK or XSYNC to D_{OUT} delay*1	t_{ZD}	10, 12, 15	—	30	—	200	ns
XCLK to D_{OUT} delay*2	t_{XD}	10, 15	—	30	—	200	ns
XCLK to D_{OUT} disable time	t_{DZ}	10, 15	High-Z	30	—	200	ns
D_{OUT} fall time	t_{DF}	15	—	10	—	100	ns

*1: Bit 1 D_{OUT} load conditions: R_{DL} = 0.5kΩ, C_{DL} = 144 pF, +I_{OL} = 0.4 mA

*2: Bit 2 to 8 D_{OUT} load conditions: R_{DL} = 0.5 kΩ, C_{DL} =144 pF, +I_{OL} = 0.4 mA

■ TIMING DIAGRAM



■ TRANSMISSION CHARACTERISTICS OF μ-LAW (MB6021A)

Recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions		Value			Unit
				Min.	Typ.	Max.	
Signal to distortion (A to A)	SDA	1020 Hz tone (C message)	+3 to –30 dBm0	35.0	—	—	dB
			–40 dBm0	30.0			dB
			–45 dBm0	25.0			dB
Signal to distortion (A to D)	SDX	1020 Hz tone (C message)	+3 to –30 dBm0	36.0	—	—	dB
			–40 dBm0	31.0			dB
			–45 dBm0	26.0			dB
Signal to distortion (D to A)	SDR	1020 Hz tone (C message)	+3 to –30 dBm0	36.0	—	—	dB
			–40 dBm0	31.0			dB
			–45 dBm0	26.0			dB
Gain tracking (A to A)	GTA	1020 Hz tone	+3 to –40 dBm0	–0.4	—	0.4	dB
			–40 to –50 dBm0	–0.8		0.8	dB
			–50 to –55 dBm0	–2.0		2.0	dB
Gain tracking (A to D)	GTX	1020 Hz tone	+3 to –40 dBm0	–0.2	—	0.2	dB
			–40 to –50 dBm0	–0.4		0.4	dB
			–50 to –55 dBm0	–0.8		0.8	dB
Gain tracking (D to A)	GTR	1020 Hz tone	+3 to –40 dBm0	–0.2	—	0.2	dB
			–40 to –50 dBm0	–0.4		0.4	dB
			–50 to –55 dBm0	–0.8		0.8	dB
Frequency response (A to A)	FRA	Relative to 0 dBm0, 820 Hz	0 to 60 Hz	24.0	—		dB
			60 to 300 Hz	–0.2			dB
			300 to 3000 Hz	–0.2			dB
			3000 to 3400 Hz	–0.2		0.3	dB
			3400 to 4600 Hz	Note 1		1.6	dB
			4.6 to 12 kHz	64.0			dB
Frequency response (A to D)	FRX	Relative to 0 dBm0, 820 Hz	0 to 60 Hz	24.0	—		dB
			60 to 300 Hz	–0.1			dB
			300 to 3000 Hz	–0.1		0.15	dB
			3000 to 3400 Hz	–0.1		0.8	dB
			3400 to 4600 Hz	Note 2			dB
			4.6 to 12 kHz	32.0			dB
Frequency response (D to A)	FRR	Relative to 0 dBm0, 820 Hz	0 to 300 Hz	–0.1	—		dB
			300 to 3000 Hz	–0.1		0.15	dB
			3000 to 3400 Hz	–0.1		0.8	dB
			3400 to 4600 Hz	Note 2			dB
			4.6 to 12 kHz	32.0			dB

(Continued)

Notes: 1. $29\left(1 - \mathrm{Sin}\frac{\pi\,(4000-f)}{1200}\right)$

2. $29\left(1 - \mathrm{Sin}\frac{\pi\,(4000-f)}{1200}\right)$

(Continued)

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Idle channel noise (A to A)	ICNA	C message	—	–80	–72.0	dBm0c
Idle channel noise (A to D)	ICNX	C message	—	–83	–74.0	dBm0c
Idle channel noise (D to A)	ICNR	C message	—	–83	–78.0	dBm0c
Crosstalk (A to A)	CTA	1020 Hz, 0dBm0	—	—	–66	dB
Crosstalk (D to D)	CTD	1020 Hz, 0dBm0	—	—	–66	dB
Absolute level	VABS	Overload Level 3.17 dBm0	—	2.500	—	V_{OP}
Analog input level	AIL	1020 Hz, 0dBm0 ±Vs = ±5.0 V, Ta = 25°C	—	1.227	—	V_{rms}
Analog output level	AOL	1020 Hz, 0dBm0 ±Vs = ±5.0 V, Ta = 25°C	1.206	1.227	1.248	V_{rms}
Gain accuracy (A to A)	GAA	1020 Hz, 0dBm0 Internal VREF	–0.5	0	+0.5	dB
		±Vs = ±5.0 V, Ta = 25°C	–0.3	0	+0.3	dB
Gain accuracy (A to D)	GAX	1020 Hz, 0dBm0 Internal VREF	–0.25	0	+0.25	dB
		±Vs = ±5.0 V, Ta = 25°C	–0.15	0	+0.15	dB
		Variation with power supply	—	±0.02	—	dB
		Variation with temperature	—	±0.001	—	dB/°C
Gain accuracy (D to A)	GAR	1020 Hz, 0dBm0 Internal VREF	–0.25	0	+0.25	dB
		±Vs = ±5.0 V, Ta = 25°C	–0.15	0	+0.15	dB
		Variation with power supply		±0.02		dB
		Variation with temperature		±0.001		dB/°C
Propagation delay (A to A)	PDA	FC ≥ 1544 kHz	—	—	540	µs
Delay to distortion (A to A)	DDA	500 to 600 Hz	—	—	1.5	ms
		600 to 1000 Hz			0.75	ms
		1000 to 2600 Hz			0.25	ms
		2600 to 2800 Hz			1.5	ms
		1020 Hz, 0dBm0 Relative to minimum delay				

(Continued)

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Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
PSRR (+VS) (A to A)	PSRRA+	0 < f ≤ 50 kHz Idle Channel Noise (C Message) +V_S +50 m V_{OP} A_{IN} = AG	25	30	—	dB
PSRR (–VS) (A to A)	PSRRA–	0 < f ≤ 50 kHz Idle Channel Noise (C Message) –V_S +50 m V_{OP} A_{IN} = AG	35	40	—	dB
Intermoduration (A to A)	IMA1	A_{IN} a. 0.47 kHz, –10 dBm0 b. 0.32 kHz, –10 dBm0 A_{OUT} (2a – b)	—	—	–38	dB
Intermoduration (A to A)	IMA2	A_{IN} a. 1.02 kHz, –9 dBm0 b. 0.05 kHz, –23 dBm0 A_{OUT} (a – b)	—	—	–52	dBm0
Signal frequency noise (A to A)	SFNA	0 to 4 kHz 4 to 200 kHz A_{IN} = AG	—	—	–70 –50	dBm0 dBm0
Discrimination (A to A)	DISA	A_{IN} = 0dBm0 4.6 to 200 kHz	30	—	—	dB
In band spurious (A to A)	IBSA	2nd, 3rd Harmonic A_{IN} = 0dBm0, 700 – 1100 Hz	43	—	—	dB

■ TRANSMISSION CHARACTERISTICS OF A-LAW (MB6022A)

Recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions		Value			Unit
				Min.	Typ.	Max.	
Signal to distortion (A to A)	SDA	CCITT G.712 Method 2 1020 Hz tone P Message	+3 to −30 dBm0 −40 dBm0 −45 dBm0	35.0 30.0 25.0	—	—	dB dB dB
		CCITT G.712 Method 1	−3 dBm0 −6 to −27 dBm0 −34 dBm0 −40 dBm0 −55 dBm0	28.0 35.5 33.5 28.5 13.5	—	—	dB dB dB dB dB
Signal to distortion (A to D)	SDX	CCITT G.712 Method 2 1020 Hz tone P Message	+3 to −30 dBm0 −40 dBm0 −45 dBm0	36.0 31.0 26.0	—	—	dB dB dB
		CCITT G.712 Method 1	−3 dBm0 −6 to −27 dBm0 −34 dBm0 −40 dBm0 −55 dBm0	30.0 36.0 34.0 29.5 14.5	—	—	dB dB dB dB dB
Signal to distortion (D to A)	SDR	CCITT G.712 Method 2 1020 Hz tone P Message	+3 to −30 dBm0 −40 dBm0 −45 dBm0	36.0 31.0 26.0	—	—	dB dB dB
		CCITT G.712 Method 1	−3 dBm0 −6 to −27 dBm0 −34 dBm0 −40 dBm0 −55 dBm0	30.0 36.0 34.0 29.5 14.5	—	—	dB dB dB dB dB
Gain tracking (A to A)	GTA	CCITT G.712 Method 2 1020 Hz tone	+3 to −30 dBm0 −40 to −50 dBm0 −50 to −55 dBm0	−0.4 −0.8 −2.0	—	0.4 0.8 2.0	dB dB dB
		CCITT G.712 Method 1	−10 to −50 dBm0 −55 to −60 dBm0	−0.5 −1.0	—	0.5 1.0	dB dB
Gain tracking (A to D)	GTX	CCITT G.712 Method 2 1020 Hz tone	+3 to −30 dBm0 −40 to −50 dBm0 −50 to −55 dBm0	−0.2 −0.4 −0.8	—	0.2 0.4 0.8	dB dB dB
		CCITT G.712 Method 1	−10 to −50 dBm0 −50 to −55 dBm0 −55 to −60 dBm0	−0.25 −0.4 −0.8	—	0.25 0.4 0.8	dB dB dB

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Parameter	Symbol	Conditions		Value			Unit
				Min.	Typ.	Max.	
Gain tracking (D to A)	GTR	CCITT G.712 Method 2 1020 Hz tone	+3 to –40 dBm0	–0.2	—	0.2	dB
			–40 to –50 dBm0	–0.4		0.4	dB
			–50 to –55 dBm0	–0.8		0.8	dB
		CCITT G.712 Method 1	–10 to –50 dBm0	–0.25	—	0.25	dB
			–50 to –55 dBm0	–0.4		0.4	dB
			–55 to –60 dBm0	–0.8		0.8	dB
Frequency response (A to A)	FRA	0 to 60 Hz		24.0	—		dB
		60 to 300 Hz		–0.2			dB
		300 to 3000 Hz		–0.2		0.3	dB
		3000 to 3400 Hz		–0.2		1.6	dB
		3400 to 4600 Hz		Note 1			dB
		4.6 to 12 kHz		64.0			dB
		Relative to 0dBm0, 820 Hz					
Frequency response (A to D)	FRX	0 to 60 Hz		24.0	—		dB
		60 to 300 Hz		–0.1			dB
		300 to 3000 Hz		–0.1		0.15	dB
		3000 to 3400 Hz		–0.1		0.8	dB
		3400 to 4600 Hz		Note 2			dB
		4.6 to 12 kHz		32.0			dB
		Relative to 0dBm0, 820 Hz					
Frequency response (D to A)	FRR	0 to 300 Hz		–0.1	—		dB
		300 to 3000 Hz		–0.1		0.15	dB
		3000 to 3400 Hz		–0.1		0.8	dB
		3400 to 4600 Hz		Note 2			dB
		4.6 to 12 kHz		32.0			dB
		Relative to 0dBm0, 820 Hz					

(Continued)

Notes: 1. $29\left(1 - \mathrm{Sin}\frac{\pi(4000-f)}{1200}\right)$

2. $29\left(1 - \mathrm{Sin}\frac{\pi(4000-f)}{1200}\right)$

(Continued)

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Idle channel noise (A to A)	ICNA	P Message	—	–80	–72.0	dBm0p
Idle channel noise (A to D)	ICNX	P Message	—	–83	–74.0	dBm0p
Idle channel noise (D to A)	ICNR	P Message	—	–83	–78.0	dBm0p
Crosstalk (A to A)	CTA	1020 Hz, 0dBm0	—	—	–66	dB
Crosstalk (D to D)	CTD	1020 Hz, 0dBm0	—	—	–66	dB
Absolute level	VABS	Overload Level 3.14 dBm0	—	2.500	—	V_{OP}
Analog input level	AIL	1020 Hz, 0dBm0 Internal VREF $\pm V_S$ = ±5.0 V, Ta 25°C	—	1.231	—	V_{rms}
Analog output level	AOL	1020 Hz, 0dBm0 Internal VREF $\pm V_S$ = ±5.0 V, Ta 25°C	1.210	1.231	1.252	V_{rms}
Gain accuracy (A to A)	GAA	1020 Hz, 0dBm0 Internal VREF	–0.5	0	+0.5	dB
		$\pm V_S$ = ±5.0 V, Ta 25°C	–0.3	0	+0.3	dB
Gain accuracy (A to D)	GAX	1020 Hz, 0dBm0 Internal VREF	–0.25	0	+0.25	dB
		$\pm V_S$ = ±5.0 V, Ta 25°C	–0.15	0	+0.15	dB
		Variation with power supply	—	±0.02	—	dB
		Variation with temperature	—	±0.001	—	dB/°C
Gain accuracy (D to A)	GAR	1020 Hz, 0dBm0 Internal VREF	–0.25	0	+0.25	dB
		$\pm V_S$ = ±5.0 V, Ta 25°C	–0.15	0	+0.15	dB
		Variation with power supply	—	±0.02	—	dB
		Variation with temperature	—	±0.001	—	dB/°C
Propagation delay (A to A)	PDA	FC ≥ 1544 kHz	—	—	540	µs

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(Continued)

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Delay to distortion (A to A)	DDA	500 to 600 Hz 600 to 1000 Hz 1000 to 2600 Hz 2600 to 2800 Hz 1020 Hz, 0dBm0 Relative to minimum delay	— — — —	— — — —	1.5 0.75 0.25 1.5	ms ms ms ms
PSRR (+VS) (A to A)	PSRRA+	0 < f ≤ 50 kHz Idle channel noise (P Message) +V_S +50 m V_{OP} A_{IN} = AG	25	30	—	dB
PSRR (–VS) (A to A)	PSRRA–	0 < f ≤ 50 kHz Idle channel noise (P Message) +V_S +50 m V_{OP} A_{IN} = AG	35	40	—	dB
Intermoduration (A to A)	IMA1	A_{IN} a. 0.47 kHz, –10 dBm0 b. 0.32 kHz, –10 dBm0 A_{OUT} (2a – b)	—	—	–38	dB
Intermoduration (A to A)	IMA2	A_{IN} a. 1.02 kHz, –9 dBm0 b. 0.05 kHz, –23 dBm0 A_{OUT} (a – b)	—	—	–52	dBm0
Signal frequency noise (A to A)	SFNA	0 to 4 kHz 4 kHz to 200 kHz A_{IN} = AG	— —	— —	–70 –50	dBm0 dBm0
Discrimination (A to A)	DISA	A_{IN} = 0dBm0 4.6 kHz to 200 kHz	30	—	—	dB
In band spurious (A to A)	IBSA	2nd, 3rd harmonic A_{IN} = 0dBm0, 700 to 1100 Hz	43	—	—	dB

MEMO

4 Wireless Communication Products

FUJITSU SEMICONDUCTOR
DATA SHEET

DS04–21600–3E

ASSP for DTS

BIPOLAR

Prescaler with VCO (Dual-Modulus, 1.0 GHz)

MB551

■ DESCRIPTION

The MB551 is a dual-modulus prescaler incorporating a voltage controlled oscillator (VCO) used for 900-MHz band frequency synthesizers. The MB551 consists of: a Colpitts oscillator with grounded base capacitor, a buffer amplifier with collector open output, a prescaler interface circuit, and a dual-modulus prescaler operating at frequencies divided by 128/129. The oscillator block accommodates external components such as a capacitor, a dielectric oscillator (resonator), and a variable capacitor, making up the VCO.

The VCO and the prescaler are connected by an internal control circuit, minimizing the effects of prescaler input load variation on VCO characteristics such as a C/N ratio.

The MB551 operates at 5 V (typical) and draws 16 mA of current (typical).

■ FEATURES

- Oscillator frequency: 1 GHz (Max)
- Low power consumption: Icc = 16 mA (Typical)
- Oscillator output power: 0 dBm (Typical)
- C/N ratio: 70 dB (Typical) Measurement conditions: Δf = 50 kHz, BW = 15 kHz
  65 dB (Typical) Measurement conditions: Δf = 25 kHz, BW = 15 kHz
- S/N ratio: 45 dB (Typical) Measurement conditions: BW = 0.3 to 3 kHz, 3 kHz.Dev, 1 kHz Tone
- Stable oscillator output
  Supply voltage dependence: ±200 kHz/V (Typical)
  Frequency stability: 35 ppm/°C (Typical)

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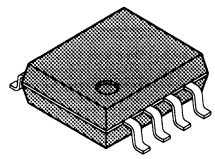
■ PACKAGE

8 pin Plastic SOP

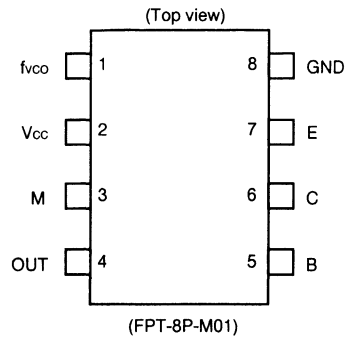


(FPT-8P-M01)

(Continued)

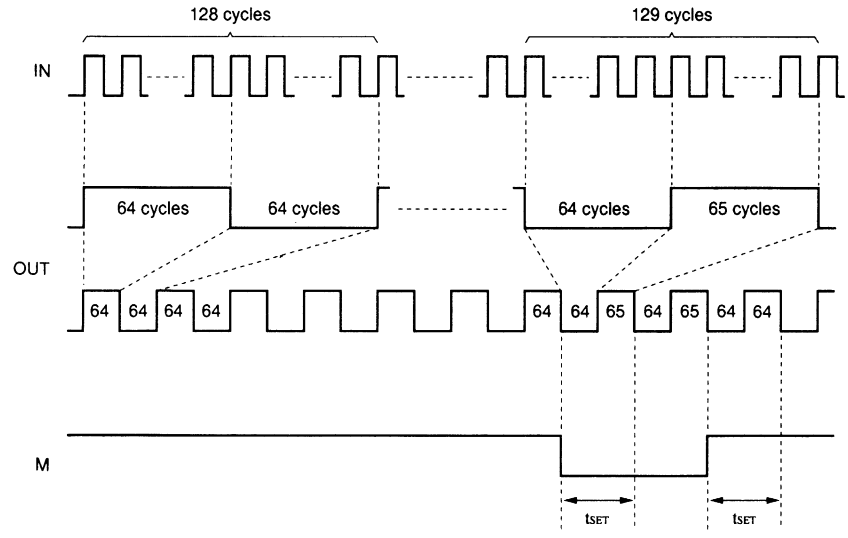
- Pulse swallow method: Division-by-128/129 prescaler
- Prescaler output with termination circuit: V_I = 1.6 V_{P-P}

■ PIN ASSIGNMENT



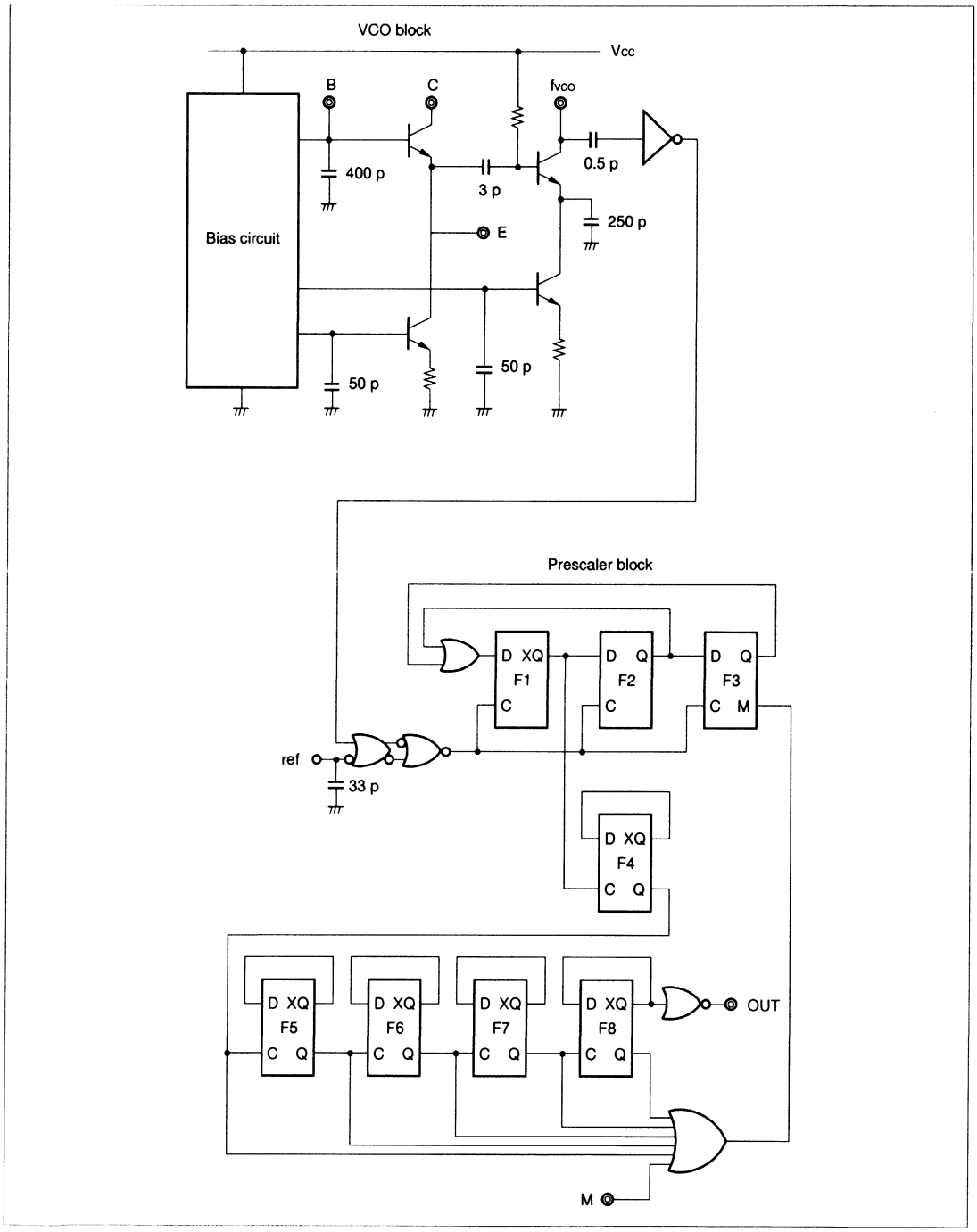
Pin No.	Symbol	Function
1	fvco	VCO signal pin
2	Vcc	Power supply pin
3	M	Module setting pin
4	OUT	Prescaler output pin
5	B	Oscillator transistor base pin
6	C	Oscillator transistor collector pin
7	E	Oscillator transistor emitter pin
8	GND	Ground pin

■ TIMING DIAGRAM (Example of Dual-modulus, division-by-128/129 type)



- M pin = High: Division by 128
  M pin = Low: Division by 129
  (V_{IH} = 2.0 V min, V_{IL} = 0.8 V max.)
- Division plus one makes the high-to-low transition longer by one cycle of the frequency-divided signal.
- Setup time (t_{SET}) from input of the M signal to change in the divide ratio of the prescaler is 16 ns (typical).

■ BLOCK DIAGRAM



■ MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Remarks
Supply voltage	V_{CC}	−0.5 to +7.0	V	
Oscillator transistor base/ emitter applied voltage	V_B, V_E	—	—	Do not apply external DC voltage to the base or emitter pin.
M/OUT (Pin 3/4) applied voltage	V_{P1}	−0.5 to V_{CC} + 0.5	V	
fVCO/C (Pin 1/6) applied voltage	V_{P2}	$V_{CC} \leq V_{P2} < +7.0$	V	
Applied current	I_P	±10	mA	
Storage temperature	Tstg	−55 to +125	°C	

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
External variable capacitor control voltage	V_T	1.5	—	4.5	V	
Operating temperature	Ta	−40	—	+85	°C	
Prescaler output load	CL	—	—	8	pF	

■ ELECTRICAL CHARACTERISTICS

1. VCO Block

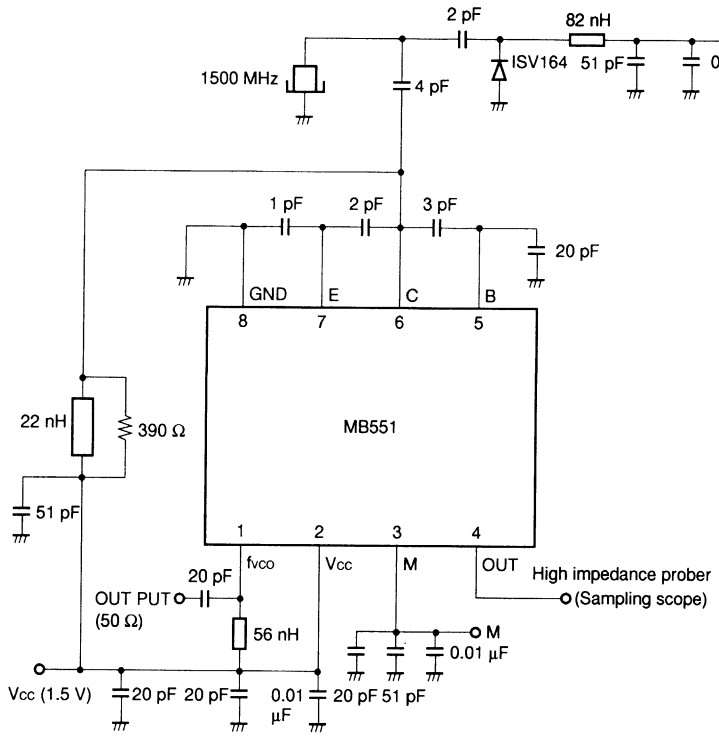
Parameter	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
Oscillator frequency	fosc	—	—	1000	MHz	
Oscillator output	Pout	—	0	—	dBm	
C/N ratio	C/N	—	70	—	dB	Df = 50 kHz, BW = 15 kHz
			65	—	dB	Df = 25 kHz, BW = 15 kHz
S/N ratio	S/N	—	45	—	dB	BW = 0.3 to 3 kHz, 3 kHz, Dev, Tone 1 kHz
Fundamental/1st harmonic ratio	SP–1	—	–10	—	dB	
Frequency stability	Δft	—	35	—	ppm/°C	–40 to 85°C, 25°C (Typical)
Supply voltage variation	Δfr	—	±200	—	kHz/V	5 V ± 10 %
Conversion gain	Δfosc	—	4	—	MHz/V	Control range: 1.0 to 4.0 V

Note: Electrical characteristics depend on external components and mounting conditions. These values are reference values assuming the test circuit examples on pages 6 and 7.

2. Prescaler Block

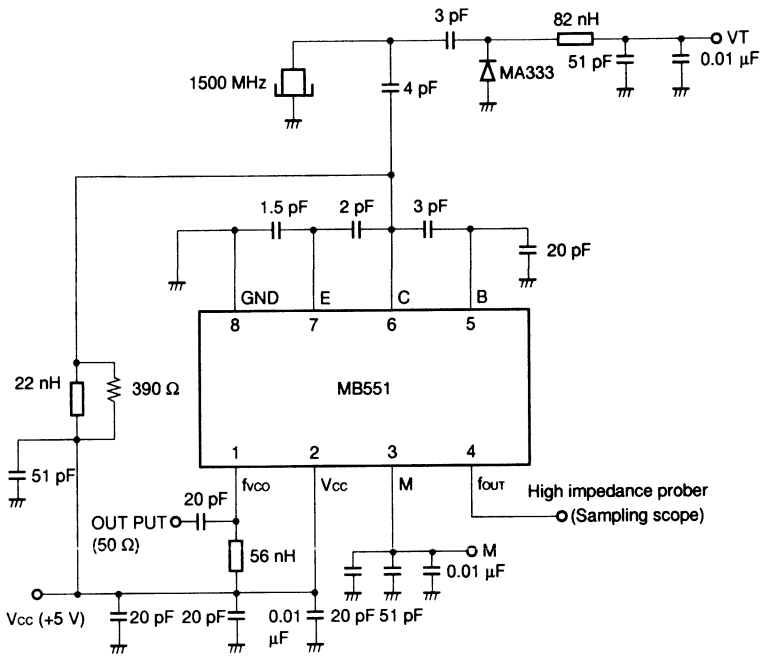
Parameter	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
Supply current	I_{CC}	—	16.0	—	mA	
Output amplitude	V_{OUT}	1.0	1.6	—	V_{P-P}	Load capacitance when internal termination pin is used: 8 pF or less
Response frequency	f_{in}	—	—	1000	MHz	
Allowable input power	V_{in}	–4	—	+10	dBm	
High-level input voltage (MC)	V_{IH}	2.0	—	—	V	
	V_{IL}	—	—	0.8	V	
High-level input current (MC)	I_{IH}	—	—	0.4	mA	
	I_{IL}	–0.2	—	—	mA	
Module setup time	t_{SET}	—	16	26	ns	

■ TEST CIRCUIT EXAMPLE 1



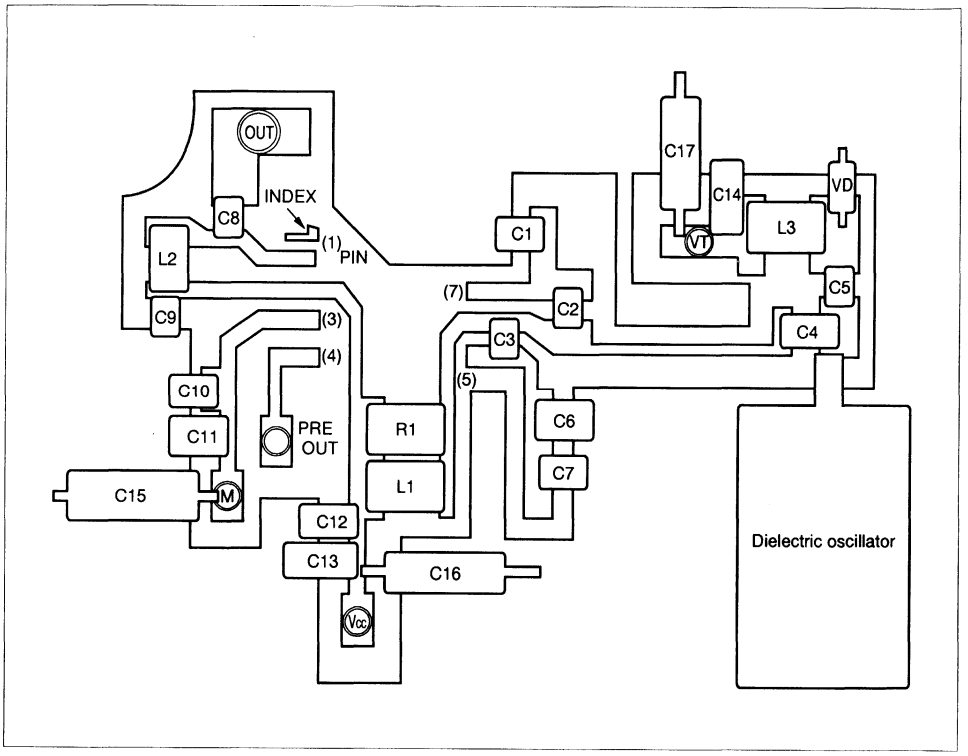
Chip capacitor: UMK316C, UMK212C, UCN103C Series (Taiyo Yuden)
Chip coil: LQN2A Series (Murata Works)
Dielectric oscillator: DRR060UE (Murata Works)
Varicap: ISV164 (NEC)

■ TEST CIRCUIT EXAMPLE 2



Chip capacitor: UMK316C Series (Taiyo Yuden)
Chip coil: LQN2A Series (Murata Works)
Dielectric oscillator: DRR060UE (Murata Works)
Varicap: MA333 (Mitsubishi Electric)

■ RECOMMENDED PC BOARD PATTERN



[Mounted component list]

C1: 1 pF (Taiyo Yuden UMK212C)
C2: 2 pF (Taiyo Yuden UCN103C)
C3: 3 pF (Taiyo Yuden UMK212C)
C4: 4 pF (Taiyo Yuden UMK212C)
C5: 2 pF (Taiyo Yuden UMK212C)
C6: 20 pF (Taiyo Yuden UMK316C)
C7: 51 pF (Taiyo Yuden UMK212C)
C8: 20 pF (Taiyo Yuden UMK316C)
C9: 20 pF (Taiyo Yuden UMK316C)
C10: 51 pF (Taiyo Yuden UMK212C)
C11: 20 pF (Taiyo Yuden UMK316C)
C12: 51 pF (Taiyo Yuden UMK212C)
C13: 20 pF (Taiyo Yuden UMK316C)
C14: 51 pF (Taiyo Yuden UMK212C)

C15: 0.01 μF (Film capacitor)
C16: 0.01 μF (Film capacitor)
C17: 0.01 μF (Film capacitor)

R1: 390 Ω (Rohm MCR25)

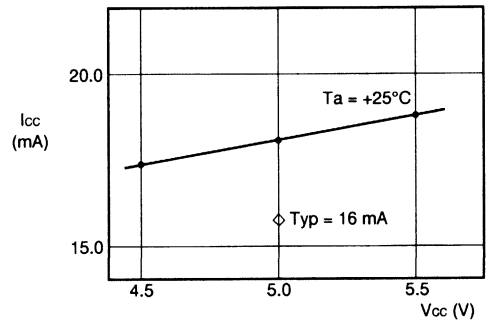
L1: 22 nH (Murata Works LQN2A)
L2: 56 nH (Murata Works LQN2A)
L3: 82 nH (Murata Works LQN2A)

VD: 1SV164 (NEC)

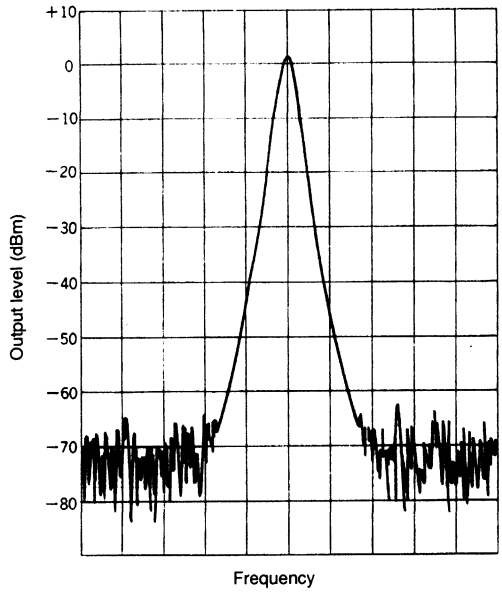
Dielectric oscillator: (Murata Works DRR060 Series, 1.5 GHz)

■ MEASUREMENT RESULTS

(1) Supply Current

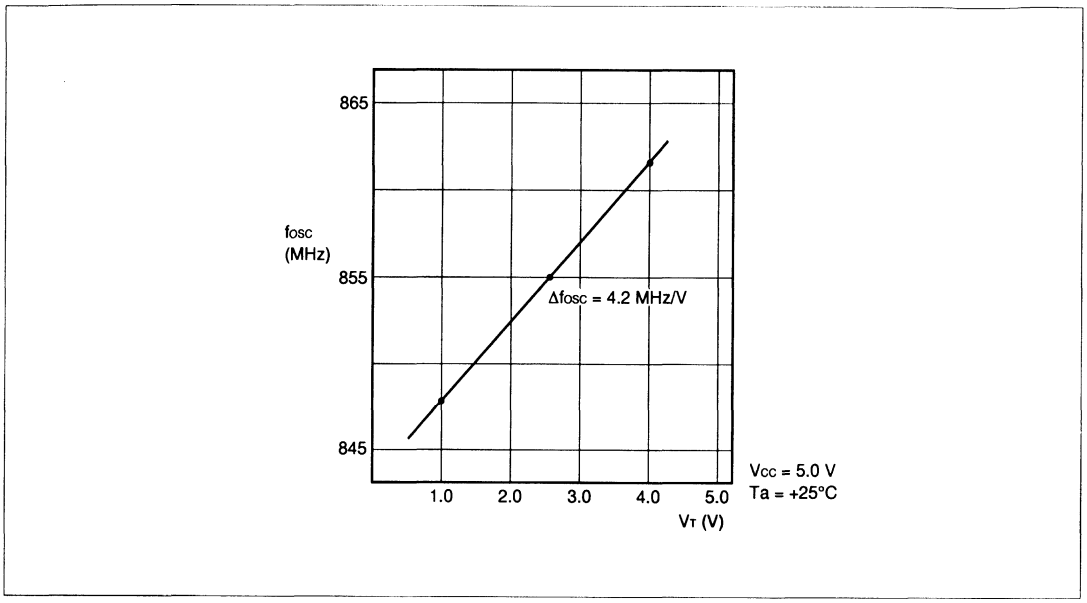


(2) Oscillation Waveform (50-kHz span)

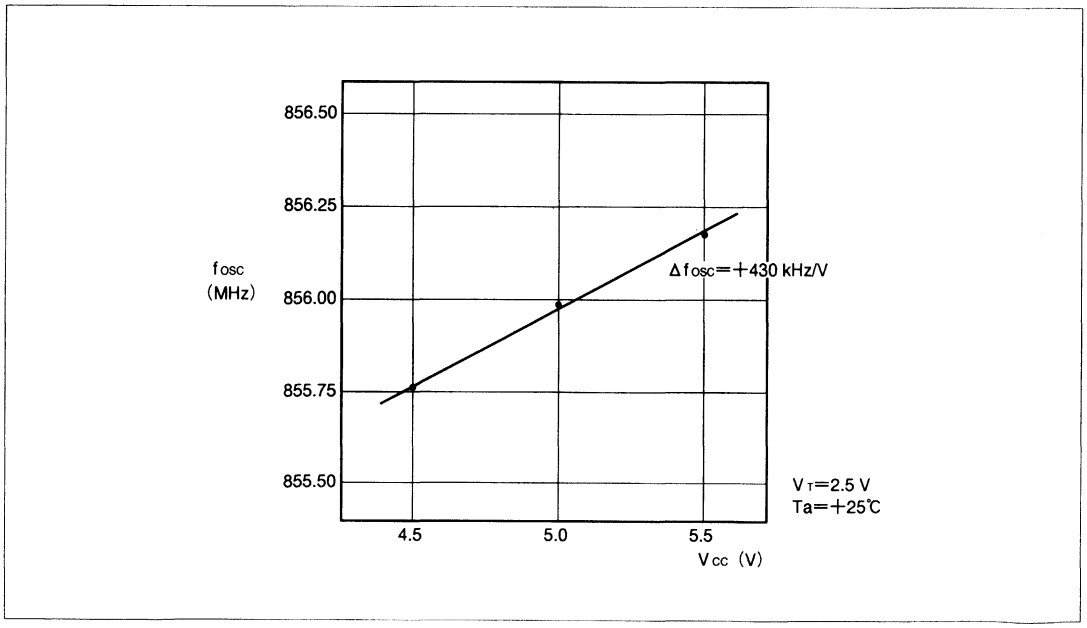


■ MEASUREMENT RESULTS (TEST CIRCUIT 1 ON RECOMMENDED PC BOARD)

(1) Conversion Gain

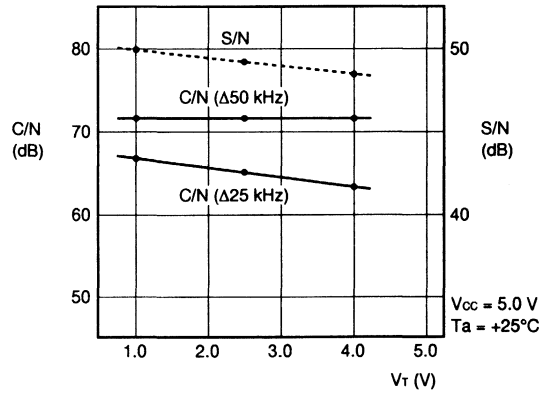


(2) Supply Voltage Variation

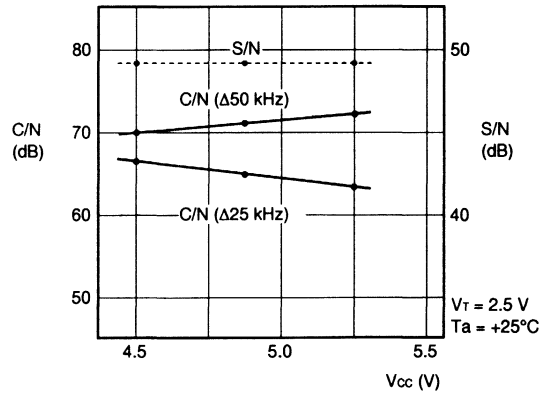


(3) C/N, S/N

- **Control Voltage Dependence**



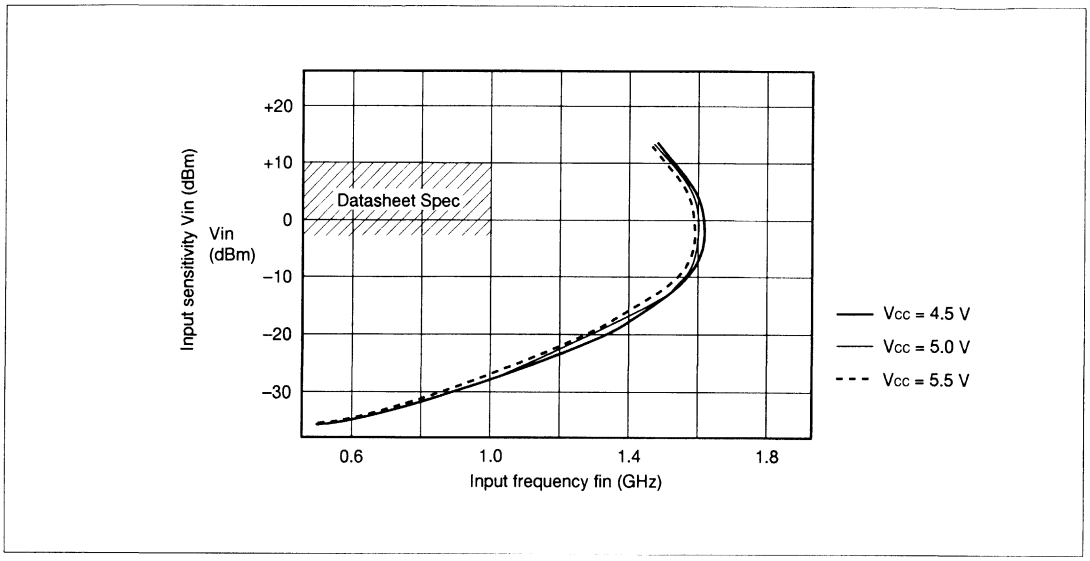
- **Supply Voltage Dependence**



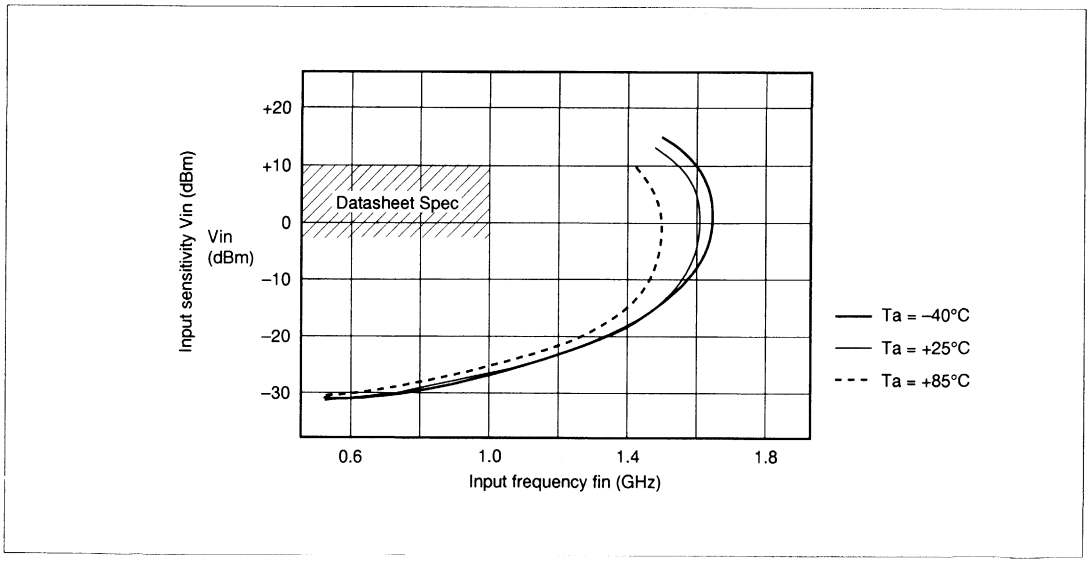
■ MEASUREMENT RESULTS

(1) Prescaler Input Sensitivity Curve

- **Supply voltage dependence (Ta = +25°C)**

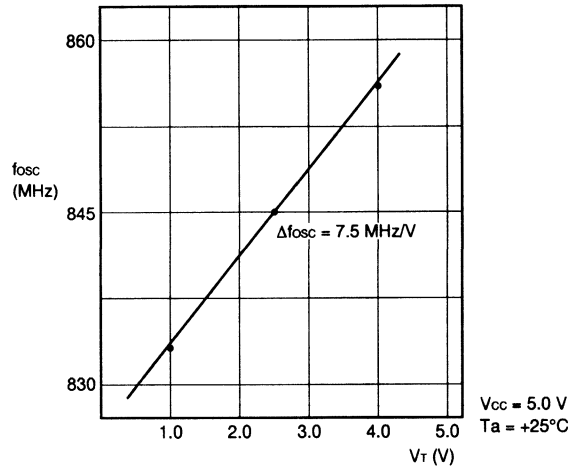


- **Temperature dependence (V_{CC} = 5 V)**



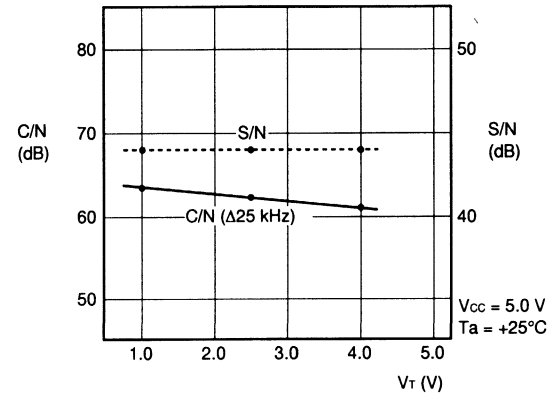
■ MEASUREMENT RESULTS (TEST CIRCUIT 2)

(1) Conversion Gain

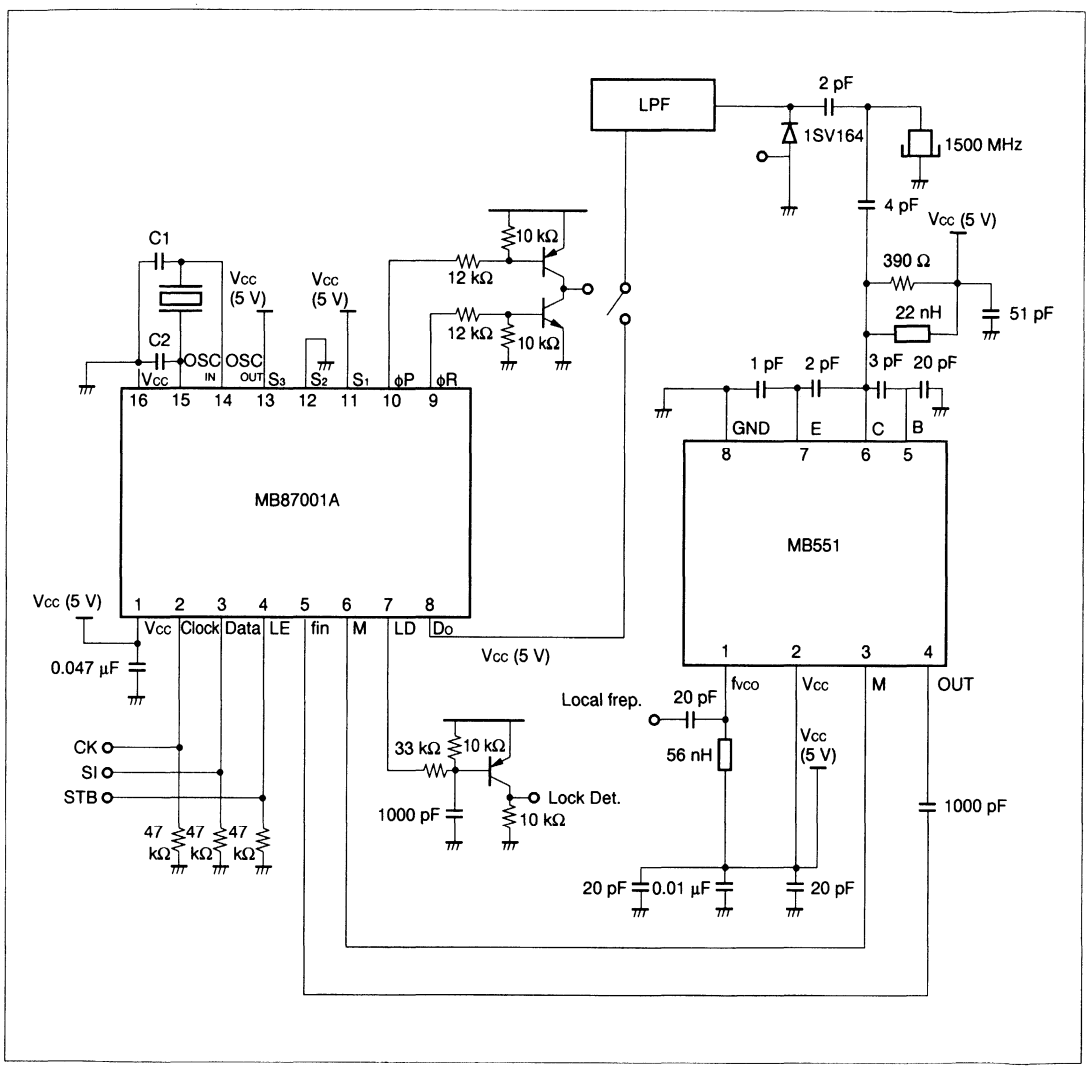


(2) C/N, S/N

- **Control voltage dependence**



■ SAMPLE APPLICATION CIRCUIT



■ ORDERING INFORMATION

Part number	Package	Remarks
MB551PF	8 pin Plastic SOP (FPT-8P-M01)	

MEMO

FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-21321-2E

ASSP for DTS

Bi-CMOS

1.1 GHz PLL Frequency Synthesizer

MB15A02

■ DESCRIPTION

The Fujitsu MB15A02, utilizing Bi-CMOS technology, is a single chip serial input PLL synthesizer with pulse-swallow function.

The MB15A02 contains a 1.1 GHz two modulus prescaler that can select either a 64/65 or 128/129 divide ratio, control signal generator, 16-bit shift register, 15-bit latch, programmable reference divider (binary 14-bit programmable reference counter), 1-bit switch counter, phase comparator with phase reverse function, charge pump, crystal oscillator, 19-bit shift register, 18-bit latch, and programmable divider (binary 7-bit swallow counter and binary 11-bit programmable counter).

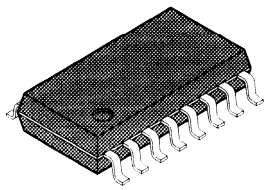
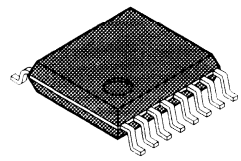
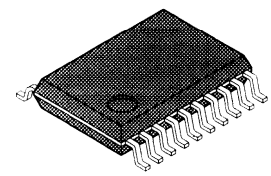
it operates supply voltage of 5 V typ. and achieves very low supply current of 7 mA typ. realized through the use of Fujitsu Advanced Process Technology.

■ FEATURES

- High operating frequency: $f_{IN\ MAX}$ = 1.1 GHz ($V_{IN\ un}$ = −10 dBm)
- Pulse swallow function: 64/65 or 128/129
- Low supply current: I_{CC} = 7 mA typ.
- Serial input 18-bit programmable divider consisting of:
  - Binary 7-bit swallow counter: 0 to 127
  - Binary 11-bit programmable counter: 16 to 2,047

(Continued)

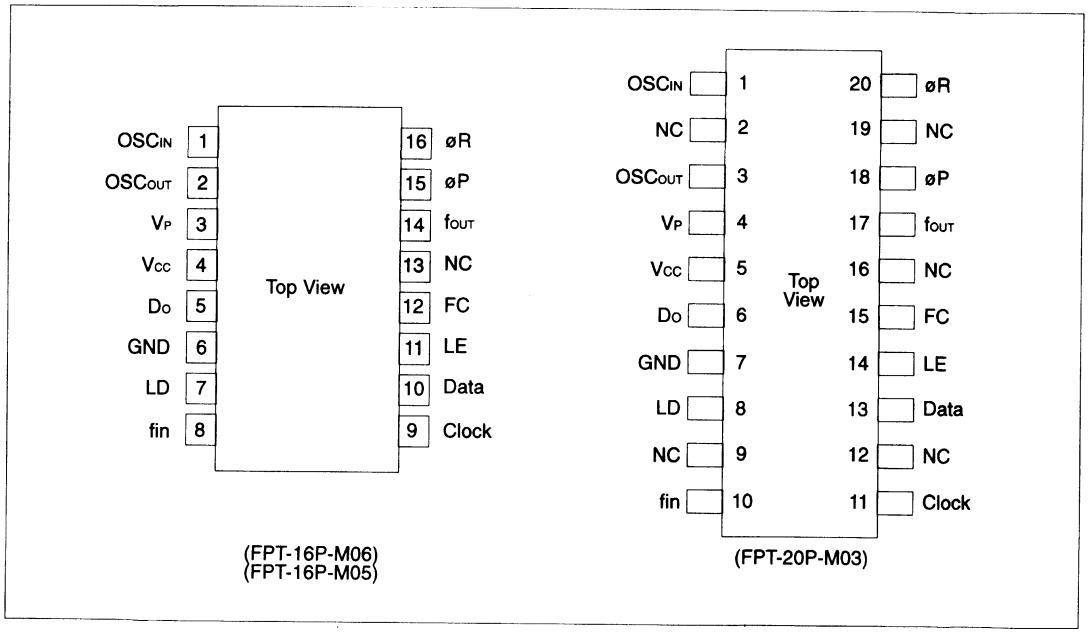
■ PACKAGES

16-pin Plastic SOP	16-pin Plastic SSOP	20-pin Plastic SSOP
		
(FPT-16P-M06)	(FPT-16P-M05)	(FPT-20P-M03)

(Continued)

- Serial input 15-bit programmable reference divider consisting of:
  - Binary 14-bit programmable reference couter: 6 to 16,383
  - 1-bit switch counter (SW) sets divide ratio of prescaler
- Two types of phase detector output
  - On-chip charge pump (Bipolar type)
  - Output for external charge pump
- Wide operating temperature: –40°C to +85°C
- 16-pin Plastic SOP Package
  16-pin and 20-pin Plastic SSOP Packages

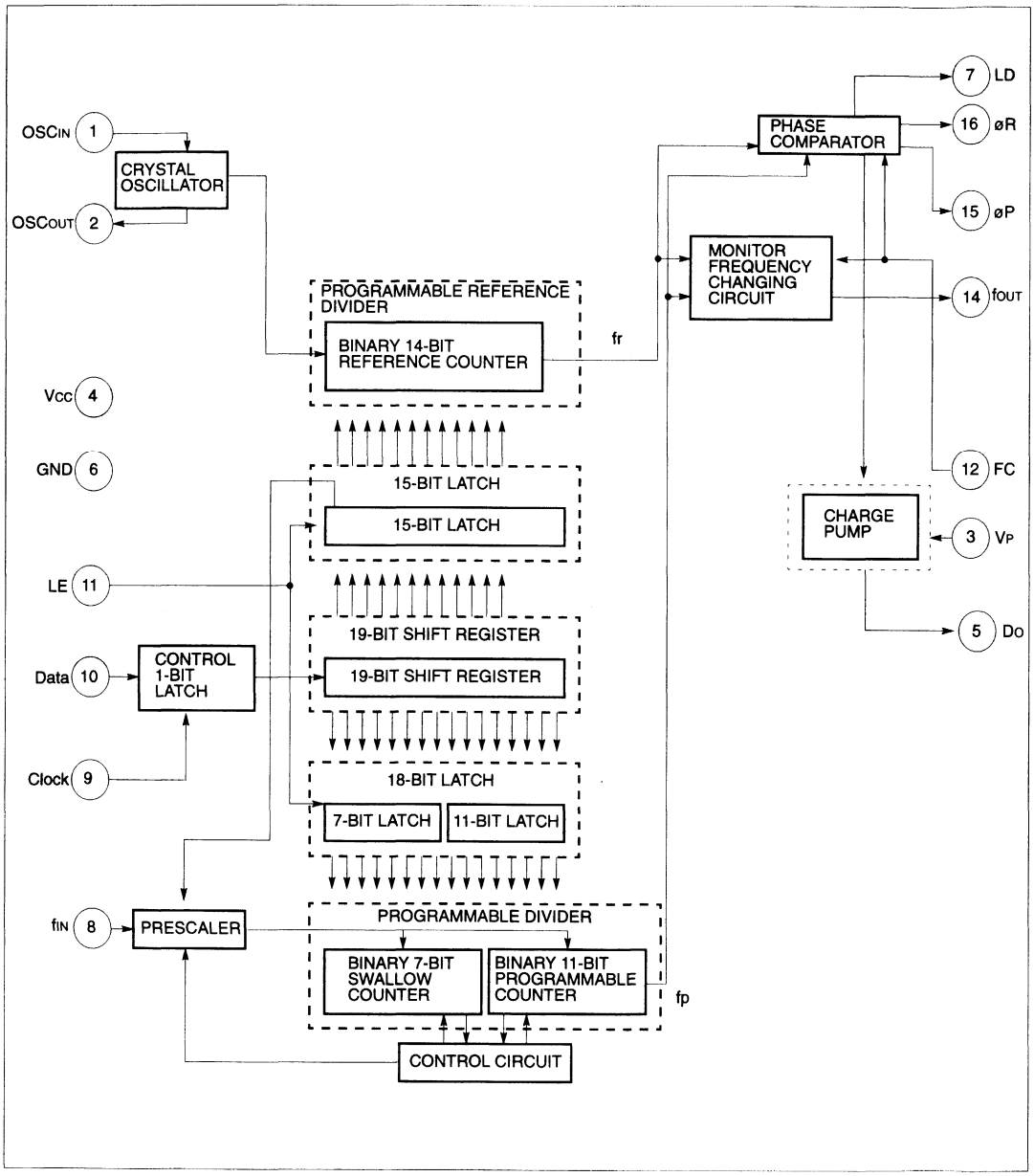
■ PIN ASSIGNMENTS



■ PIN DESCRIPTION

Pin No.		Pin name	I/O	Function
SOP-16P SSOP-16P	SSOP-20			
1 2	1 3	OSC_{IN} OSC_{OUT}	I O	Oscillator input. Oscillator output. A crystal is placed between OSC_{IN} and OSC_{OUT}.
3	4	V_P	—	Power supply pin for charge pump. When the internal charge pump is not used, V_P pin needs to be connected to V_{CC}.
4	5	V_{CC}	—	Power supply pin
5	6	D_O	O	Charge pump output.
6	7	GND	—	Ground.
7	8	LD	O	Phase comparator output. Normally this pin outputs high level. When there is a phase error between fr and fp, LD becomes low for the period corresponding to the error.
8	10	f_{IN}	I	Prescaler input. The connection with an external VCO should be AC connection.
9	11	Clock	I	Clock input for 19-bit shift register an 16-bit shift register. On rising edge of the clock shifts one bit of data into shift register.
10	13	Data	I	Binary serial data input. The last bit of data is a control bit. When this bit is high level, the data stored in shift register is transferred to 15-bit latch. When this bit is low level and LE is high level, the data is transferred to 18-bit latch.
11	14	LE	I	Load enable input (with internal pull up resistor). When LE is high, the data stored in shift register is transferred into latch according to the control bit.
12	15	FC	I	Phase select input of phase comparator (with internal pull up resistor). When FC is low level, the characteristics of phase comparator is reversed. FC input signal is also used to select fout pin (test pin) output, fr or fp.
13	2, 9, 12, 16, 19	N.C.	—	No connection
14	17	f_{OUT}	O	Minitor pin of phase comparator input. fout pin outputs either programmable reference divider output (fr)or programmable divider output (fp) according to FC pin input level. FC = H: It is the same as fr output level. FC = L: It is the same as fp output level.
15	18	øP	O	Outputs for external charge pump. The characteristics are reversed according to FC input. øP pin is N-channel open drain output.
16	20	øR	O	Outputs for external charge pump. øR pin is CMOS output.

■ BLOCK DIAGRAM



Note: Pin numbers are based on SOP/SSOP 16-pin packages.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Remarks
Supply voltage	V_{CC}	−0.5 to +7.0	V	
	V_P	V_{CC} to 8.0	V	
Output voltage	V_{OUT}	−0.5 to V_{CC} +0.5	V	øP pin
Open-drain voltage	V_{OOP}	−0.5 to 6.0	V	
Output current	I_{OUT}	±10	mA	
Storage temperature	T_{STG}	−55 to +125	°C	

Note: Permanent device damage may occur if the above absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_P	V_{CC}	—	6.0	V
Input voltage	V_I	GND	—	V_{CC}	V
Operating temperature	Ta	−40	—	85	°C

■ ELECTRICAL CHARACTERISTICS

Parameter		Symbol	Condition	Value			Unit
				Min.	Typ.	Max.	
Power supply current		I_{CC}	*1	—	7.0	—	mA
Operating frequency	fin	fin	*2	10	—	1100	MHz
	OSC_{IN}	f_{OSC}		—	12	20	MHz
Input sensitivity	fin	V_{fin}	50 Ω system	−10	—	6	dBm
	OSC_{IN}	V_{OSC}		0.5	—	—	V_{P-P}
"H" level input voltage	Clock Data LE	V_{IH}		$V_{CC} \times 0.7$	—	—	V
"L" level input voltage		V_{IL}		—	—	$V_{CC} \times 0.3$	V
"H" level input current	Clock Data	I_{IH}		—	—	1.0	µA
"L" level input current		I_{IL}		—	—	−1.0	µA
Input current	OSC_{IN}	I_{OSC}		—	±50	—	µA
	LE, FC	I_{LE}		—	−60	—	µA
"H" level output voltage	øR, LD	V_{OH}	V_{CC} = 5 V, I_{OH} = −1.0 mA	4.4	—	—	V
"L" level output voltage	øP/R, LD	V_{OL}	V_{CC} = 5 V, I_{OL} = 1.0 mA	—	—	0.4	V
High impedance cutoff current	D_O, øP	I_{OFF}	V_P = V_{CC} to 6 V, V_{OOP} = GND to 6 V	—	—	1.1	µA
Output current	øR, LD	I_{OH}	V_{CC} = 5 V	−1.0	—	—	mA
	øP/R, LD	I_{OL}	V_{CC} = 5 V	—	—	1.0	mA

*1: fin = 1.1 GHz, OSC_{IN} = 12 MHz, V_{CC} = 5 V. In locked state.

*2: AC coupling. Minimum operating frequency is measured when a capacitor 1000 pF is connected.

■ FUNCTIONAL DESCRIPTIONS

1. Pulse Swallow Function

For the pulse swallow function, use the following equations to select their respective setting values:

$$f_{VCO} = ((P \times N) + A) \times f_{OSC} + R$$

f_{VCO}	:	Output frequency of external voltage controlled oscillator (VCO)
N	:	Preset divide ratio of binary 11-bit programmable counter (16 to 2,047)
A	:	Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$, $A < N$)
f_{OSC}	:	Output frequency of the external reference frequency oscillator
R	:	Preset divide ratio of binary 14-bit programmable reference couter (6 to 16,383)
P	:	Preset modulus of external dual modulus prescaler (64 or 128)

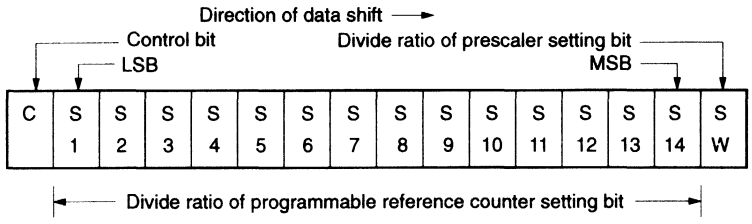
2. Serial Data Input Method

Serial data is processed using three input pins (Data, Clock, and LE pins) to control the 15-bit reference divider and the 18-bit programmable divider separately.
Input binary-coded serial data to the Data pin.
Serial data is input to the internal shift register in sequence at the rise of each clock pulse. When the load enable signal input pin has a high level (or open), the input data is transferred to the latch depending on the control bit.

Control bit = "H": Transfer to the 15-bit latch
Control bit = "L": Transfer to the 18-bit latch

(1) Divide Ratio of Reference Divider

The reference divider consisits of a 16-bit shift register, a 15-bit latch, and a 14-bit reference counter. Serial datais made up of the following 16 bits:



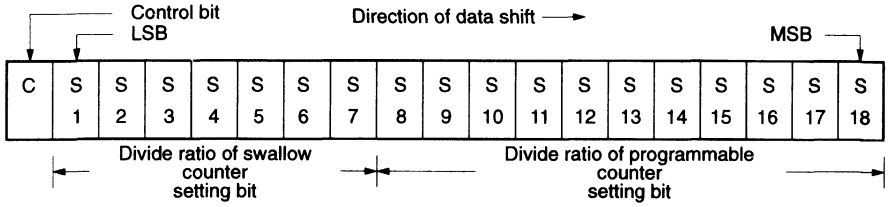
• 14-bit programmable reference counter divide ratio

Divide Ratio R	S 14	S 13	S 12	S 11	S 10	S 9	S 8	S 7	S 6	S 5	S 4	S 3	S 2	S 1
6	0	0	0	0	0	0	0	0	0	0	0	1	1	0
7	0	0	0	0	0	0	0	0	0	0	0	1	1	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Notes: Divide ratio less than 6 is prohibited.
Divide ratio: 6 to 16,383
SW: This bit selects divide ratio of prescaler.
SW = H: 64/65
SW = L: 128/129
S1 to S14: These bits select divide ratio of programmable reference divider.
C: Control bit (sets at high level).
Start data input with MSB first.

(2) Divide Ratio of Programmable Divider

The programmable divider consists of a 19-bit shift register, an 18-bit latch, 7-bit swallow counter, and an 11-bit programmable counter. Serial data is made up of the following 19 bits:



• 7-bit swallow counter divide ratio

Divide Ratio N	S7	S6	S5	S4	S3	S2	S1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

Notes: Divide ratio: 0 to 127

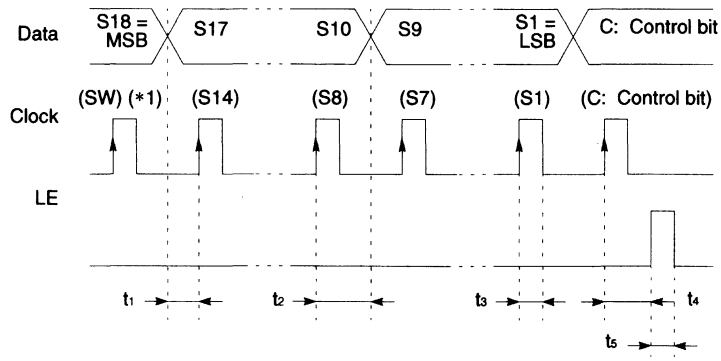
• 11-bit programmable counter divide ratio

Divide Ratio N	S18	S17	S16	S15	S14	S13	S12	S11	S10	S9	S8
16	0	0	0	0	0	0	1	0	0	0	0
17	0	0	0	0	0	0	1	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

Notes: Divide ratio less than 16 is prohibited.
Divide ratio: 16 to 2,047
S1 to S7: Swallow counter divide ratio setting bit. (0 to 127)
S8 to S18: Programmable counter divide ratio setting bit.
C: Control bit (sets at low level)
Data input with MSB first.

(3) Serial Data Input Timing

• t_1 (≥ 100 ns): Data setup time t_2 (≥ 1000ns): Data hold time t_3 (≥ 300 ns): Clock pulse width
t_4 (≥ 100 ns): LE setup time to the rising edge of last clock t_5 (≥ 800 ns): LE pulse width



*1: Bits enclosed in parentheses are used when the divide ratio of the programmable reference divider is selected.

Note: One bit of data is shifted into the shift register on the rising edge of the clock.

3. Relation between FC Pin Inputs and Phase Characteristics

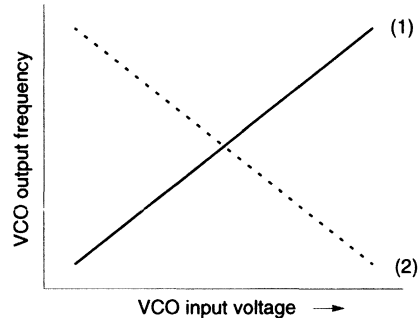
The FC pin is the phase switching pin for the phase comparator. Controlling the FC pin inverts the characteristics of the internal charge pump output (D_O) and phase comparator outputs (øR, øP). In addition, the phase comparator input monitor pin (fout) is also controlled via the FC pin. The following table lists relation between FC pin inputs and D_O, øR, øP, and fout:

	FC: "H" (or open)				FC: "L"			
	D_O	øR	øP	fout	D_O	øR	øP	fout
fr > fp	H	L	L	fr	L	H	Z	fp
fr < fp	L	H	Z		H	L	L	
fr = fp	Z	L	Z		Z	L	Z	

Z: High impedance

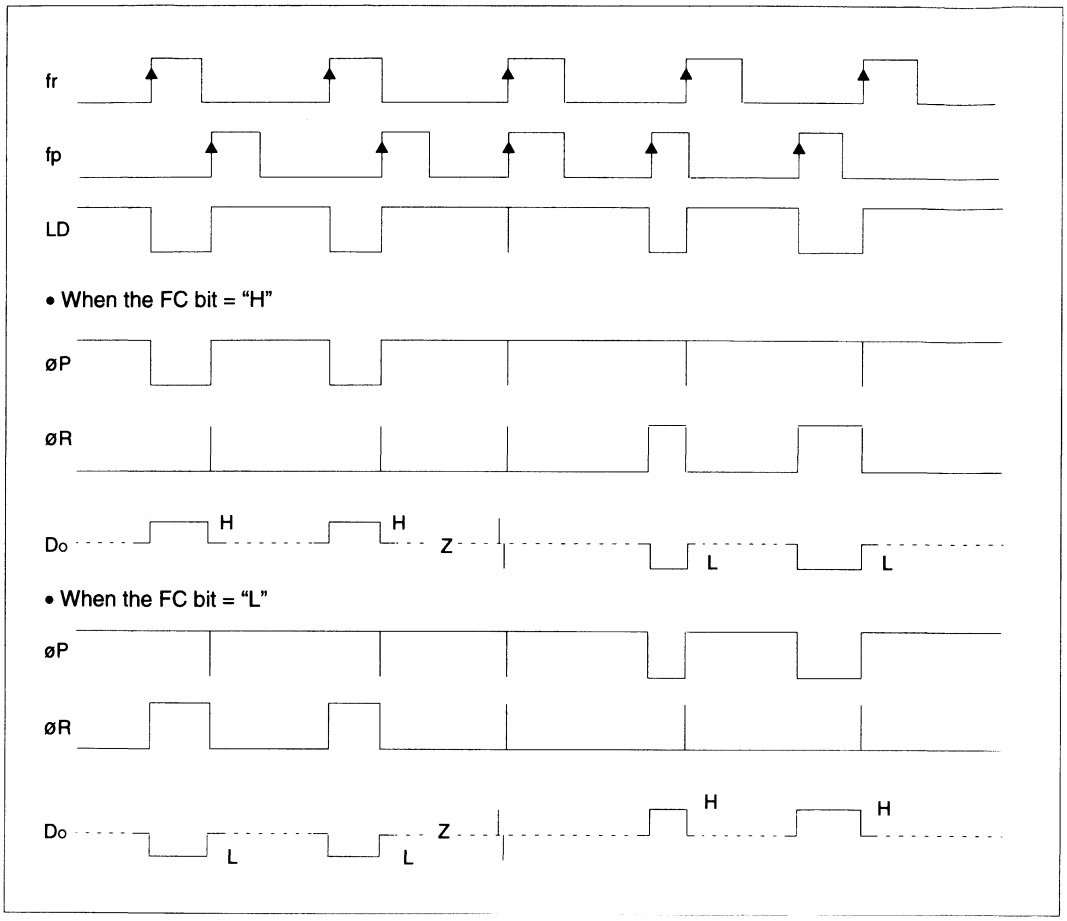
When disignaing a synthesizer, control the FC pin depending on the VCO polarity.

- When the VCO polarity is (1)
  FC: "H" or open
- When the VCO polarity is (2)
  FC: "L"



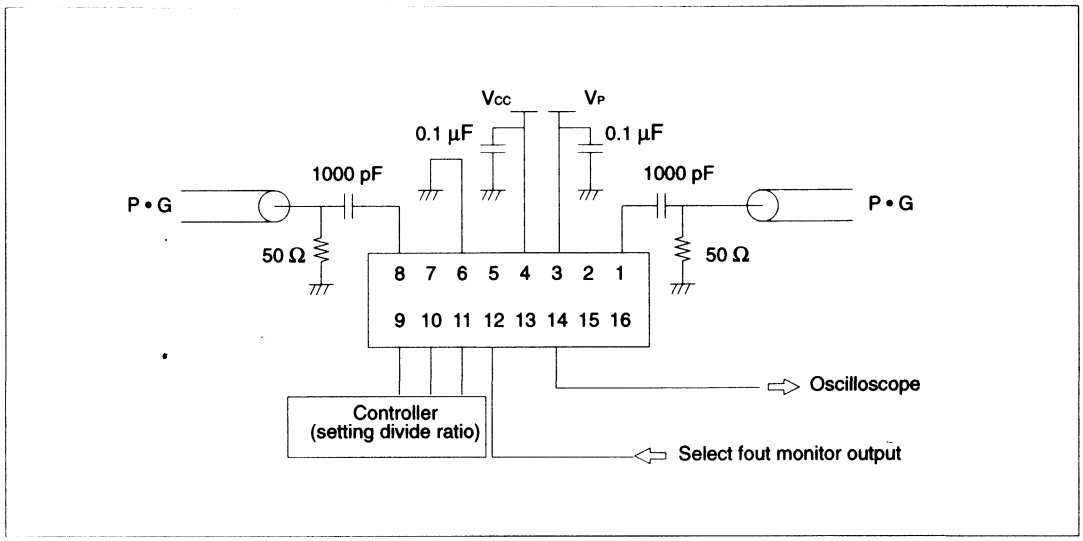
Note: When using an active lowpass filter, pay attention to its polarity.

■ PHASE COMPARATOR OUTPUT WAVEFORMS



Note: Phase error detection range: -2π to $+2\pi$

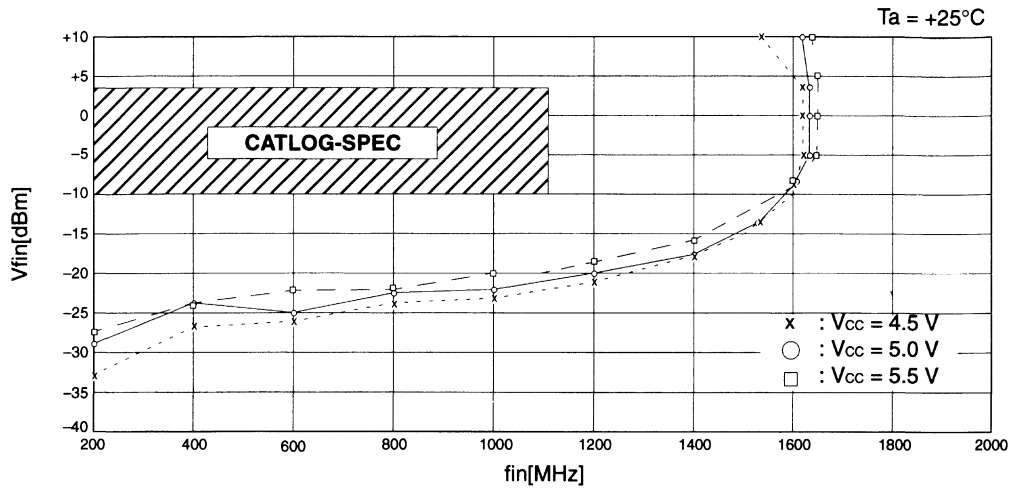
■ TEST CIRCUIT EXAMPLE (fin/OSCIN Input Sensitivity Measurement)



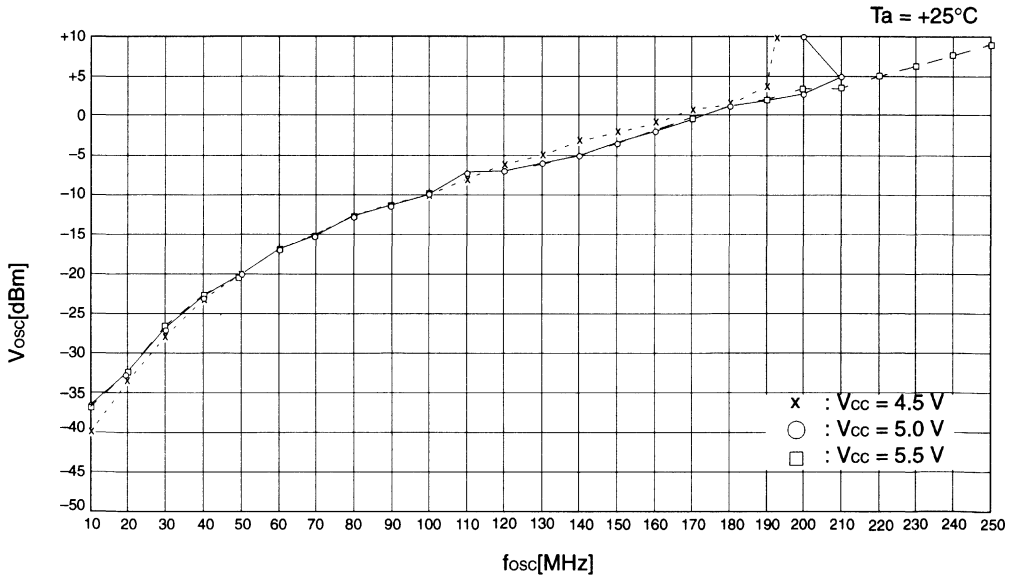
Note: Pin numbers are based on SOP/SSOP 16-pin packages.

■ TYPICAL CHARACTERISTICS

Input Sensitivity (fin Pin)



Input Sensitivity (OSCin Pin)



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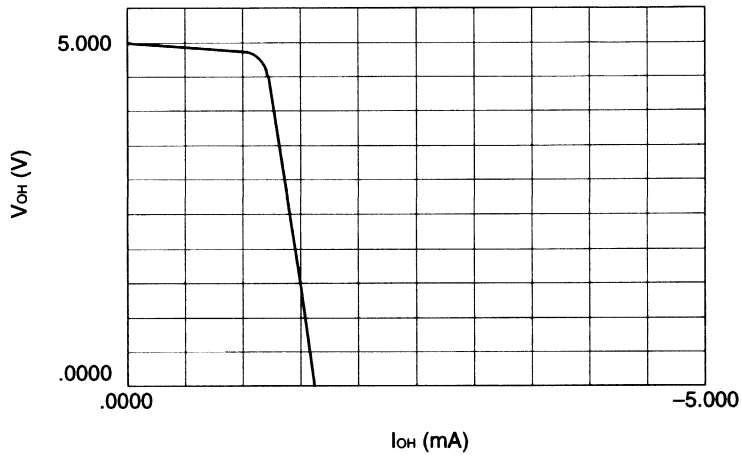
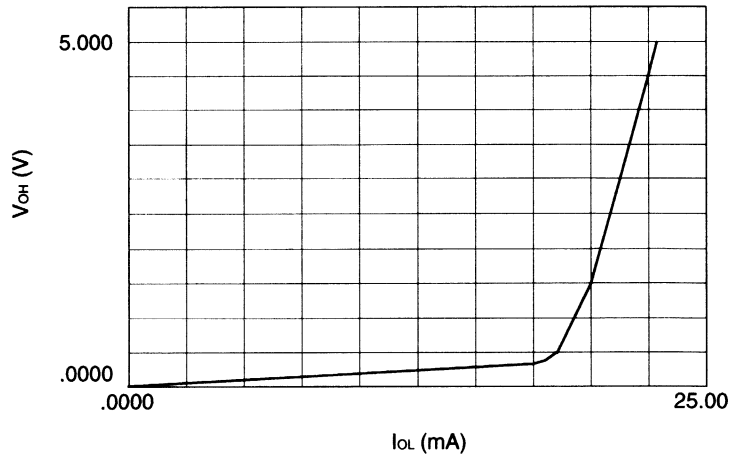
Charge Pump Current vs. Voltage (D_O Pin)

V_{OH} vs. I_{OH}



V_{OL} vs. I_{OL}



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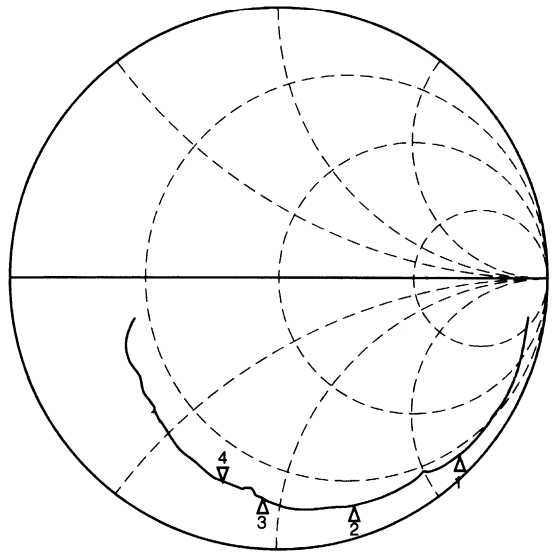
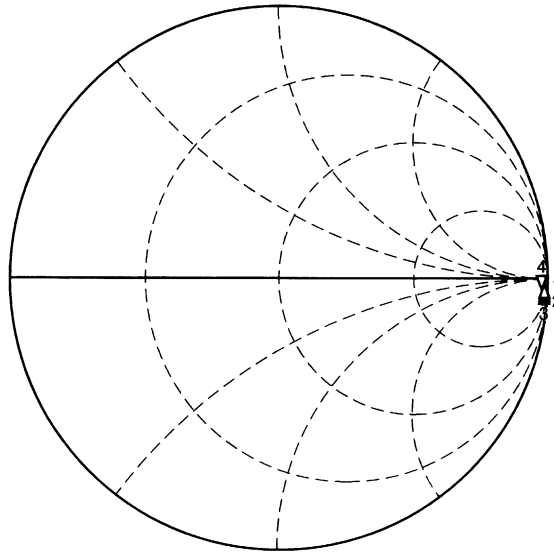
Input Impedance

fin Pin



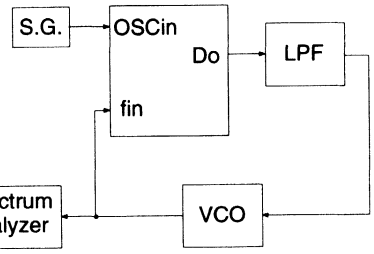
OSCin Pin



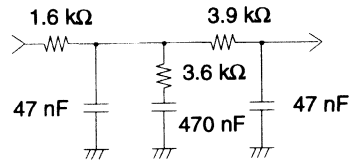
■ REFERENCE INFORMATION

Typical plots measured with the test circuit are shown below. Each plots shows lock up time, phase noise, and reference leakage.

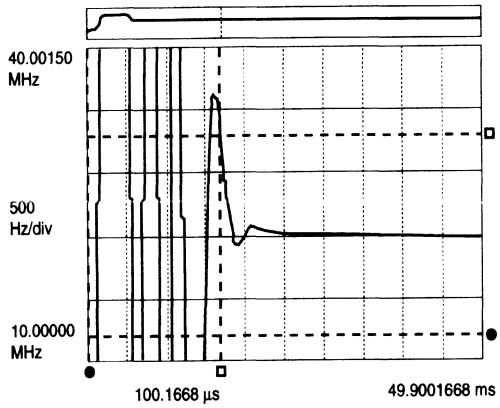
Test Circuit



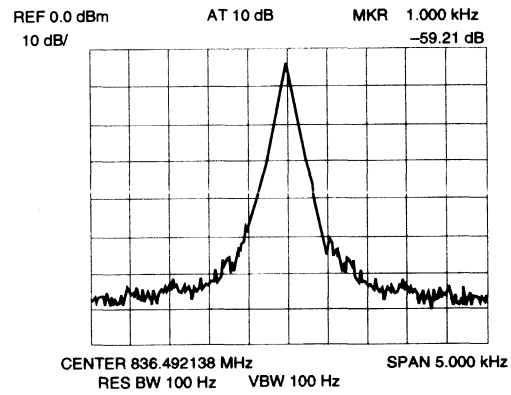
- f_{VCO} = 836.49 MHz
- K_V = 12 MHz/V
- f_r = 30 kHz
- f_{OSC} = 15.36 MHz
- LPF



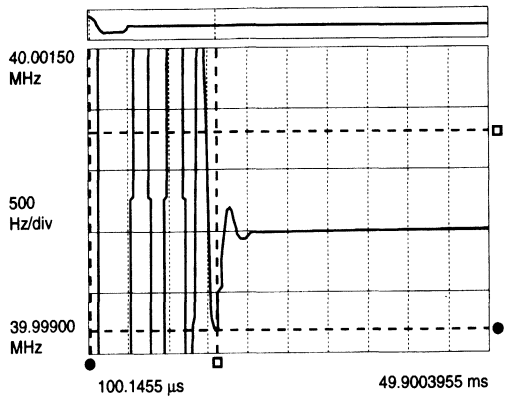
PLL Lock Up Time = 16.8 ms
(824,010 MHz → 848,97 MHz, within ± 800 Hz)



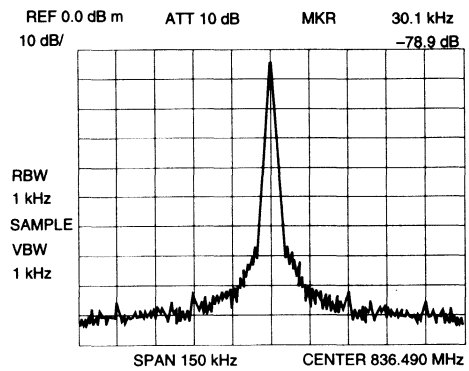
PLL Phase Noise
@Within loop band = 79.2 dBc/Hz



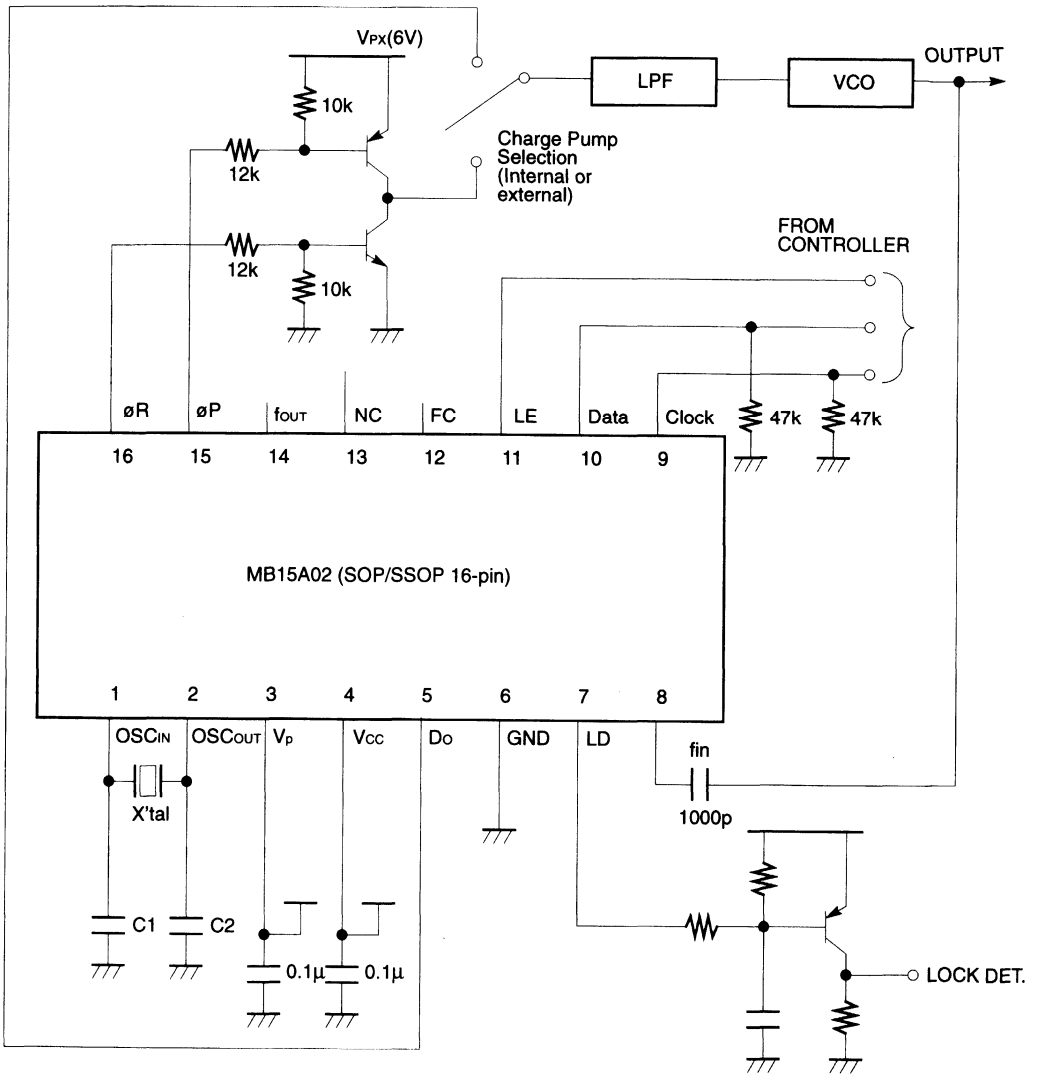
PLL Lock Up Time = 16.2 ms
(848,970 MHz → 824,010 MHz, within ± 800 Hz)



PLL Reference Leakage
@30 kHz offset = 78.9 dBc



■ APPLICATION EXAMPLE (16-pin Package)



VPX : 6 V max.
VP : When internal charge pump is not used, VP pin needs to be connected to VCC.
C1, C2 : Depends on crystal oscillator
LE,FC : With internal pull up resistor
øP : Open drain output
øR : CMOS output

■ ORDERING INFORMATION

Part number	Package	Remarks
MB15A02PF	16-pin, Plastic SOP (FPT-16P-M06)	
MB15A02PFV1	16-pin, Plastic SSOP (FPT-16P-M05)	
MB15A02PFV2	20-pin, Plastic SSOP (FPT-20P-M03)	

MEMO

FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-21324-3E

ASSP for DTS

Bi-CMOS

1.1 GHz PLL Frequency Synthesizer

MB15A01

■ DESCRIPTION

The MB15A01 is a serial-input PLL (phase locked loop) frequency synthesizer LSI supporting a pulse swallow system.

The LSI consists of: a 1.1 GHz band, dual-modulus prescaler allowing either of 64/65 and 128/129 frequency divisions to be selected, a control signal generator circuit, a 19-bit shift register, a 15-bit latch, a reference divider (binary 14-bit reference counter), a 1-bit switch counter, a phase comparator with phase conversion functions, a charge pump, a crystal oscillator, an 18-bit latch, and programmable dividers (binary 7-bit swallow counter and binary 11-bit programmable counter).

The LSI is housed in a 16-pin or 20-pin SSOP package, contributing to space saving of the system incorporating it.

In addition, the MB15A01 operates at a low supply voltage of 3.0 V (typical), achieving low current consumption (typically I_{CC} = 6.5 mA)

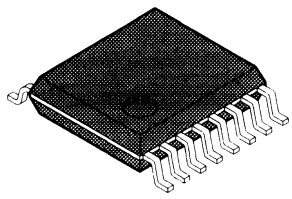
■ FEATURES

- Operation at high speed: fin = 1.1 GHz (Vin = −10 dBm)
- Pulse swallow function: Internal dual-modulus prescaler allowing either of 64/65 and 128/129 frequency divisions to be selected
- Low current consumption: I_{CC} = 6.5 mA (typical)

(Continued)

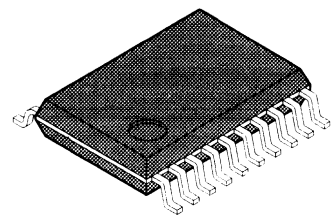
■ PACKAGES

16-pin Plastic SSOP



(FPT-16P-M05)

20-pin Plastic SSOP

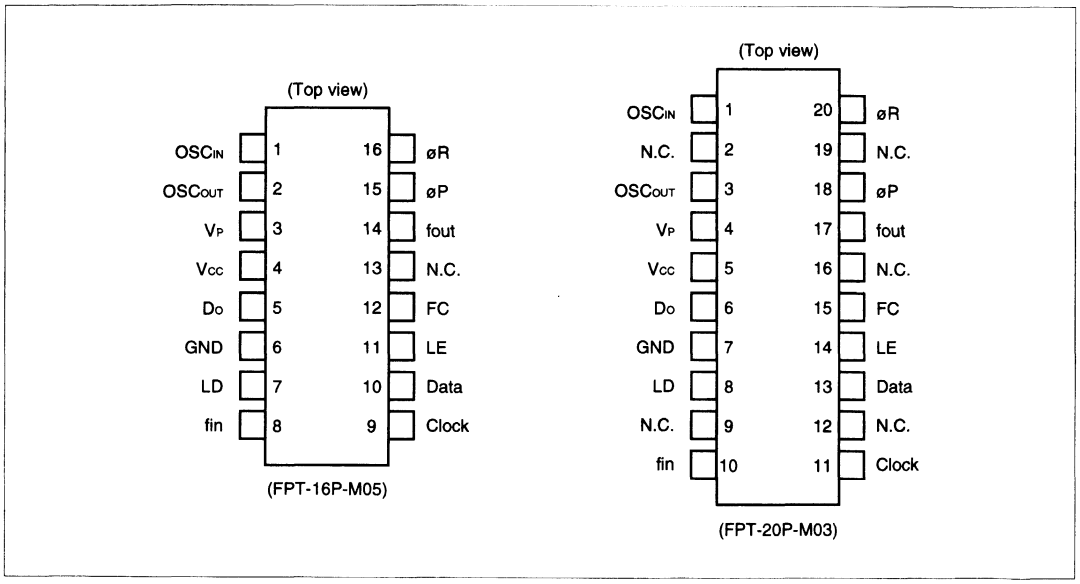


(FPT-20P-M03)

(Continued)

- Serial-input 18-bit programmable divider
  Divide ratio of binary 7-bit swallow counter (0 to 127)
  Binary 11-bit programmable counter (16 to 2,047)
- Serial-input 15-bit reference divider
  Divide ratio of binary 14-bit programmable reference counter (6 to 16,383)
  1-bit switch counter (for setting the prescaler divide ratio)
- Serial data configuration compatible with conventional models such as MB1511
- Two different phase comparator outputs
  Internal charge pump output (bipolar type)
  Output for external charge pump
- Wide range of operating temperature: Ta = –40 to +85°C

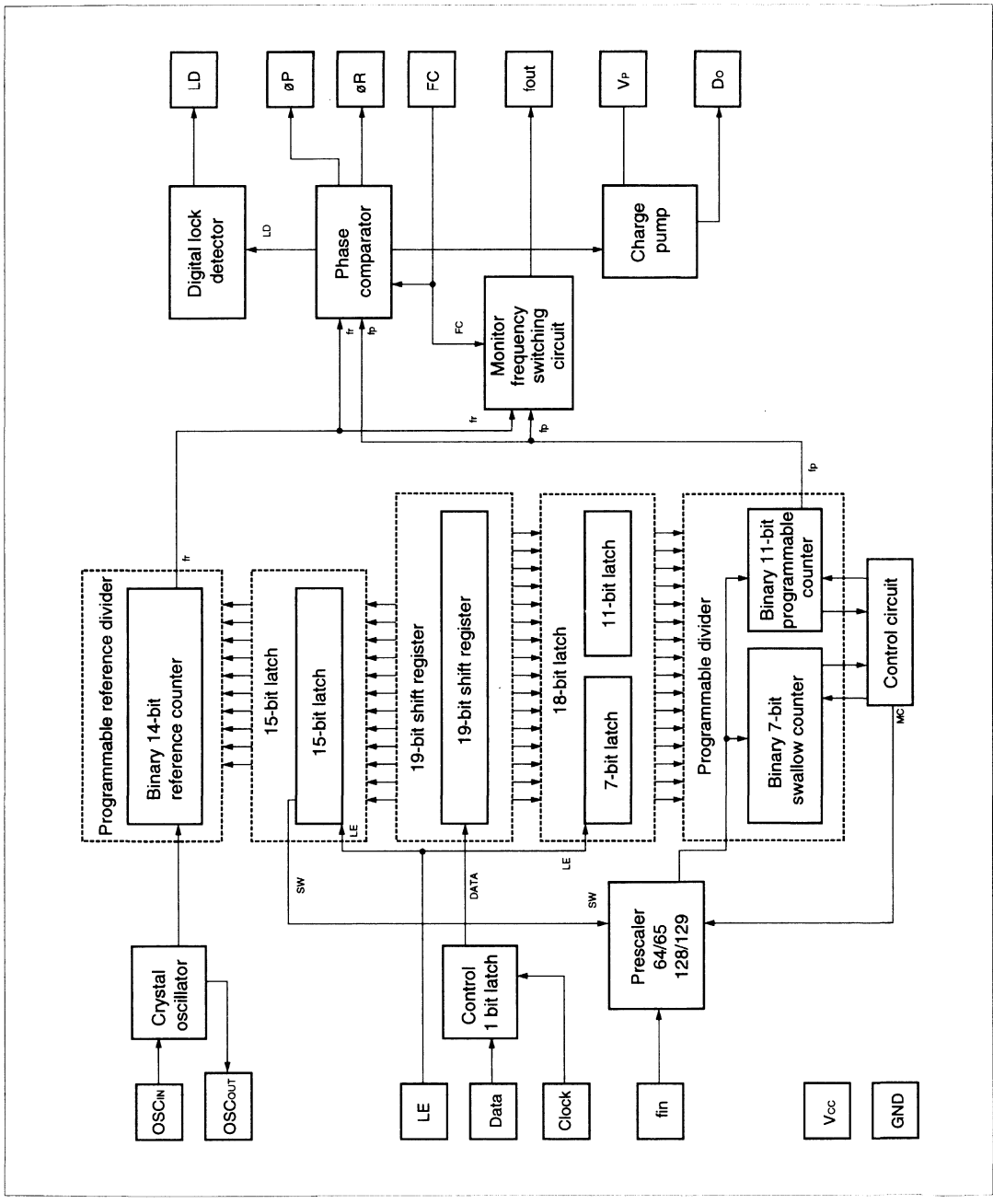
■ PIN ASSIGNMENTS



■ PIN DESCRIPTION

Pin No.		Pin name	I/O	Function
SSOP-16	SSOP-20			
1	1	OSC_{IN}	I	Crystal oscillator connection pin serving as a reference divider input pin (Oscillator circuit input pin)
2	3	OSC_{OUT}	O	Crystal oscillator connection pin (Oscillator circuit output pin)
3	4	V_P	—	Power supply pin for charge pump output Connect this pin to V_{CC} when the internal charge pump is not used.
4	5	V_{CC}	—	Power supply pin
5	6	D_O	O	Internal charge pump output pin
6	7	GND	—	GND pin
7	8	LD	O	Lock detector output pin When locked: LD = "H", When unlocked: LD = "L"
8	10	fin	I	Prescaler input pin The pin must be AC-coupled for input.
9	11	Clock	I	Clock input pin for 19-bit and 16-bit shift registers The shift resistors reads data at the rise of the clock pulse.
10	13	Data	I	Binary-coded serial data input pin The last bit in the data is a control bit. Control bit = "H": Sends data to the 15-bit latch. "L": Sends data to the 18-bit latch.
11	14	LE	I	Load enable signal input pin (with pull-up resistor) When LE = "H", the pin sends the contents of the shift register to the latch according to the control bit.
12	15	FC	I	Phase comparator phase switching pin (with pull-up resistor) When FC = "L", the pin inverts characteristics of the phase comparator. It also switches the fout pin (test pin) output between fr and fp.
13	2, 9, 12, 16, 19	N.C.	—	No connection.
14	17	fout	O	Phase comparator input monitor pin The pin outputs the reference divider output (fr) or programmable divider output (fp) signal depending on the FC pin input level. It is an N channel open-drain output.
15	18	øP	O	Phase comparator output pin for external charge pump This pin is an N channel open-drain output.
16	20	øR	O	Phase comparator output pin for external charge pump This pin is a CMOS output.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	−0.5	+5.0	V	
	V_P	V_{CC}	+8.0	V	
Output voltage	V_O	−0.5	V_{CC} + 0.5	V	
Open-drain voltage	V_{OOP}	−0.5	+6.0	V	øP pin
Output current	I_O	−10	+10	mA	
Storage temperature	Tstg	−55	+125	°C	

Precaution: Permanent device damage may occur if the above absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Power supply voltage	V_{CC}	2.7	3.0	3.5	V
	V_P	V_{CC}	—	6.0	V
Input voltage	V_I	GND	—	V_{CC}	V
Operating temperature	Ta	−40	—	+85	°C

Precautions: Although the MB15A01 contains an antistatic element to prevent electrostatic breakdown and the circuitry has been improved in electrostatic protection, observe the following precautions when handling the device:

- When storing or carrying the device, put it in a conductive case.
- This is static-sensitive device; take proper anti-ESD precautins. Ensure that personnel and equipment are properly grounded. Cover workbenches with grounded conductive mats.
- Before fitting the device into or removing it from the socket, turn the power supply off.
- Protect leads with conductive sheet when handling or transporting PC boads with devices.

■ ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.7 V to 3.5 V, Ta = −40°C to +85°C)

Parameter		Symbol	Condition	Value			Unit
				Min.	Typ.	Max.	
Power supply current		I_{CC}	V_{CC} = 3 V, assuming fin = 1.1 GHz and OSC_{IN} = 12 MHz, in locking	—	6.5	—	mA
Operating frequency	fin	fin	Must be AC-coupled. The minimum operating frequency assumes coupling at 1000 pF.	10	—	1100	MHz
	OSC_{IN}	f_{OSC}	—	—	12	23	MHz
Input sensitivity	fin	V_{fin}	50 Ω system (Refer to the test circuit example)	−10	—	6	dBm
	OSC_{IN}	V_{OSC}	—	0.5	—	—	V_{P-P}
"H" level input voltage	Clock Data LE	V_{IH}	—	V_{CC} × 0.7	—	—	V
"L" level input voltage		V_{IL}	—	—	—	V_{CC} × 0.3	V
"H" level input current	Clock Data	I_{IH}	—	—	—	1.0	µA
"L" level input current		I_{IL}	—	—	—	−1.0	µA
Input current	OSC_{IN}	I_{OSC}	—	—	±50	—	µA
	LE, FC	I_{LE}	—	—	−60	—	µA
"H" level output voltage	øR, LD	V_{OH}	V_{CC} = 3 V, I_{OH} = −1.0 mA	2.1	—	—	V
"L" level output voltage	øP/R, LD	V_{OL}	V_{CC} = 3 V, I_{OL} = 1.0 mA	—	—	0.4	V
High-impedance cutoff current	D_O øP	I_{OFF}	V_P = V_{CC} to 6.0 V V_{OOP} = GND to 6.0 V	—	—	1.1	µA
Output current	øR, LD	I_{OH}	V_{CC} = 3 V	−1.0	—	—	mA
	øP/R, LD	I_{OL}	V_{CC} = 3 V	—	—	1.0	mA

■ FUNCTIONAL DESCRIPTIONS

1. Pulse Swallow Function

For the pulse swallow function, use the following equations to select their respective setting values:

$$f_{VCO} = ((P \times N) + A) \times f_{OSC} + R$$

f_{VCO}	:	Output frequency of externally connected VCO
P	:	Prescaler divide ratio (64 or 128)
N	:	Divide ratio of 11-bit programmable counter (16 to 2047)
A	:	Divide ratio of 7-bit swallow counter (0 to 127, A < N)
f_{OSC}	:	Reference oscillation frequency
R	:	Divide ratio of 14-bit programmable reference counter (6 to 16383)

2. Serial Data Input Method

Serial data is processed using three input pins (Data, Clock, and LE pins) to control the 15-bit reference divider and the 18-bit programmable divider separately.

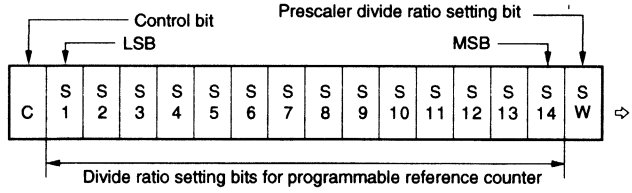
Input binary-coded serial data to the Data pin.

Serial data is input to the internal shift register in sequence at the rise of each clock pulse. When the load enable signal input pin has a high level (or open), the input data is transferred to the latch depending on the control bit.

Control bit = "H": Transfer to the 15-bit latch
Control bit = "L": Transfer to the 18-bit latch

(1) Divide Ratio of Reference Divider

The reference divider consisits of a 16-bit shift register, a 15-bit latch, and a 14-bit reference counter. Serial data is made up of the following 16 bits:



• 14-bit programmable reference counter divide ratio

Divide ratio R	S 14	S 13	S 12	S 11	S 10	S 9	S 8	S 7	S 6	S 5	S 4	S 3	S 2	S 1
6	0	0	0	0	0	0	0	0	0	0	0	1	1	0
7	0	0	0	0	0	0	0	0	0	0	0	1	1	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•

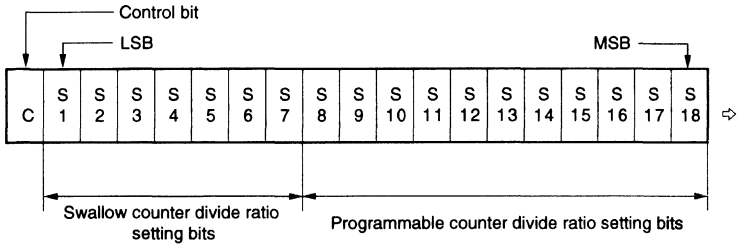
Note: The divide ratio must not be less than 6. (Set value: 6 to 16383)

SW: Prescaler division bit
SW = "H": 64/65 division
SW = "L": 128/129 division
S1 to S14: Divide ratio setting bits (Divide ratio of 6 to 16383)
C: Control bit (Set it to "H".)

Note: Start data input with MSB first.

(2) Divide Ratio of Programmable Divider

The programmable divider consists of a 19-bit shift register, an 18-bit latch, 7-bit swallow counter, and an 11-bit programmable counter. Serial data is made up of the following 19 bits:



• 7-bit swallow counter divide ratio

Divide ratio A	S 7	S 6	S 5	S 4	S 3	S 2	S 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.

(Set value: 0 to 127)

• 11-bit programmable counter divide ratio

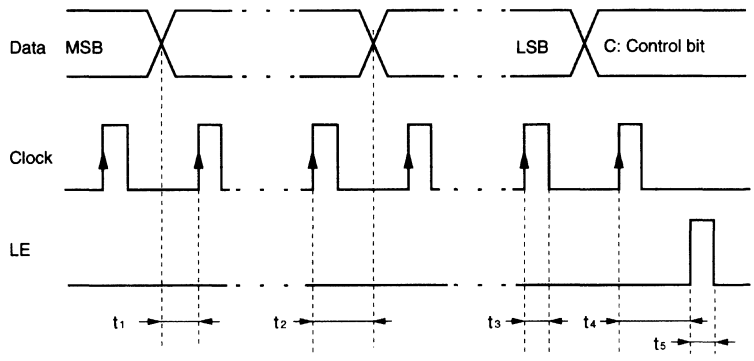
Divide ratio N	S 18	S 17	S 16	S 15	S 14	S 13	S 12	S 11	S 10	S 9	S 8
16	0	0	0	0	0	0	1	0	0	0	0
17	0	0	0	0	0	0	1	0	0	0	1
.	.	.	.	.	.	.	.	.	.	.	.

Note: The divide ratio must not be less than 16. (Set value: 16 to 2047)

S1 to S7: Swallow counter divide ratio setting bits (Divide ratio of 0 to 127)
S8 to S18: Programmable counter divide ratio setting bits (Divide ratio of 16 to 2047)
C: Control bit (Set it to "L".)

Note: Start data input with MSB first.

(3) Serial Data Input Timing



t_1, t_4>100 ns, t_2>1000 ns, t_3>300 ns, t_5>800 ns

Note: Serial data is fetched at the rise of each clock pulse.

3. Relation between FC Pin Inputs and Phase Characteristics

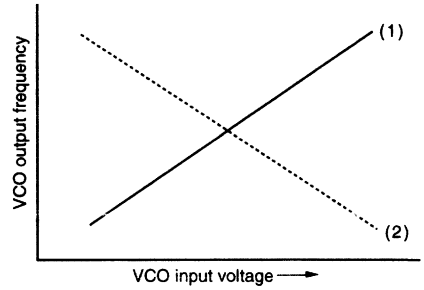
The FC pin is the phase switching pin for the phase comparator. Controlling the FC pin inverts the characteristics of the internal charge pump output (D_O) and phase comparator outputs (øR, øP). In addition, the phase comparator input monitor pin (fout) is also controlled via the FC pin. The following table lists relation between FC pin inputs and D_O, øR, øP, and fout:

	FC: "H" (or open)				FC: "L"			
	D_O	øR	øP	fout	D_O	øR	øP	fout
fr > fp	H	L	L	fr	L	H	Z	fp
fr < fp	L	H	Z		H	L	L	
fr = fp	Z	L	Z		Z	L	Z	

Z: High impedance

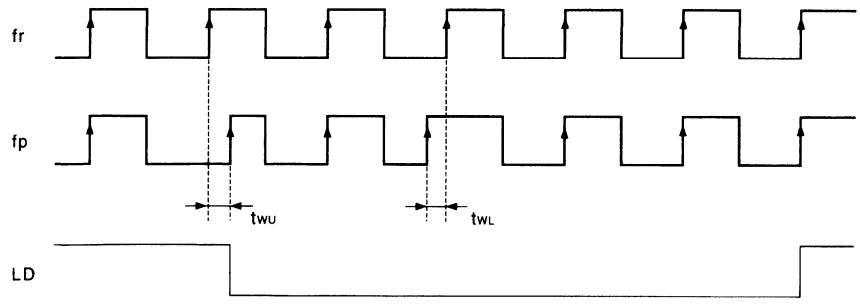
When disigning a synthesizer, control the FC pin depending on the VCO polarity.

- When the VCO polarity is (1)
  FC: "H" or open
- When the VCO polarity is (2)
  FC: "L"

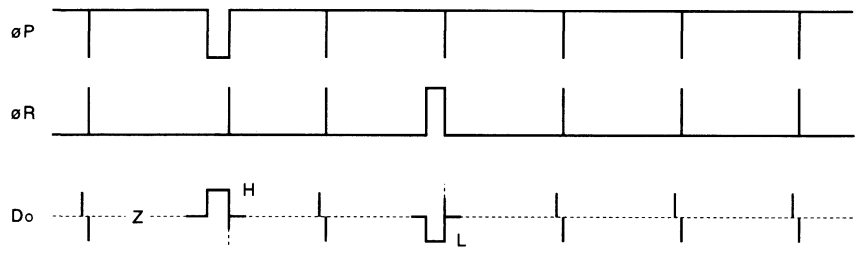


Note: When using an active lowpass filter, pay attention to its polarity.

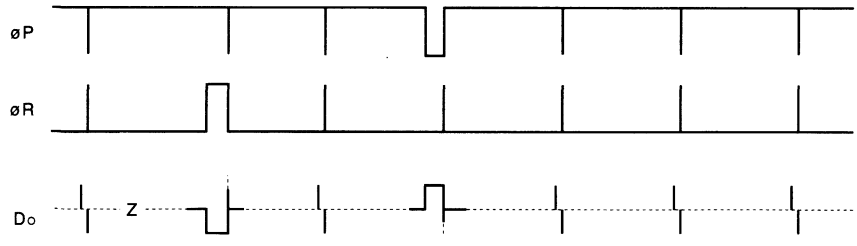
■ PHASE COMPARATOR OUTPUT WAVEFORMS



• When the FC bit = "H"



• When the FC bit = "L"



Notes:
- A phase difference is detected between -2π and $+2\pi$, with gain = $V_P/4\pi$.
- The LD output goes low when it becomes phase difference t_{WU} or more. The LD output goes high when it remains equal to or smaller than t_{WL} for three cycles or more.
- t_{WU} and t_{WL} are determined by the OSC_{IN} input frequency as follows:

  $t_{WU} \geq 8/f_{OSC}$ (s)

  When f_{OSC} = 12.8 MHz: $t_{WU} \geq 625$ ns

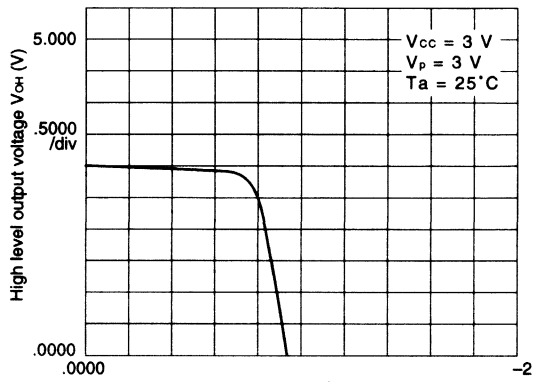
  $t_{WL} \leq 16/f_{OSC}$ (s)

  When f_{OSC} = 12.8 MHz: $t_{WL} \leq 1250$ ns

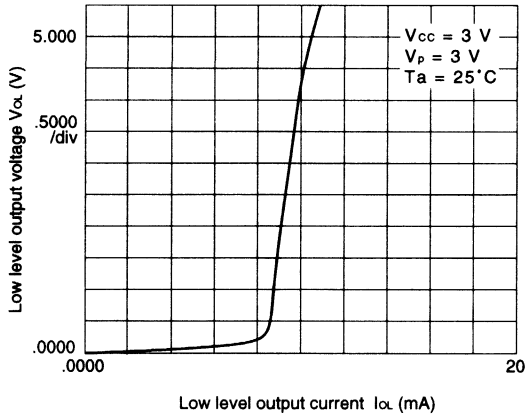
■ TYPICAL CHARACTERISTIC CURVES

1. D_O Output Current Characteristics

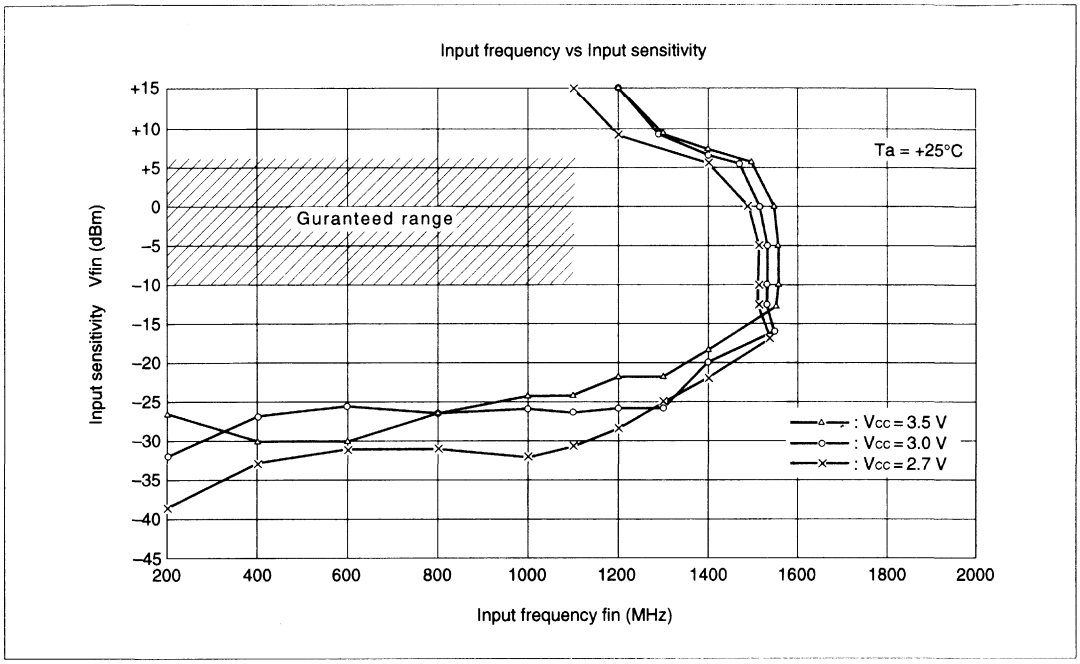
I_{OH} vs V_{OH} characteristics



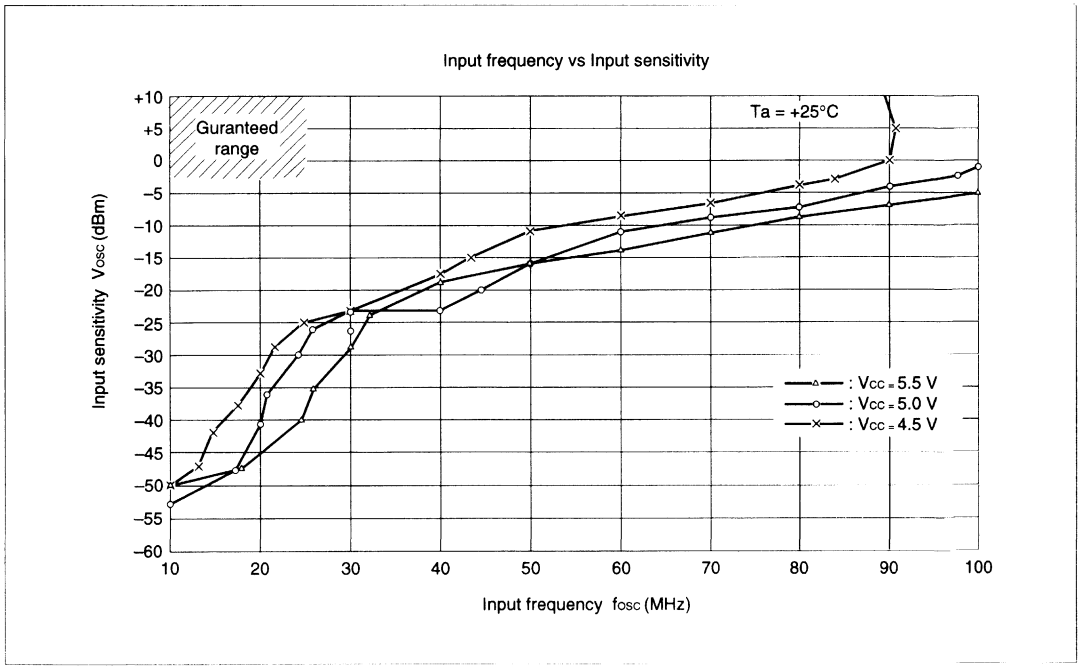
V_{OL} vs I_{OL} characteristics



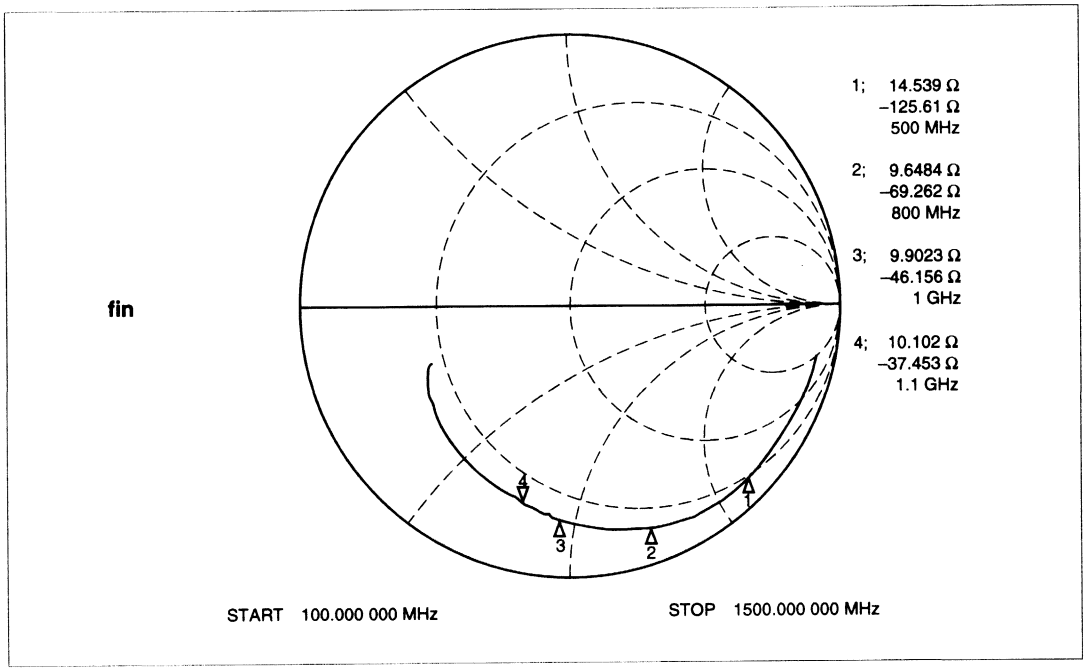
2. fin Input Sensitivity Characteristics



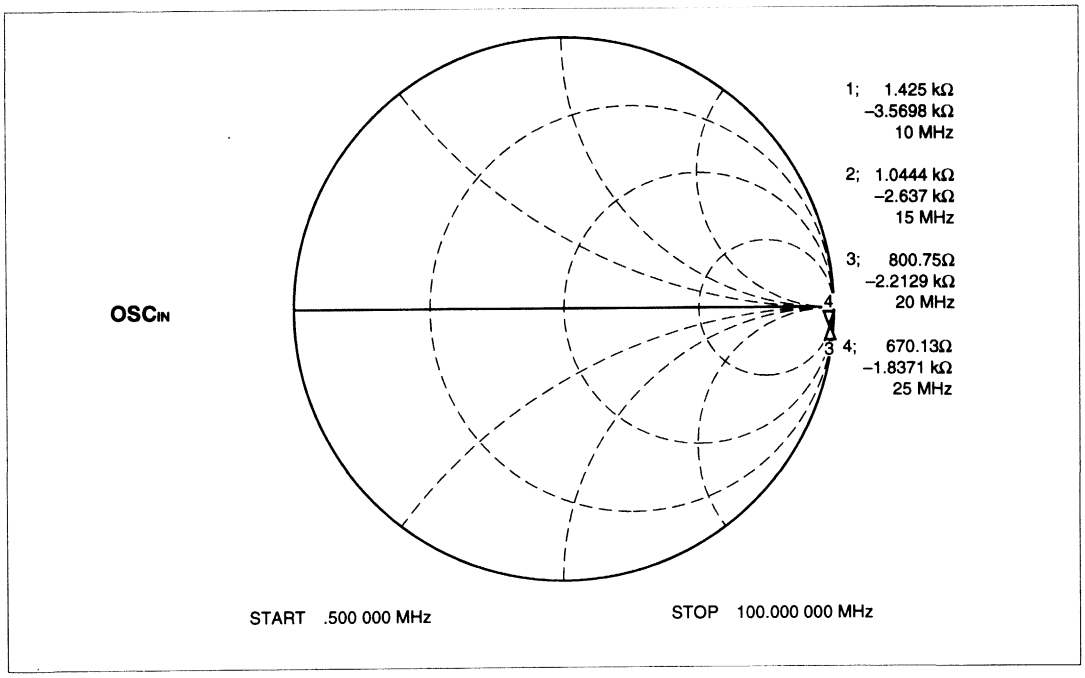
3. OSCIN Input Sensitivity Characteristics



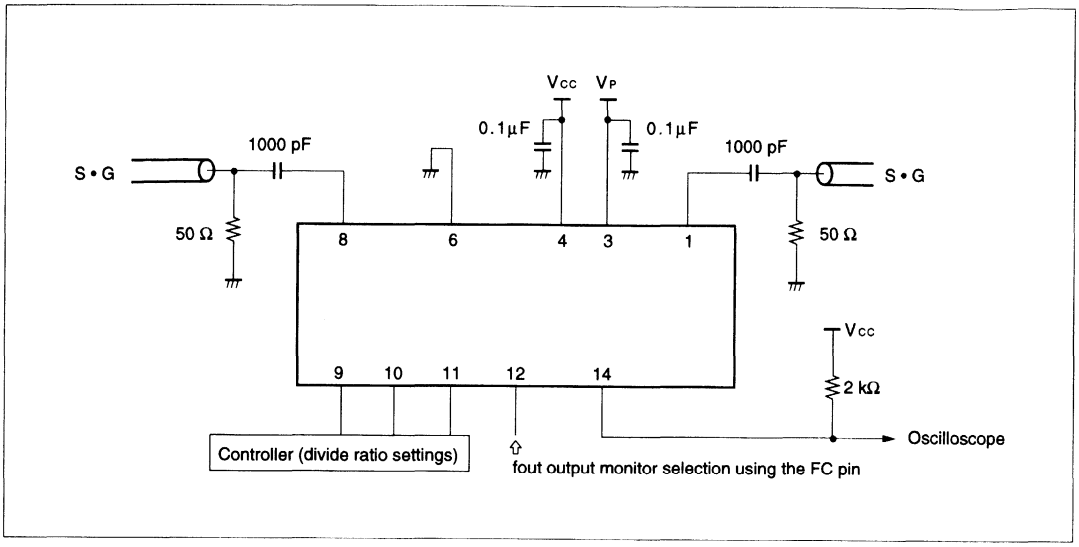
4. fin Input Impedance Characteristics



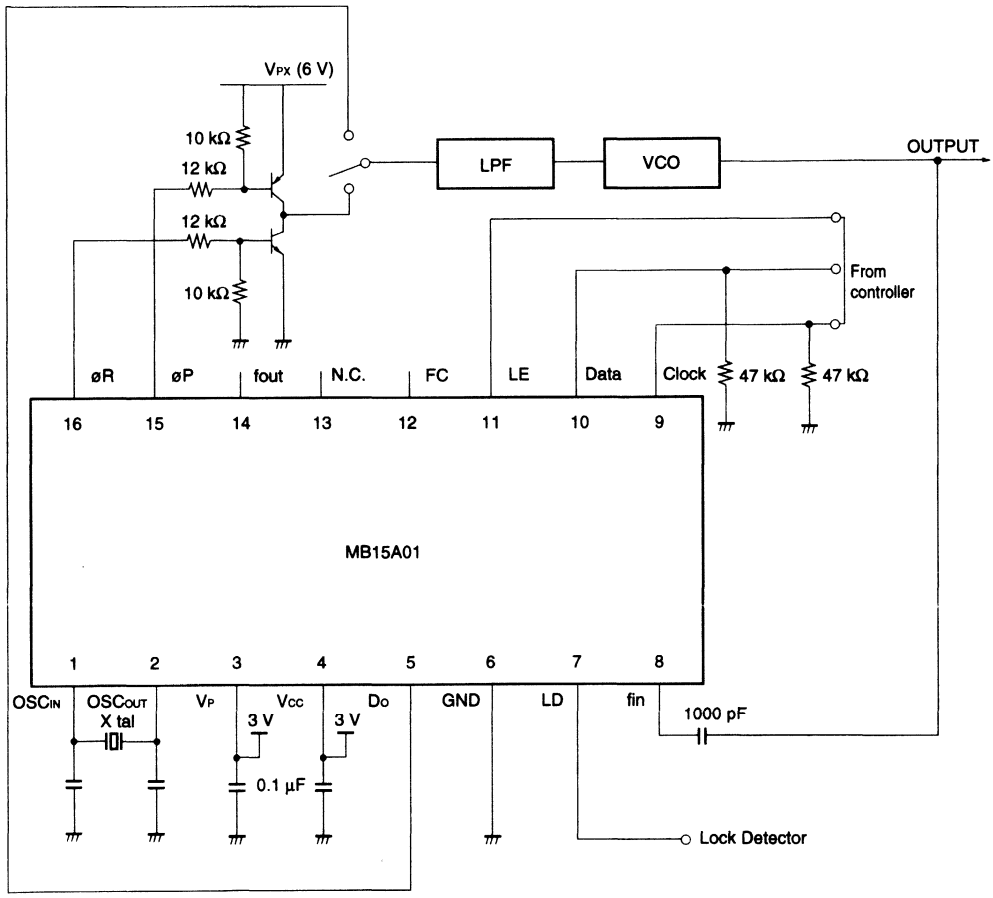
5. OSC_{IN} Input Impedance Characteristics



■ TEST CIRCUIT EXAMPLE (fin/OSC_{IN} Input Sensitivity Measurement)



■ APPLICATION EXAMPLE (16-pin Package)

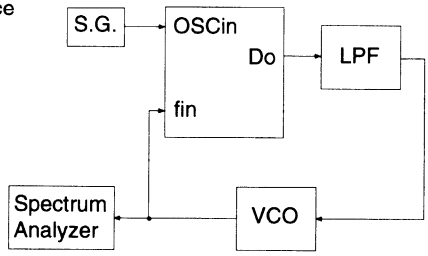


VPX : 6 V max.
VP : Connect the pin to VCC when the internal charge pump is not used.
LE, FC : With pull-up resistor
øP, fout : N channel open-drain output
øR : CMOS output

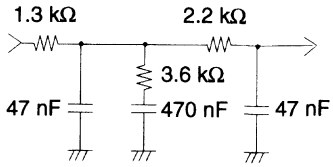
■ REFERENCE INFORMATION

Typical plots measured with the test circuit are shown below. Each plots show lock up time, phase noise, and reference leakage.

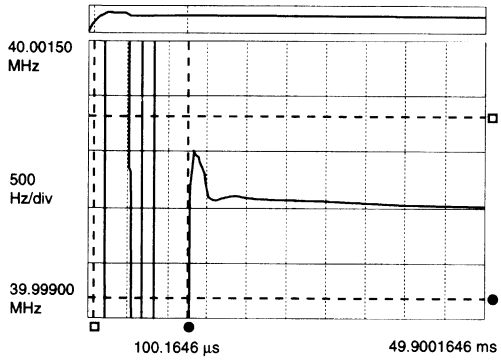
Test Circuit



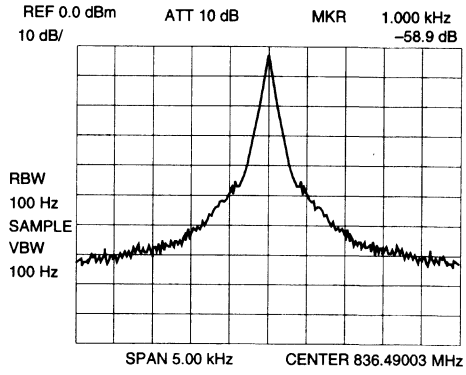
- f_{VCO} = 836.49 MHz
- K_V = 12 MHz/V
- f_r = 30 kHz
- f_{OSC} = 15.36 MHz
- LPF



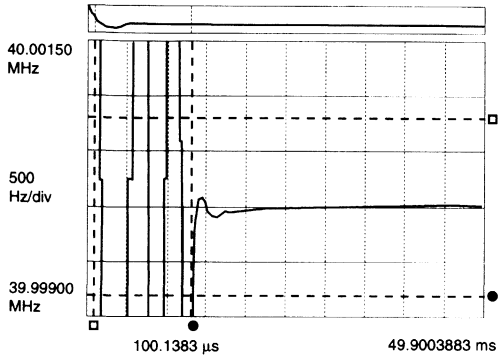
PLL Lock Up Time = 12 ms
(824.010 MHz → 848.97 MHz, within ±800 Hz)



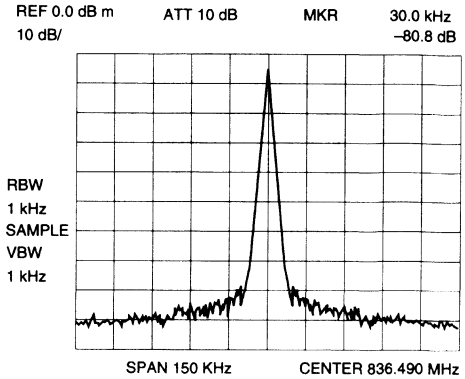
PLL Phase Noise
@ within loop band = 78.9 dBc/Hz



PLL Lock Up Time = 12.4 ms
(848.97 MHz → 824.019 MHz, within ±800 Hz)



PLL Reference Leakage
@ 30kHz offset = 80.8 dBc



■ ORDERING INFORMATION

Part number	Package	Remarks
MB15A01PFV1	16-pin, Plastic SSOP (FPT-16P-M05)	
MB15A01PFV2	20-pin, Plastic SSOP (FPT-20P-M03)	

MEMO

FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-21322-2E

ASSP

Dual Serial Input PLL Frequency Synthesizer

MB15B01

■ DESCRIPTION

The Fujitsu MB15B01 is a 1.1 GHz dual serial input PLL (Phase Locked Loop) frequency synthesizer designed for cellular phones, cordless phones and other radio applications.

The MB15B01 has two PLL circuits on a single chip: PLL1 and PLL2. An analog switch is provided for each PLL circuit to decrease lock up time. Separate power supply pins are provided for each PLL circuit.

Two 1.1 GHz dual modulus prescalers are included inside and enables a pulse swallow function.

It operates with a supply voltage of 3.0V typ. and dissipates 13 mA typ. of current realized through the use of Fujitsu's unique Bi-CMOS technology.

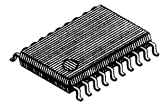
■ FEATURES

- High operating frequency: fin = 1.1 GHz (Vin = -10 dBm, V_{CC} = 3V)
- Pulse swallow function: 64/65 or 128/129
- Serial input 14-bit programmable reference divider: R = 8 to 16,383
- Serial input 18-bit programmable divider consisting of:
  - Binary 7-bit swallow counter: 0 to 127
  - Binary 11-bit programmable counter: 16 to 2,047

  Each programmable counter can be controlled independently.
- Low power supply voltage: V_{CC} = 2.7 to 3.5V
- Low power supply current: I_{CC} (total) = 13 mA typ. (V_{CC} = 3V)
- Power saving function : I_{CC1} = I_{CC2} = 100 µA typ (V_{CC} = 3V)
- On-chip analog switches achieve fast lock up time
- Digital lock detector
- Wide operating temperature: Ta = –30 to 80°C
- Plastic 20-pin SSOP package

■ PACKAGE

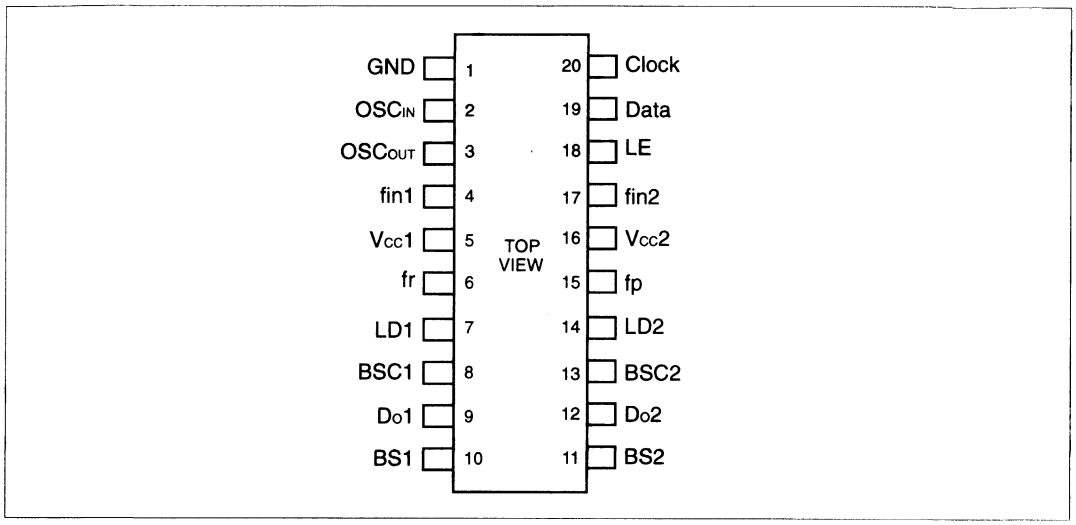
Plastic Flat Package



(FPT-20P-M03)

This device contains circuitry to protect the inputs against damage due to high static voltages or electroc fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

■ PIN ASSIGNMENT



■ PIN DESCRIPTIONS

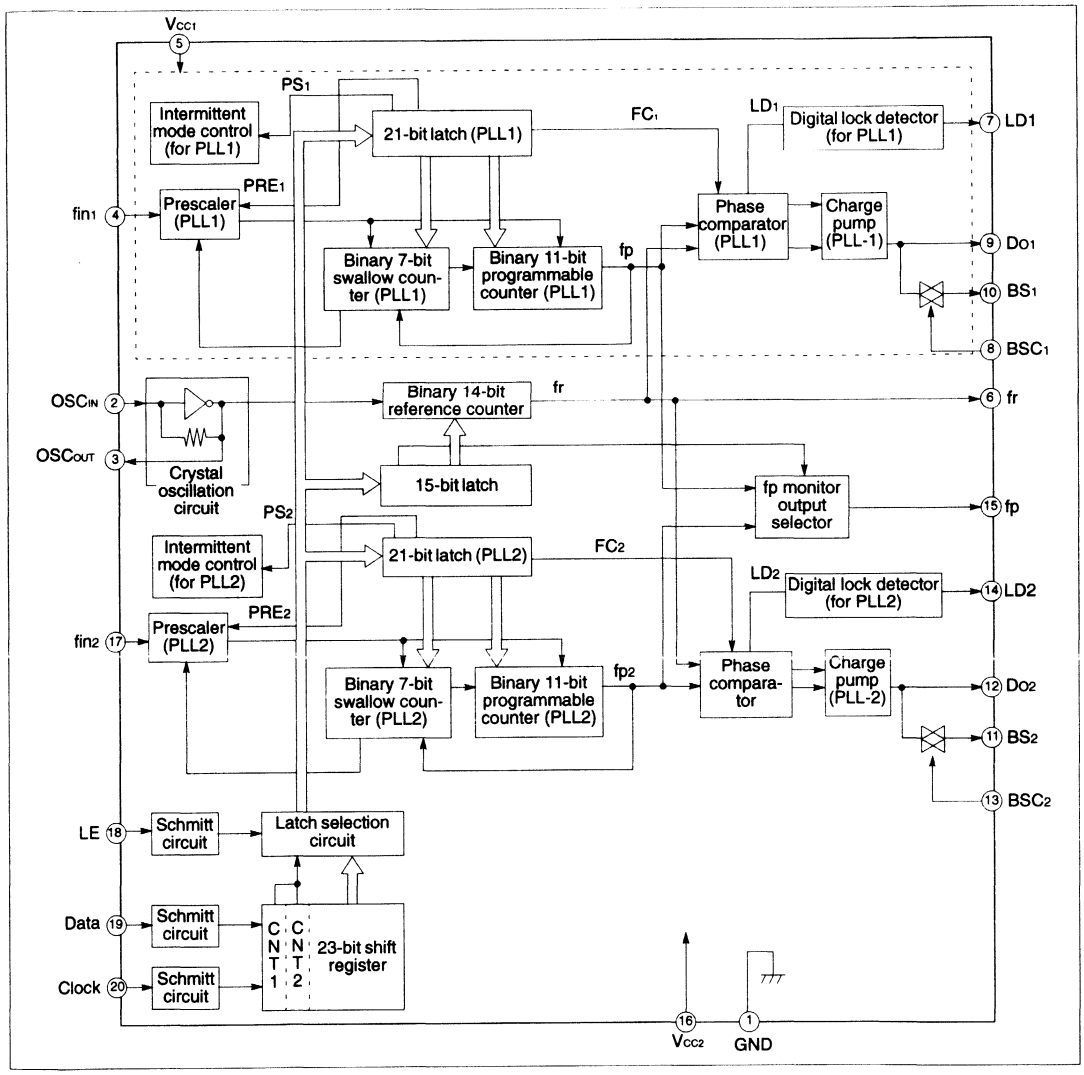
<table>
<tr><th>Pin No.</th><th>Pin name</th><th>I/O</th><th>Descriptions</th></tr>
<tr><td>1</td><td>GND</td><td>–</td><td>Ground</td></tr>
<tr><td>2
3</td><td>OSCIN
OSCOUT</td><td>I
O</td><td>Oscillator input pin.
Oscillator output pin.
A crystal is connected between OSCIN pin and OSCOUT pin.</td></tr>
<tr><td>4</td><td>fin1</td><td>I</td><td>Prescaler input pin of PLL1 section.
The connection with VCO should be AC coupling.</td></tr>
<tr><td>5</td><td>Vcc1</td><td>–</td><td>Power supply voltage input pin of PLL1 section.
When power is OFF, latched data of PLL1 section is cancelled.</td></tr>
<tr><td>6</td><td>fr</td><td>O</td><td>Monitor pin for programmable reference divider output. (Open drain output)</td></tr>
<tr><td>7</td><td>LD1</td><td>O</td><td>Lock detect signal output pin of PLL1 section.
<table>
<tr><th>Status</th><th>LD pin output level</th></tr>
<tr><td>Lock</td><td>H</td></tr>
<tr><td>Unlock</td><td>L</td></tr>
</table></td></tr>
<tr><td>8</td><td>BSC1</td><td>I</td><td>Analog switch control pin of PLL1 section.
<table>
<tr><th>BSC1</th><th>BS1 pin output</th></tr>
<tr><td>L</td><td>High-impedance</td></tr>
<tr><td>H</td><td>Charge pump output</td></tr>
</table></td></tr>
<tr><td>9</td><td>Do1</td><td>O</td><td>Charge pump output pin of PLL1 section.
Phase characteristics of the phase detector can be reversed depending upon FC-bit setting.</td></tr>
<tr><td>10</td><td>BS1</td><td>O</td><td>Analog switch output pin of PLL1 section, and controlled by BSC1.</td></tr>
<tr><td>11</td><td>BS2</td><td>O</td><td>Analog switch output pin of PLL2 section, and controlled by BSC2.</td></tr>
<tr><td>12</td><td>Do2</td><td>O</td><td>Charge pump output pin of PLL2 section.
Phase characteristics of the phase detector can be reversed depending upon FC-bit setting.</td></tr>
<tr><td>13</td><td>BSC2</td><td>I</td><td>Analog switch control pin of PLL2 section.
<table>
<tr><th>BSC2</th><th>BS2 pin output</th></tr>
<tr><td>L</td><td>High-impedance</td></tr>
<tr><td>H</td><td>Charge pump output</td></tr>
</table></td></tr>
<tr><td>14</td><td>LD2</td><td>O</td><td>Lock detection signal output pin of PLL2 section.
<table>
<tr><th>Status</th><th>LD pin output level</th></tr>
<tr><td>Lock</td><td>H</td></tr>
<tr><td>Unlock</td><td>L</td></tr>
</table></td></tr>
<tr><td>15</td><td>fp</td><td>O</td><td>Monitor pin for programmable divider output. (Open drain output)
This pin outputs divided frequency of PLL1 section or PLL2 section depending upon FP bit setting.
<table>
<tr><th>FP bit</th><th>Output</th></tr>
<tr><td>H</td><td>PLL1 section (fp1)</td></tr>
<tr><td>L</td><td>PLL2 section (fp2)</td></tr>
</table></td></tr>
</table>

(Continued)

(Continued)

Pin No.	Pin name	I/O	Descriptions
16	V_{CC2}	–	Power supply voltage input pin for PLL2 section, programmable reference divider, shift register, and cyrstal oscilator. When power is OFF, latched data of PLL2 section and reference counter is cancelled.
17	fin2	I	Prescaler input pin of PLL2 section. The connection with VCO should be AC coupling.
18	LE	I	Load enable input pin. This pin is followed by a schmitt trigger circuit. When this pin is high, the data stored in the shift register is transferred into the latch depending on control data.
19	Data	I	Serial data input pin of 23-bit shift register. This pin is followed by a schmitt trigger circuit. The stored data in the shift register is transferred to one of PLL1 programmable counter, PLL2 programmable counter and programmable reference counter depending upon control data settings.
20	Clock	I	Clock input pin of 23-bit shift register. This pin is followed by a shmitt trigger circuit. On rising edge of the clock, one bit of data is transferred into the shift register.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Remark
Power supply voltage	V_{CC}	−0.5 to +5.0	V	
Output voltage	V_{OUT}	−0.5 to V_{CC} +0.5	V	
Open drain voltage	V_{OOP}	−0.5 to +0.5	V	fr, fp
Output current	I_{OUT}	±10	mA	
Storage temperature	T_{STG}	−55 to +125	°C	

Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power supply voltage	V_{CC}	2.7	3.0	3.5	V	$V_{CC1} = V_{CC2}$
Input voltage	V_{IN}	GND	−	V_{CC}	V	
Operating temperature	Ta	−30	−	+80	°C	

Handling Precautions

- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover workbenches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

■ ELECTRICAL CHARACTERISTICS

Parameter		Symbol	Condition	Value			Unit
				Min.	Typ.	Max.	
Power supply current		I_{CC1}	PLL1 section	–	6.0 (0.1)*1	–	mA
		I_{CC2}	PLL2 & common sections	–	7.0 (0.1)*1	–	
Operating frequency	fin	fin		100	–	1100	MHz
	OSC_{IN}	f_{OSC}		–	12.8	20.0	
Input sensitivity	fin	Vfin	50 Ω (Refer to TEST CIRCUIT)	–10	–	0	dBm
	OSC_{IN}	V_{OSC}		0.5	–	–	V_{p-p}
High-level input voltage	Data, Clock, LE, BSC	V_{IH}		$V_{CC} \times 0.7 + 0.4$	–	–	V
Low-level input voltage		V_{IL}		–	–	$V_{CC} \times 0.3 - 0.4$	
High-level input current	Data, Clock, LE, BSC	I_{IH}		–	1.0	–	µA
Low-level input current		I_{IL}		–	–1.0	–	
Input current	OSC_{IN}	I_{OSC}		–	±50	–	
High-level output voltage	LD	V_{OH}	Vcc = 3.0V	2.2	–	–	V
Low-level output voltage		V_{OL}	Vcc = 3.0V	–	–	0.4	
High-impedance cutoff current	Do,BS	I_{OFF}		–	–	1.1	µA
Output current	LD	I_{OH}		–1.0	–	–	mA
		I_{OL}		–	–	1.0	
	Do 1, 2	I_{OH}	Vcc = 3.0V	–	–2.5	–	mA
		I_{OL}	Vcc = 3.0V	–	5.0	–	
Analog switch ON resistance		R_{ON}		–	50	–	Ω

*1: The value in ( ) is power supply current in power saving mode.

■ FUNCTIONAL DESCRIPTION

The divide ratio can be calculated using the following equation:

$f_{VCO} = \{(P \times N) + A\} \times f_{OSC} \div R \quad (A < N)$

f_{VCO}: Output frequency of external voltage controlled ocillator (VCO)
P: Preset divide ratio of dual modulus prescaler (64 or 128)
N: Preset divide ratio of binary 11-bit programmable counter (16 to 2,047)
A: Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$)
f_{OSC}: Reference oscillation frequency
R: Preset divide ratio of binary 14-bit programmable reference counter (8 to 16,383)

Serial Data Input

Serial data is entered using three pins, Data pin, Clock pin, and LE pin. Programmable counters of PLL1 section and PLL2 section, and programmable reference counter are controlled individually.
Serial data of binary data is entered via Data pin.
On rising edge of clock, one bit of serial data is transferred into the shift register. When load enable signal is high, the data stored in the shift register is transferred to one of latch of them depending upon the control bit data setting.

Control bit		Destination of serial data
CN1	CN2	
L	L	Reference counter
L	H	Programmable counter of PLL1
H	H	Programmable counter of PLL2

Shift Register Configuration

Programmable Reference Counter

LSB ↓ Data Flow → MSB ↓

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
CN1	CN2	FP	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14

R1 to R14 : Divide ratio setting bit for the programmable counter (8 to 16,383)
FP : Test purpose bit (monitor output fp1/fp2 selection)
CN1, 2 : Control bit

Programmable Counter

LSB ↓ Data Flow → MSB ↓

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
CN1	CN2	PS	PRE	FC	A1	A2	A3	A4	A5	A6	A7	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11

N1 to N11 : Divide ratio setting bit for the programmable counter (16 to 2,047)
A1 to A7 : Divide ratio setting bit for the swallow counter (0 to 127)
FC : Phase control bit for the phase detector
PRE : Divide ratio setting bit for the prescaler (64/65, 128/129)
PS : Power saving control bit
CN1, 2 : Control bit

Binary 14-bit Programmable Reference Counter Data Setting

Divide ratio (R)	R 14	R 13	R 12	R 11	R 10	R 9	R 8	R 7	R 6	R 5	R 4	R 3	R 2	R 1
8	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	1	0	0	1
·	·	·	·	·	·	·	·	·	·	·	·	·	·	·
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: • Divide ratio less than 8 is prohibited.
• Divide ratio (R) range = 8 to 16383

Binary 11-bit Programmable Counter Data Setting

Divide ratio (N)	N 11	N 10	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1
16	0	0	0	0	0	0	1	0	1	0	0
17	0	0	0	0	0	0	1	0	1	1	1
·	·	·	·	·	·	·	·	·	·	·	·
2047	1	1	1	1	1	1	1	1	1	1	1

Note: • Divide ratio less than 16 is prohibited.
• Divide ratio (N) range = 16 to 2047

Binary 7-bit Swallow Counter Data Setting

Divide ratio (A)	A 7	A 6	A 5	A 4	A 3	A 2	A 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
·	·	·	·	·	·	·	·
127	1	1	1	1	1	1	1

Note: • Divide ratio (A) range = 0 to 127

Prescaler Data Setting

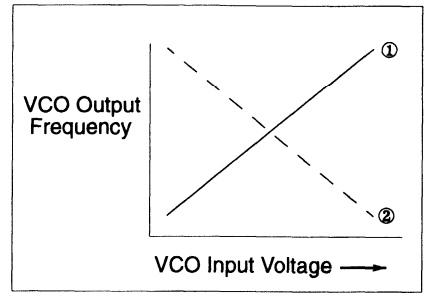
Divide Ratio	PRE
64/65	1
128/129	0

Note: • Divide ratio for each PLL1 and PLL2 is set by the serial data at that time of divide ratio setting for each programmable divider.

Phase Comparator Phase Switching Data Setting

	FC = H	FC = L
fr > fp	H	L
fr = fp	Z	Z
fr < fp	L	H
VCO polarity	①	②

Note: • Z = High–impedance
• Depending upon the VCO polarity, FC bit should be set.
• Phase characteristic for each PLL1 and PLL2 is set by the serial data at that time of divide ratio setting for each programmable divider.



Power Saving Function Control (Intermittent Operation)

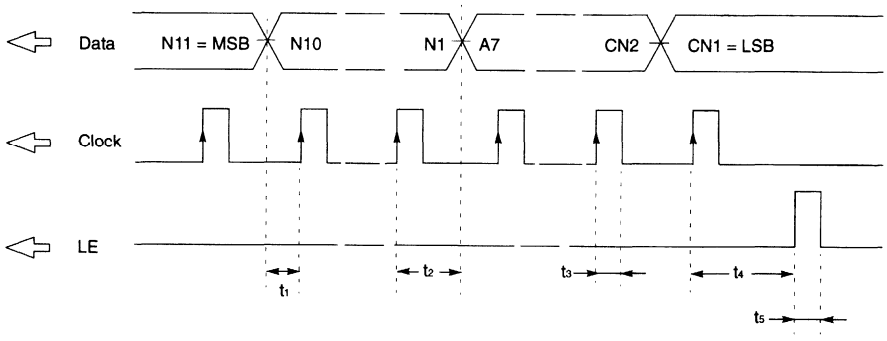
	PS	
	H	L
PLL1's section	ON	OFF
PLL2's section and common section	ON	OFF

Note: • Power saving mode for each PLL1 and PLL2 is selected by the serial data at that timeof divide ratio setting for each programmable divider.
• Common section; Crystal oscillator circuit, reference counter
• Just after powering up, please set PS bit to "L" at first.

Intermittent operation limits power consumption by shutting down or start the internal circuits case by case. If device operation resumes uncontrolled, the error signal output from the phase comparator may exceed the limit due to an undefined phase relationship between the reference frequency (f_R) and the comparison frequency (f_P) and frequency lock is lost.
To prevent this, an intermittent operation control circuit is provided to decrease the variation in the locking frequency by forcibly correcting phase of both frequencies to limit the error signal output.

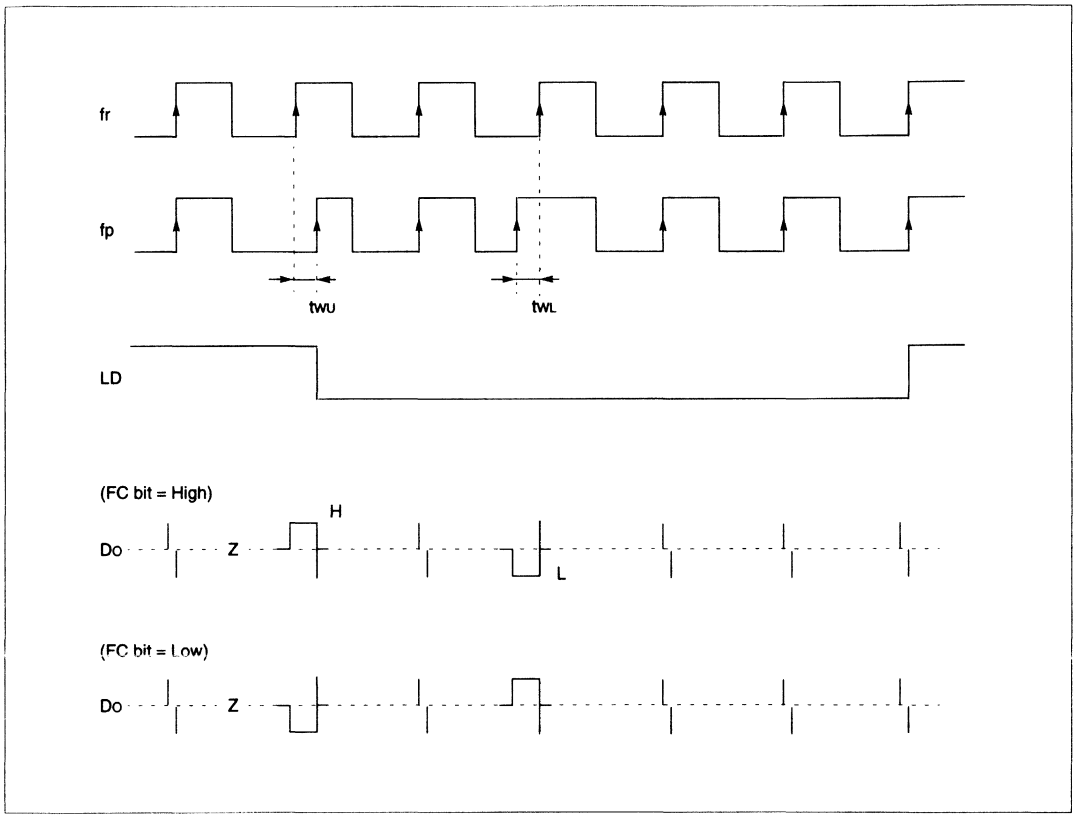
Serial Data Input Timing

t1 (>100ns) : Data set up time t2 (>1000ns) : Data hold time t3 (>300ns) : Clock pulse width
t4 (>100ns) : LE set up time to the rising edge of the last clock t5 (>800ns) : LE pulse width



On rising edge of the clock, one bit of the data is transferred into the shift register.

■ PHASE DETECTOR OUTPUT WAVEFORM

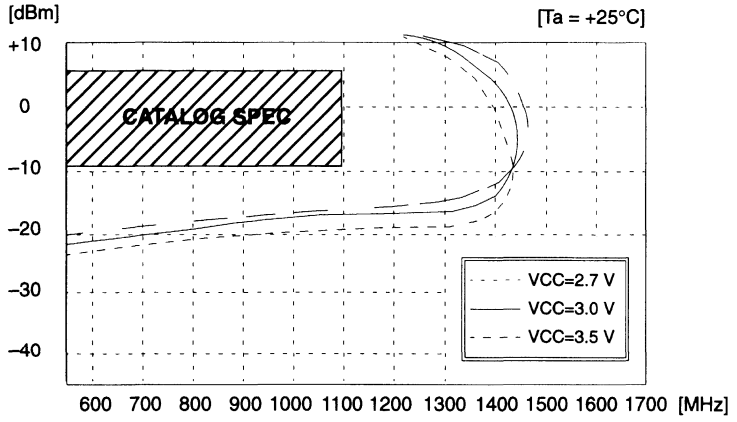


Note: • Phase error detection range = -2π to $+2\pi$

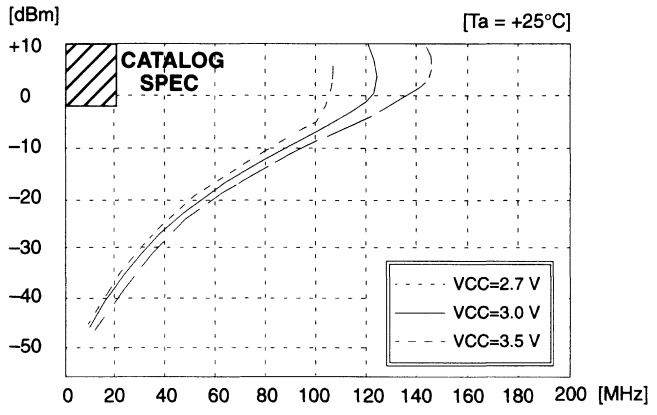
- LD output becomes low when phase error is twu or more.
- LD output becomes high when phase error is twL or less and continues to be so for three cycles or more.
- twu and twL depend on OSCin input frequency.
  twu ≥ 8/fosc: (e.g. twu ≥ 625ns when foscin = 12.8 MHz)
  twL ≤ 16/fosc: (e.g. twL ≤ 1250ns when foscin = 12.8 MHz)

■ TYPICAL CHARACTERISTICS

Input sensivity of f_{IN} (RF) vs. Input Frequency



Input sensivity of OSC vs. Input Frequency



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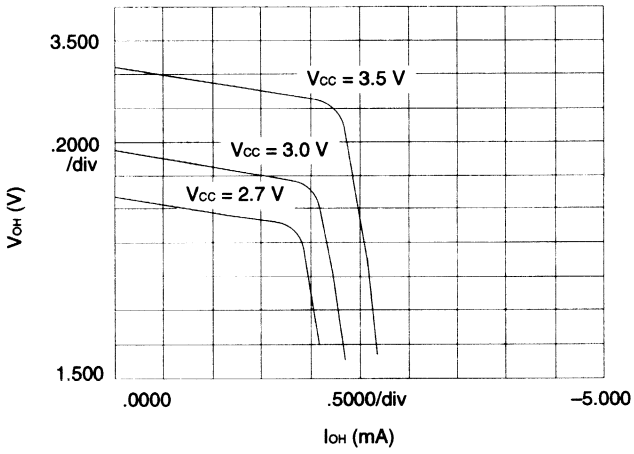
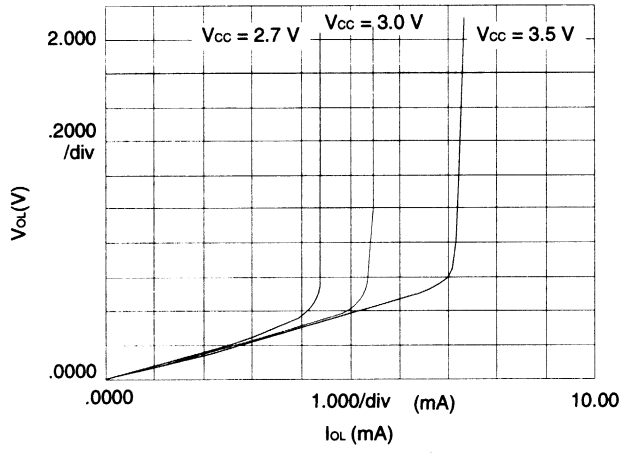
Do output Current





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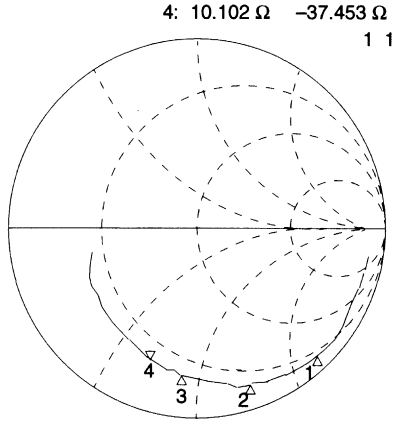
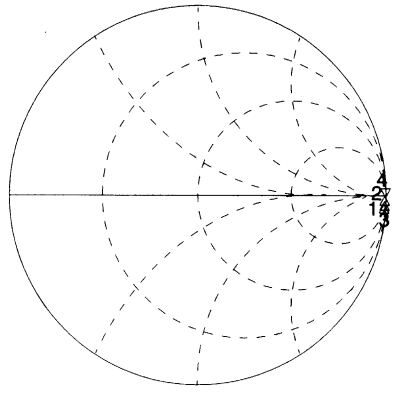
Input Impedance

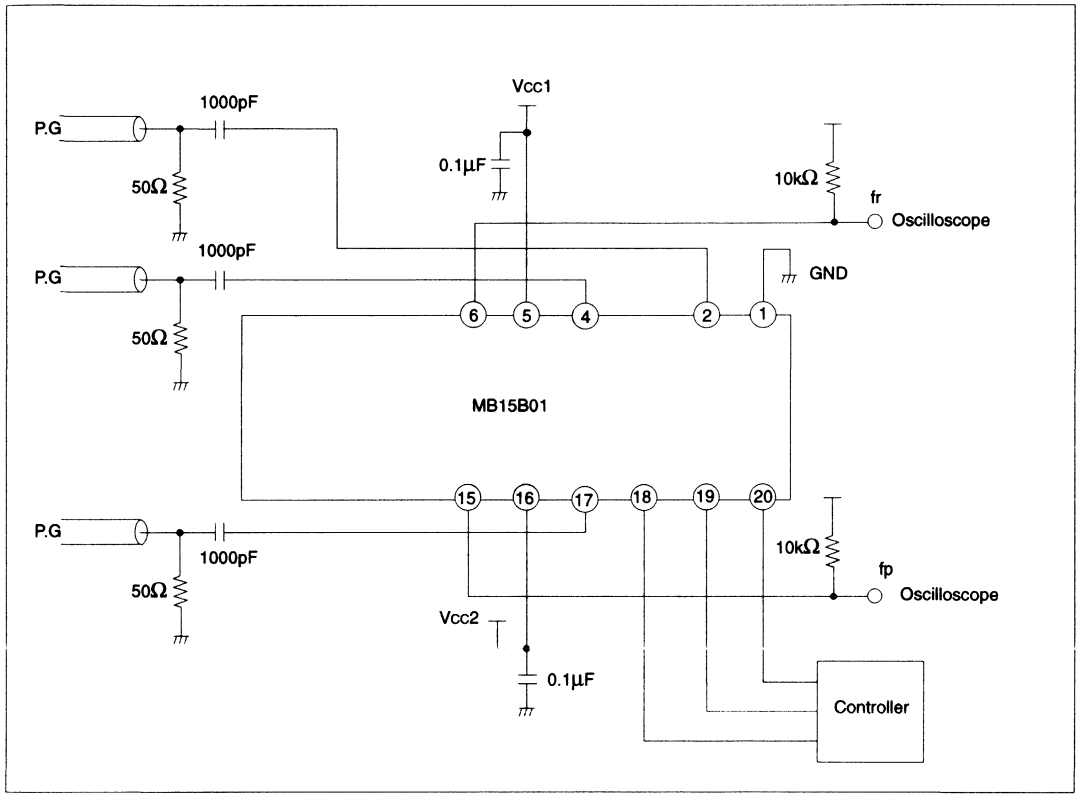
finRF Pin



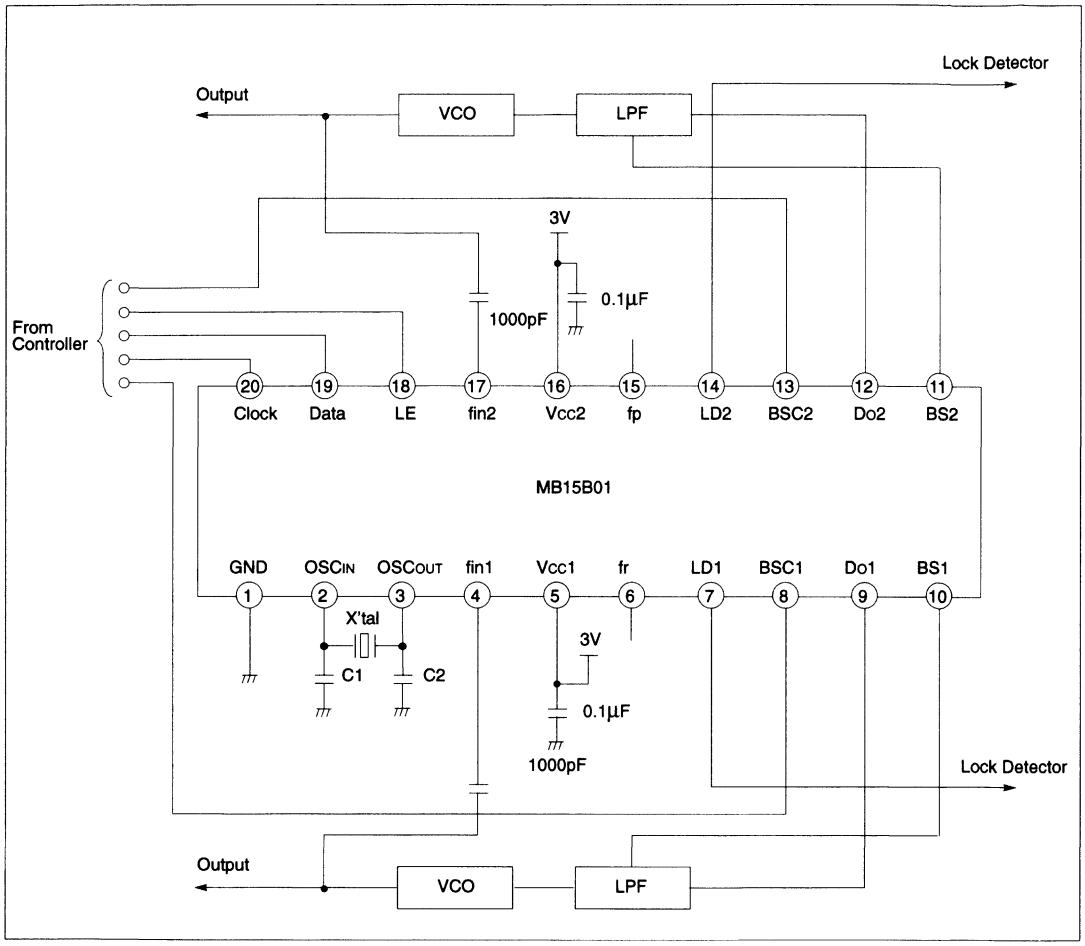
OSCin Pin



■ TEST CIRCUIT (Prescaler Input Sensitivity Test)



■ APPLICATION EXAMPLE

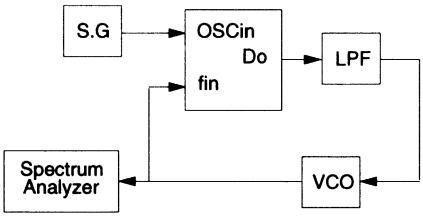


Note: C1, C2 : depends on a crystal oscillator.
Clock, Data, LE : involves a schmitt circuit.
When input pins are open, please insert the pull down/up resistor individually to prevent oscillation.

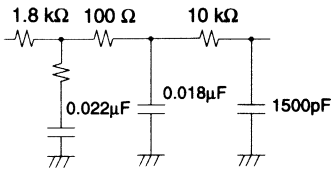
■ REFERENCE INFORMATION

Typical plots measured with the test circuit are shown below. Each plot shows lock up time, phase noise and reference leakage.

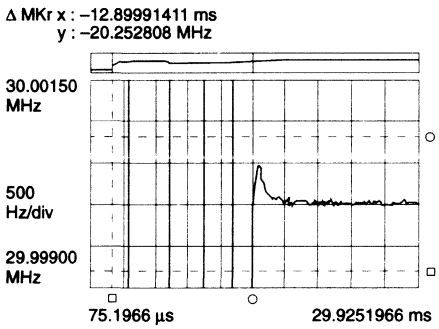
Test Circuit



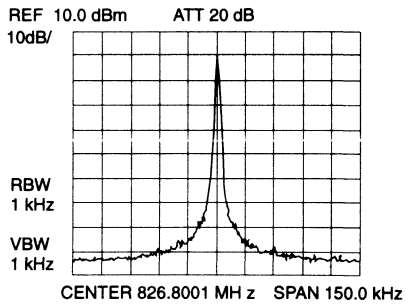
- fvco = 826.8 MHz
- Kv = 9.7 MHz/v
- fr = 30 kHz
- fosc = 10 MHz
- LPF:



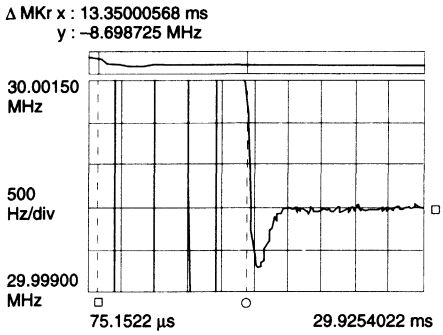
PLL Lock Up Time = 12.9 ms
(822.6 MHz → 831.3 MHz, within ± 800 Hz)



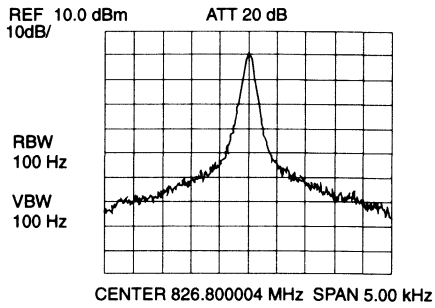
PLL Phase Noise
@ within loop band = 74 dBc/Hz



PLL Lock Up Time = 13.4 ms
(831.3 MHz → 822.6 MHz, within ± 800 Hz)



PLL Reference Leakage
@ 30 kHz offset = 80 dBc



■ ORDERING INFORMATION

Part number	Package	Remarks
MB15B01 PFV	20pin, Plastic SSOP (FPT-20P-M03)	

FUJITSU SEMICONDUCTOR
DATA SHEET

DS04–21309–2E

ASSP

SERIAL INPUT PLL FREQUENCY SYNTHESIZER

MB1511

■ DESCRIPTION

The Fujitsu MB1511 is a single chip serial input PLL frequency synthesizer designed for VHF tuner and cellular telephone applications.

It contains a 1.1 GHz dual modulus prescaler which enables pulse swallow function, and an analog switch to speed up lock up time.

It operates supply voltage of 3.0 V typ. and dissipates 7 mA typ. of current realized through the use of Fujitsu's unique U-ESBIC Bi-CMOS technology.

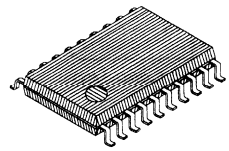
The MB1511 is housed in SSOP package, this enables high integration.

■ FEATURES

- Low power supply voltage: V_{CC} = 2.7 to 5.5 V
- High operating frequency: $f_{IN\ MAX}$ = 1.1 GHz ($V_{IN\ MIN}$ = −10dBm)
- Pulse swallow function: 64/65 or 128/129
- Low supply current: I_{CC} = 7 mA typ.

(Continued)

■ PACKAGE

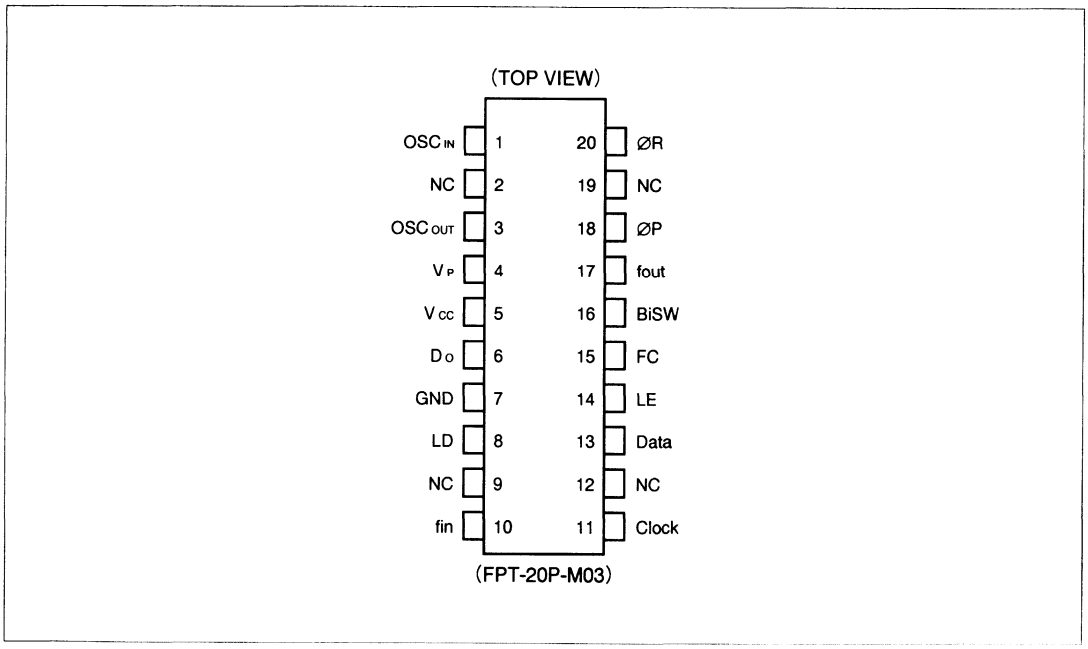


PLASTIC PACKAGE
FPT-20P-M03

(Continued)

- Serial input 18-bit programmable divider consisting of:
  Binary 7-bit swallow counter: 0 to 127
  Binary 11-bit programmable counter: 16 to 2047
- Serial input 15-bit programmable reference divider consisting of:
  Binary 14-bit programmable reference counter: 8 to 16383
  1-bit switch counter (SW) sets divide ratio of prescaler
- On-chip analog switch achieves fast lock up time
- 2 types of phase detector output
  On-chip charge pump (Bipolar type)
  Output for external charge pump
- Wide operating temperature: –40°C to +85°C
- 20-pin Plastic Shrink Small Outline Package (Suffix: –PFV)

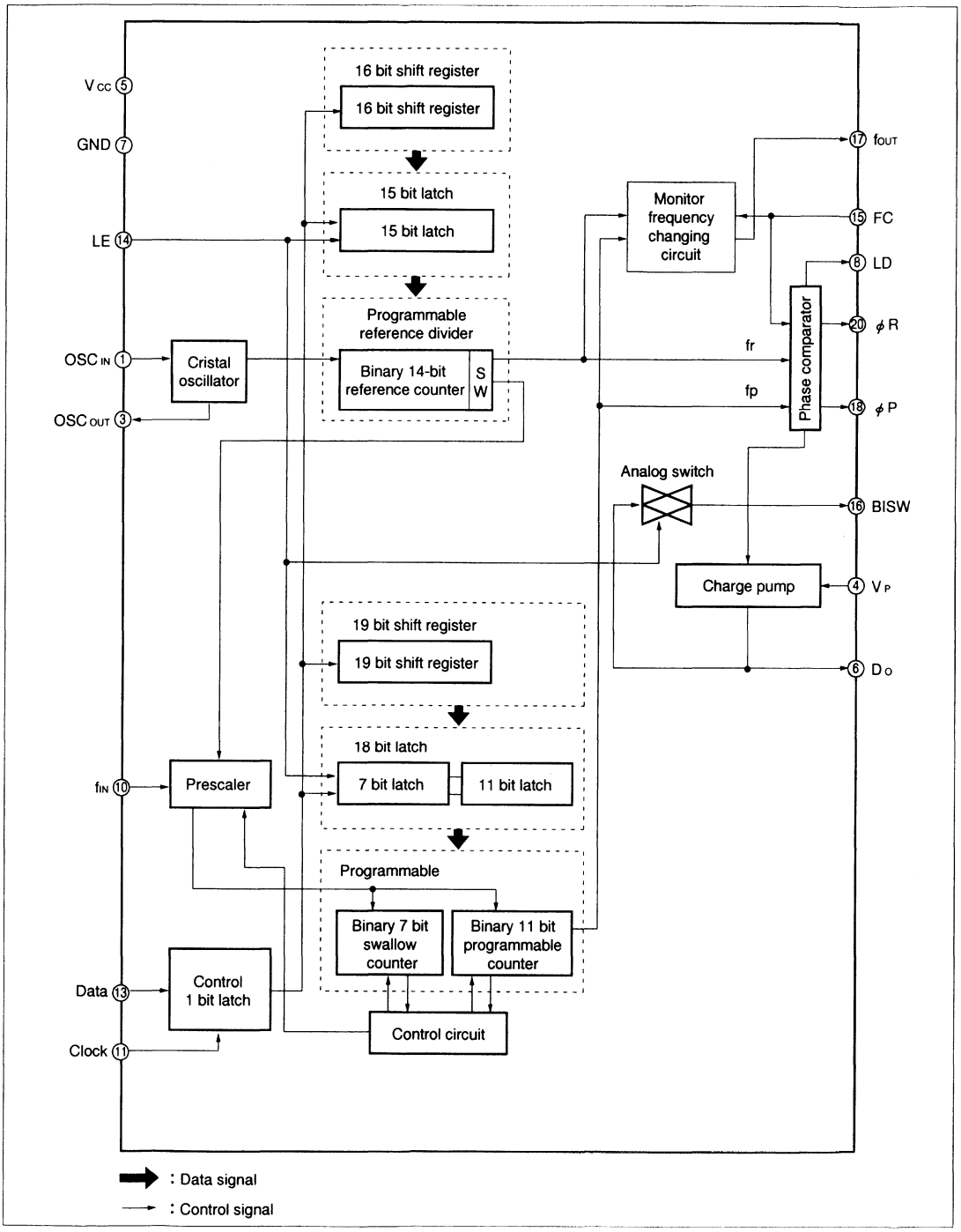
■ PIN ASSIGNMENT



■ PIN DESCRIPTION

Pin No.	Pin Name	I/O	Description
1	OSC_{IN}	I	Oscillator input. Oscillator output. A crystal is placed between OSC_{IN} and OSC_{OUT}.
3	OSC_{OUT}	O	
4	V_P	—	Power supply input for charge pump and analog switch.
5	V_{CC}	—	Power supply voltage input.
6	D_O	O	Charge pump output. The characteristics of charge pump is reversed depending upon FC input.
7	GND	—	Ground.
8	LD	O	Phase comparator output. Normally this pin outputs high level. While the phase difference of f_r and f_p exists, this pin outputs low level.
10	f_{IN}	I	Prescaler input. The connection with an external VCO should be AC connection.
11	Clock	I	Clock input for 19-bit shift register and 16-bit shift register. On rising edge of the clock shifts one bit of data into the shift registers.
13	Data	I	Binary serial data input. The last bit of the data is a control bit which specified destination of shift registers. When this bit is high level and LE is high level, the data stored in shift register is transferred to 15-bit latch. When this bit is low level and LE is high level, the data is transferred to 18-bit latch.
14	LE	I	Load enable input (with internal pull up resistor). When LE is high or open, the data stored in shift register is transferred into latch depending upon the control bit. At the time, internal charge pump output is connected to BISW pin because internal analog switch becomes ON state.
15	FC	I	Phase select input of phase comparator (with internal pull up resistor). When FC is low level, the characteristics of charge pump, phase comparator is reversed. FC input signal controls f_{out} pin (test pin) output level, f_r or f_p.
16	BISW	O	Analog switch output. Usually BISW pin is set high-impedance state. When internal analog switch is ON (LE pin is high level), this pin outputs internal charge pump output.
17	f_{OUT}	O	Minitor pin of phase comparator input. f_{out} pin outputs either programmable reference divider output (f_r) or programmable divider output (f_p) depending upon FC pin input level. FC = H: It is the same as f_r output level. FC = L: It is the same as f_p output level.
18	ØP	O	Output for external charge pump. The characteristics are reversed according to FC input. ØP pin is N-channel open drain output.
20	ØR	O	
2, 9 12, 19	NC	—	No connection.

■ BLOCK DIAGRAM



■ FUNCTIONAL DESCRIPTIONS

1. PULSE SWALLOW FUNCTION

The divide ratio is set using the following equation.

$$fvco = [(M \times N) + A] \times fosc \div R$$

fvco : Output frequency of external voltage controlled oscillator (VCO)
M : Preset modulus of external dual modulus prescaler (64 or 128)
N : Preset divide ratio of binary 11-bit programmable counter (16 to 2047)
A : Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$, $A < N$)
fosc : Output frequency of the external reference frequency oscillator
R : Preset divide ratio of binary 14-bit programmable reference counter (8 to 16383)

2. SERIAL DATA INPUT

Serial data input is achieved by three inputs, such as Data pin, Clock pin and LE pin. Serial data input controls 15-bit programmable reference divider and 18-bit programmable divider, respectively.

Binary serial data is input to Data pin.

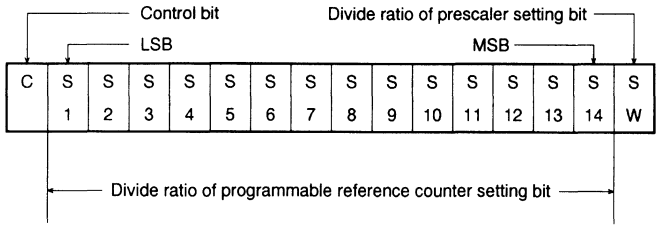
On rising edge of clock shifts one bit of serial data into the internal shift registers and when load enable pin is high level or open, stored data is transferred into latch depending upon the control bit.

Control data "H" data is transferred into 15-bit latch.

Control data "L" data is transferred into 18-bit latch.

(1) PROGRAMMABLE REFERENCE DIVIDER

Programmable reference divider consists of 16-bit shift register, 15-bit latch and 14-bit reference counter. Serial 16-bit data format is shown below.



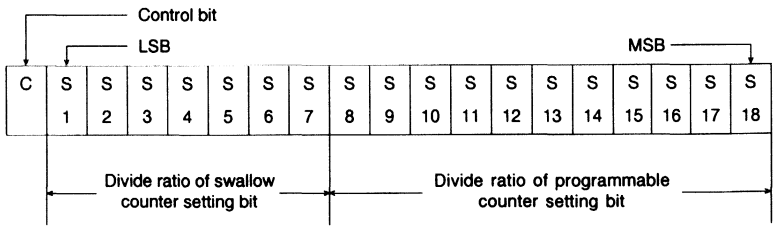
· 14-BIT PROGRAMMABLE REFERENCE COUNTER DIVIDE RATIO

Divide Ratio R	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1
8	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	1	0	0	1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

NOTES: Divide ratio less than 8 is prohibited.
Divide ratio: 8 to 16383
SW: This bit selects divide ratio of prescaler.
SW = H: 64/65
SW = L: 128/129
S1 to S14: These bits select divide ratio of programmable reference divider.
C: Control bit (sets as high level).
Data is input from MSB side.

(2) PROGRAMMABLE DIVIDER

Programmable divider consists of 19-bit shift register, 18-bit latch, 7-bit swallow counter and 11-bit programmable counter. Serial 19-bit data format is shown following page.



· 7-BIT SWALLOW COUNTER DIVIDE RATIO

Divide Ratio A	S7	S6	S5	S4	S3	S2	S1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
127	1	1	1	1	1	1	1

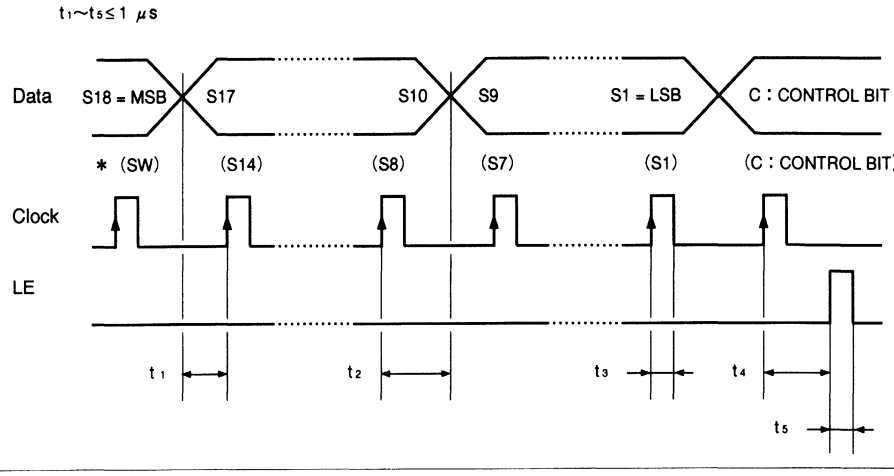
NOTE: Divide ratio: 0 to 127

· 11-BIT PROGRAMMABLE COUNTER DIVIDE RATIO

Divide Ratio N	S18	S17	S16	S15	S14	S13	S12	S11	S10	S9	S8
16	0	0	0	0	0	0	1	0	0	0	1
17	0	0	0	0	0	0	1	0	0	0	1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
2047	1	1	1	1	1	1	1	1	1	1	1

NOTES. Divide ratio less than 16 is prohibited.
Divide ratio: 16 to 2047
S1 to S7: Swallow counter divide ratio setting bit. (0 to 127)
S8 to S18: Programmable counter divide ratio setting bit. (16 to 2047)
C: Control bit (sets as low level).
Data is input from MSB side.

3. SERIAL DATA INPUT TIMING



NOTES: Parenthesis data is used for setting divide ratio of programmable reference divider.
On rising edge of clock shifts one bit of data in the shift register.

4. PHASE CHARACTERISTICS

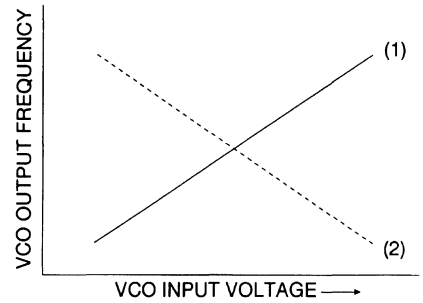
FC pin is provided to change phase characteristics of phase comparator. Characteristics of internal charge pump output level (D_O), phase comparator output level (ØR, ØP) are reversed depending upon FC pin input level. Also, monitor pin (f_{OUT}) output level of phase comparator is controlled by FC pin input level. The relation between outputs (D_O, ØR, ØP) and FC input level are shown below.

	FC: "H" or open				FC: "L"			
	D_O	ØR	ØP	f_{OUT}	D_O	ØR	ØP	f_{OUT}
fr > fp	H	L	L	(fr)	L	H	Z	(fp)
fr = fp	Z	L	Z	(fr)	Z	L	Z	(fp)
fr < fp	L	H	Z	(fr)	H	L	L	(fp)

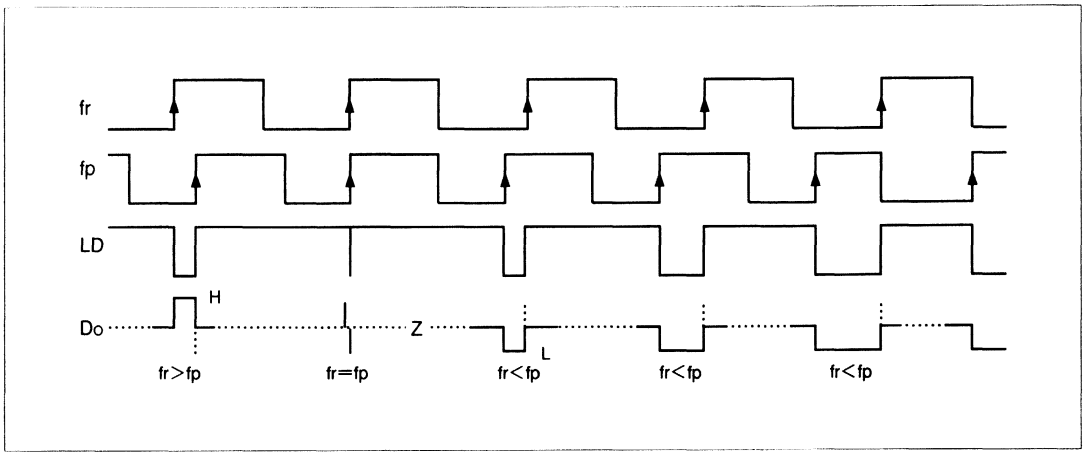
NOTE: Z = (High impedance)

Depending upon VCO characteristics, FC pin should be set accordingly:

- When VCO characteristics are like (1), FC should be set High or open circuit; When VCO characteristics are like (2), FC should be set Low.



Phase comparator output waveforms are shown below.



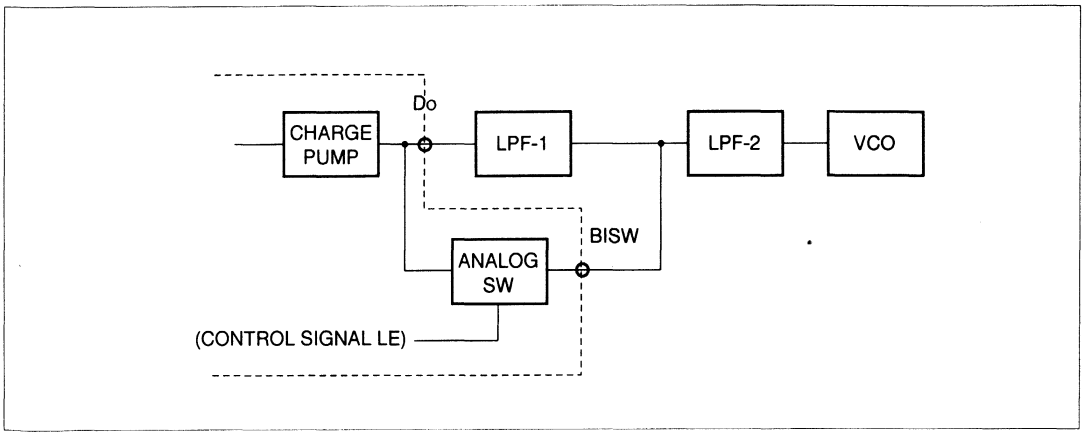
NOTES: Phase difference detection range: -2π to $+2\pi$
Spike appearance depends on charge pump characteristics. Also, the spike is output in order to diminish dead band.
When fr>fp or fr<fp, spike might not appear depending upon charge rump characteristics.

5. ANALOG SWITCH

ON/OFF of analog switch is controlled by LE input signal. When the analog switch is ON, internal charge pump output (Do) is connected to BISW pin. When the analog switch is OFF, BISW pin is set to high-impedance state.

LE	Analog Switch
H (Changing the divide ratio of internal prescaler)	ON
L (Normal operating mode)	OFF

When an analog switch is inserted between LP1 and LP2, faster lock up times is achieved to reduce LPF time constant during PLL channal switching.



■ ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5 to +7.0	V
	V_P	V_{CC} to 10.0	V
Output Voltage	V_{OUT}	–0.5 to V_{CC}+0.5	V
Open-drain Voltage	V_{OOP}	–0.5 to 8.0	V
Output Current	I_{OUT}	±10	mA
Storage Temperature	Tstg	–55 to +125	°C

NOTE: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	2.7	3.0	5.5	V
	V_P	V_{CC}	—	8.0	V
Input Voltage	V_{IN}	GND	—	V_{CC}	V
Operating Temperature	Ta	–40	—	+85	°C

HANDLING PRECAUTIONS

- This device should be transported and stored in anti-static containers.
- This is static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover workbenches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handing or transporting PC boards with devices.

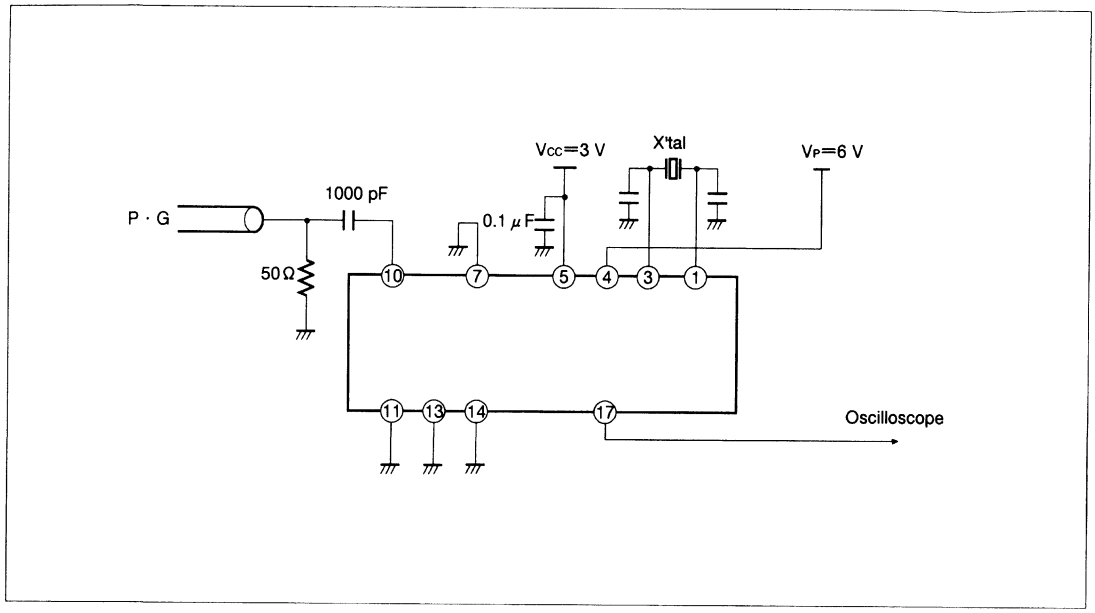
■ ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.7 V to 5.5 V, Ta = −40°C to +85°C)

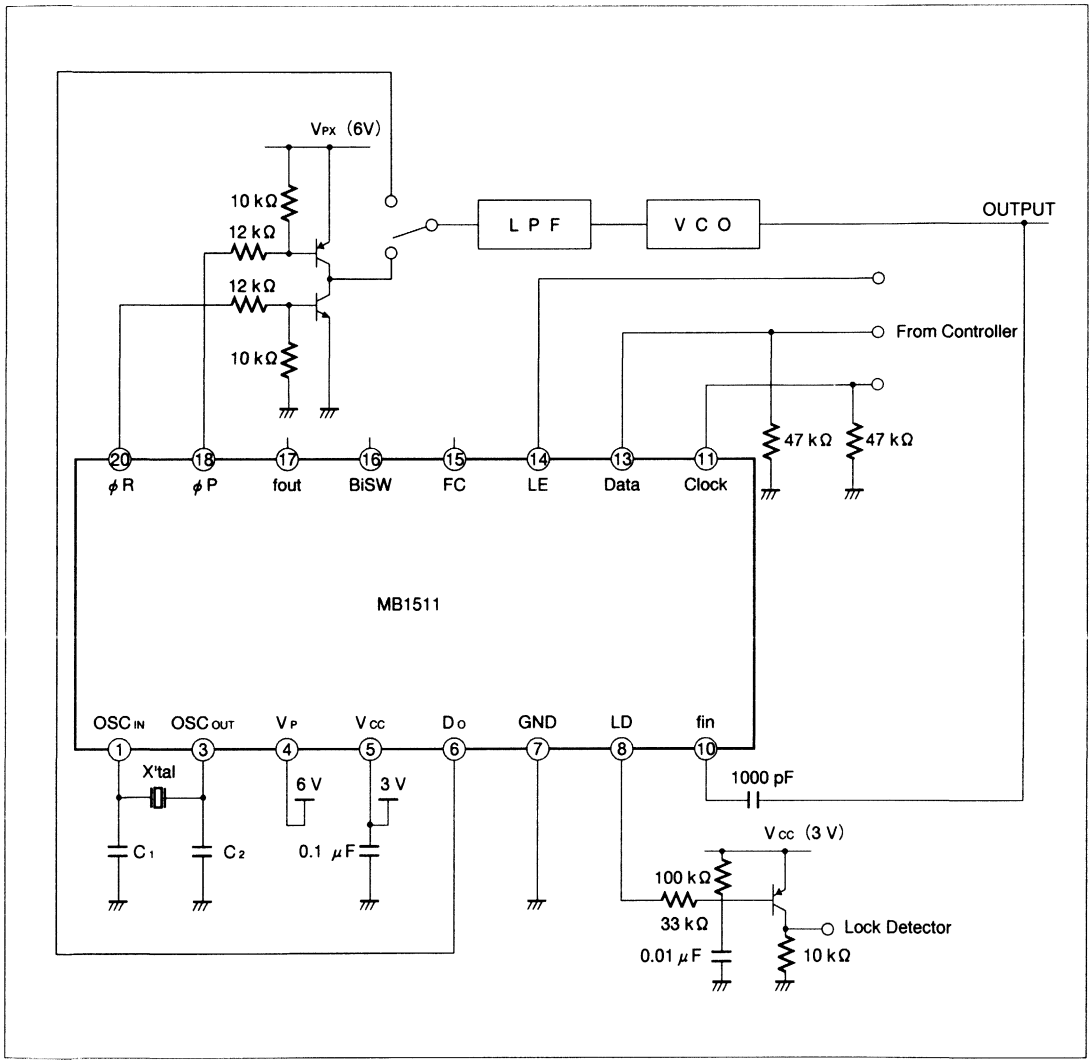
Parameter		Symbol	Value			Unit
			Min	Typ	Max	
Power Supply Current*1		I_{CC}	—	7.0	—	mA
Operating Frequency	fin*2	f_{IN}	10	—	1100	MHz
	OSC_{IN}	fosc	—	12	20	MHz
Input Sensitivity	fin-1*3	V_{fin1}	−4	—	6	dBm
	fin-2*4	V_{fin2}	−10	—	6	dBm
	OSC_{IN}	V_{OSC}	0.5	—	—	V_{p-p}
High-level Input Voltage	Except fin and OSC_{IN}	V_{IH}	Vcc×0.7	—	—	V
Low-level Input Voltage		V_{IL}	—	—	Vcc×0.3	V
High-level Input Current	Data clock	I_{IH}	—	1.0	—	µA
Low-level Input Current		I_{IL}	—	−1.0	—	µA
Input Current	OSC_{IN}	I_{OSC}	—	±50	—	µA
	LE, FC	I_{LE}	—	−60	—	µA
High-level Output Current	Except Do and OSC_{OUT}	V_{OH}*5	2.2	—	—	V
Low-level Output Current		V_{OL}	—	—	0.4	V
N-channel Open Drain Cutoff Current	Do, ØP*6	I_{OFF}	—	—	1.1	µA
Output Current	Except Do and OSC_{OUT}	I_{OH}	−1.0	—	—	mA
		I_{OL}	1.0	—	—	mA
Analog Switch on Resistance		R_{ON}	—	50	—	Ω

*1: f_{in} =1.1 GHz, OSC_{IN}=12 MHz, V_{CC}=3V. Inputs are grounded and outputs are open.
*2: AC coupling. Minimum operating frequency is measured when a capacitor 1000pF.
*3: V_{CC}=4.0 to 5.5V, 50Ω
*4: V_{CC}=2.7 to 4.0V, 50Ω
*5: V_{CC}=3V
*6: V_P=V_{CC} to 8V, V_{OOP}=GND to 8V

■ MEASUREMENT CIRCUIT



■ TYPICAL APPLICATION EXAMPLE



VPX, VP : 8V max.

C1, C2 : Depends on crystal oscillator

LE, FC : With internal pull up resistor

φP : Open drain output

MEMO

FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-21312-1E

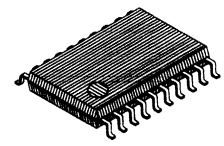
ASSP
SERIAL INPUT PLL FREQUENCY SYNTHESIZER

MB1512

LOW POWER SERIAL INPUT PLL SYNTHESIZER WITH 1.1GHz PRESCALER

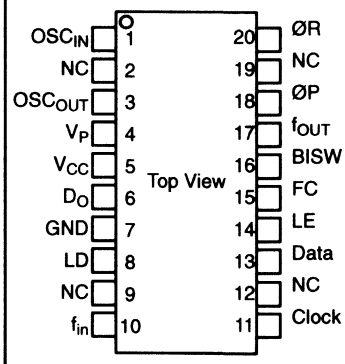
The Fujitsu MB1512, utilizing BI-CMOS technology, is a single chip serial input PLL synthesizer with pulse-swallow function.
The MB1512 contains a 1.1 GHz two modulus prescaler that can select of either 64/65 or 128/129 divide ratio, control signal generator, 16-bit shift register, 15-bit latch, programmable reference divider (binary 14-bit programmable reference counter), 1-bit switch counter, phase comparator with phase conversion function, charge pump, crystal oscillator, 19-bit shift register, 18-bit latch, programmable divider (binary 7-bit swallow counter and binary 11-bit programmable counter) and analog switch to speed up lock up time.
It operates supply voltage of 5V typ. and achieves very low supply current of 8mA typ. realized through the use of Fujitsu Advanced Process Technology.

- High operating frequency: $f_{IN\ MAX}$=1.1GHz ($V_{IN\ MIN}$=−10dBm)
- Pulse swallow function: 64/65 or 128/129
- Power supply voltage: V_{CC}=4.5 to 5.5V
- Low supply current: I_{CC}=8mA typ.
- Serial input 18-bit programmable divider consisting of:
  - Binary 7-bit swallow counter: 0 to 127
  - Binary 11-bit programmable counter: 16 to 2047
- Serial input 15-bit programmable reference divider consisting of:
  - Binary 14-bit programmable reference counter: 8 to 16383
  - 1-bit switch counter (SW) sets divide ratio of prescaler
- On-chip analog switch achieves fast lock up time
- 2types of phase detector output
  - On-chip charge pump (Bipolar type)
  - Output for external charge pump
- Wide operating temperature: −40°C to +85°C
- 20-pin Plastic Shrink Small Outline Package



PLASTIC PACKAGE
FPT-20P-M03

PIN ASSIGNMENT



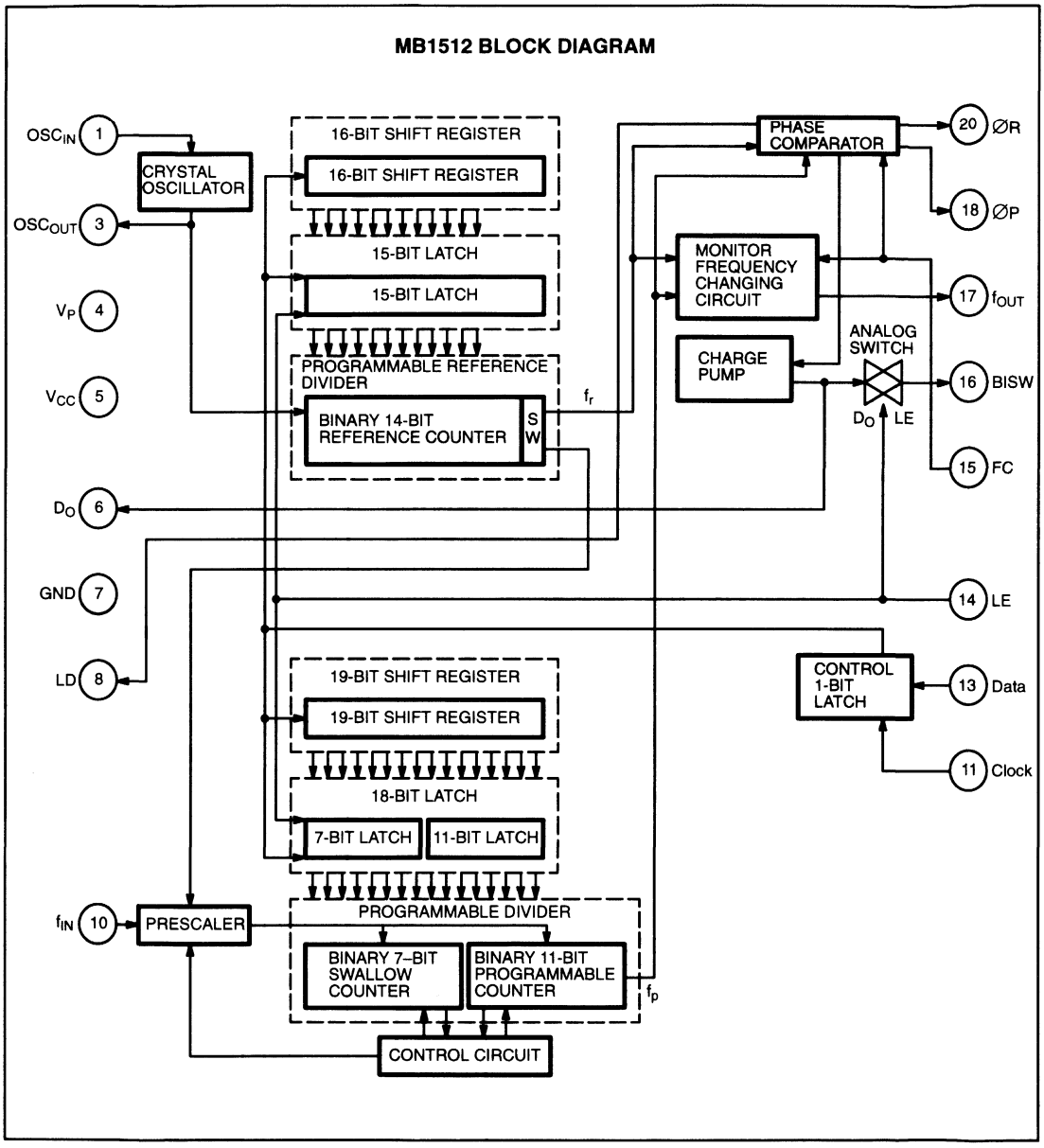
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
	V_P	V_{CC} to 10.0	V
Output Voltage	V_{OUT}	−0.5 to V_{CC} +0.5	V
Open-drain Voltage	V_{OOP}	−0.5 to 0.8	V
Output Current	I_{OUT}	±10	mA
Storage Temperature	T_{STG}	−55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MB1512 BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Pin Name	I/O	Description
1 3	OSC_{IN} OSC_{OUT}	I O	Oscillator input. Oscillator output. A crystal is placed between OSC_{IN} and OSC_{OUT}.
4	V_P	–	Power supply input for charge pump and analog switch.
5	V_{CC}	–	Power supply voltage input.
6	D_O	O	Charge pump output. The characteristics of charge pump is reversed depending upon FC input.
7	GND	–	Ground.
8	LD	O	Phase comparator output. Normally this pin outputs high level. While the phase difference of f_r and f_p exists, this pin outputs low level.
9	NC	–	No connection.
10	f_{IN}	I	Prescaler input. The connection with an external VCO should be AC connection.
11	Clock	I	Clock input for 19-bit shift register and 16-bit shift register. On rising edge of the clock shifts one bit of data into the shift registers.
12	NC	–	No connection.
13	Data	I	Binary serial data input. The last bit of the data is a control bit which specified destination of shift registers. When this bit is high level and LE is high level, the data stored in shift register is transferred to 15-bit latch. When this bit is low level and LE is high level, the data is transferred to 18-bit latch.
14	LE	I	Load enable input (with internal pull up resistor). When LE is high or open, the data stored in shift register is transferred into latch depending upon the control bit. At the time, internal charge pump output to be connected to BISW pin because internal analog switch becomes ON state.
15	FC	I	Phse select input of phase comparator (with internal pull up resistor). When FC is low level, the characteristics of charge pump, phase comparator is reversed. FC input signal is also used to control f_{out} pin (test pin) output level, f_r or f_p.
16	BISW	O	Analog switch output. Usually BISW pin is set high-impedance state. When internal analog switch is ON (LE pin is high level), this pin outputs internal charge pump state.
17	f_{OUT}	O	Minitor pin of phase comparator input. f_{out} pin outputs either programmable reference divider output (f_r) or programmable divider output (f_p) depending upon FC pin input level. FC=H: It is the same as f_r output level. FC=L: It is the same as f_p output level.
18 20	ØP ØR	O O	Outputs for external charge pump. The characteristics are reversed according to FC input. ØP pin is N-channel open drain output.
2 19	NC	–	No connection.

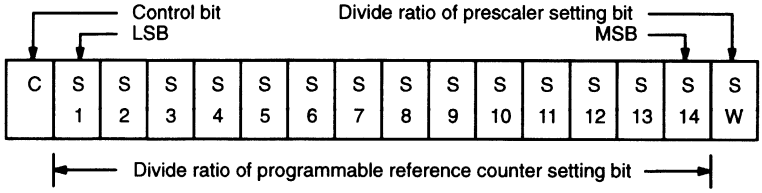
FUNCTIONAL DESCRIPTIONS

SERIAL DATA INPUT

Serial data input is achieved by three inputs, such as Data pin, Clock pin and LE pin. Serial data input controls 15-bit programmable reference divider and 18-bit programmable divider, respectively.
Binary serial data is input to Data pin.
On rising edge of clock shifts one bit of serial data into the internal shift registers and when load enable pin is high level or open, stored data is transferred into latch depending upon the control bit.
Control data "H" data is transferred into 15-bit latch.
Control data "L" data is transferred into 18-bit latch.

PROGRAMMABLE REFERENCE DIVIDER

Programmable reference divider consists of 16-bit shift register, 15-bit latch and 14-bit reference counter. Serial 16-bit data format is shown below.



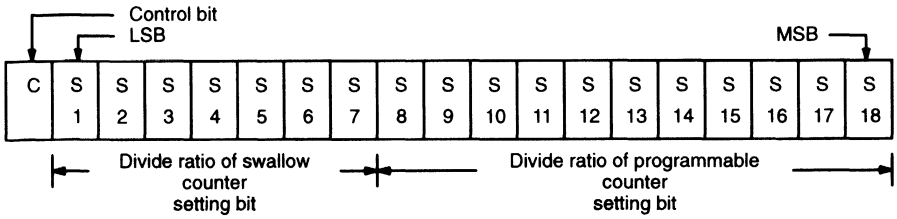
14-BIT PROGRAMMABLE REFERENCE COUNTER DIVIDE RATIO

Divide Ratio R	S 14	S 13	S 12	S 11	S 10	S 9	S 8	S 7	S 6	S 5	S 4	S 3	S 2	S 1
8	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	1	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

NOTES: Divide ratio less than 8 is prohibited.
Divide ratio: 8 to 16383
SW: This bit selects divide ratio of prescaler.
SW=H : 64/65
SW=L : 128/129
S1 to S14: These bits select divide ratio of programmable reference divider.
C: Control bit (sets as high level).
Data is input from MSB side.

PROGRAMMABLE DIVIDER

Programmable divider consists of 19-bit shift register, 18-bit latch, 7-bit swallow counter and 11-bit programmable counter. Serial 19-bit data format is shown following page.



7-BIT SWALLOW COUNTER DIVIDE RATIO

Divide Ratio A	S 7	S 6	S 5	S 4	S 3	S 2	S 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

NOTE: Divide ratio: 0 to 127

11-BIT PROGRAMMABLE COUNTER DIVIDE RATIO

Divide Ratio N	S 18	S 17	S 16	S 15	S 14	S 13	S 12	S 11	S 10	S 9	S 8
16	0	0	0	0	0	0	1	0	0	0	Ø
17	0	0	0	0	0	0	1	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

NOTES: Divide ratio less than 16 is prohibited.
Divide ratio: 16 to 2047
S1 to S7: Swallow counter divide ratio setting bit. (0 to 127)
S8 to S18: Programmable counter divide ratio setting bit. (16 to 2047)
C: Control bit (sets as low level).
Data is input from MSB side.

PULSE SWALLOW FUNCTION

$f_{VCO} = [(P \times N) + A] \times f_{OSC} \div R$

f_{VCO}: Output frequency of external voltage controlled oscillator (VCO)

N: Preset divide ratio of binary 11-bit programmable counter (16 to 2047)

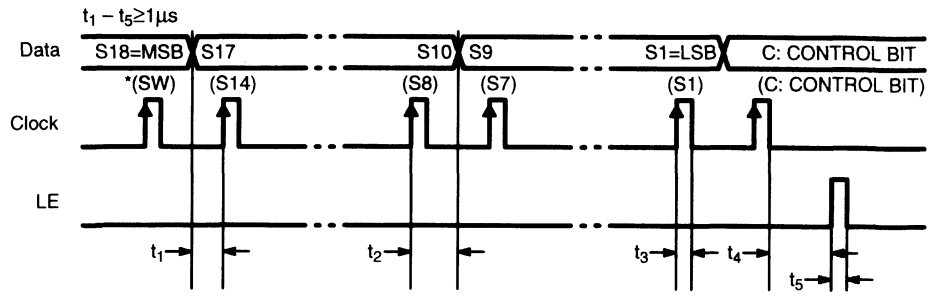
A: Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$, $A < N$)

f_{OSC}: Output frequency of the external reference frequency oscillator

R: Preset divide ratio of binary 14-bit programmable reference counter (8 to16383)

P: Preset modulus of external dual modulus prescaler (64 or 128)

SERIAL DATA INPUT TIMING



NOTES: Parenthesis data is used for setting divide ratio of programmable reference divider.
On rising edge of clock shifts one bit of data in the shift register.

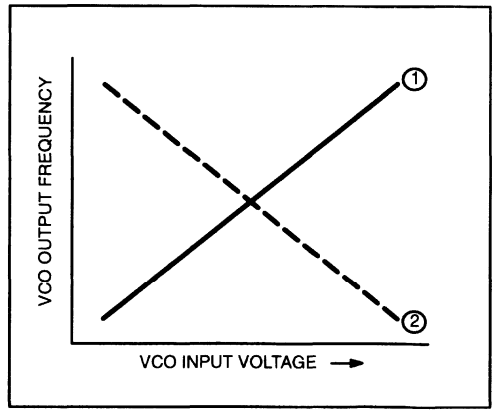
PHASE CHARACTERISTICS

FC pin is provided to change phase characteristics of phase comparator. Characteristics of internal charge pump output level (D_O), phase comparator output level (ØR, ØP) are reversed depending upon FC pin input level. Also, monitor pin (f_{out}) output level of phase comparator is controlled by FC pin input level. The relation between outputs (D_O, ØR, ØP) and FC input level are shown below.

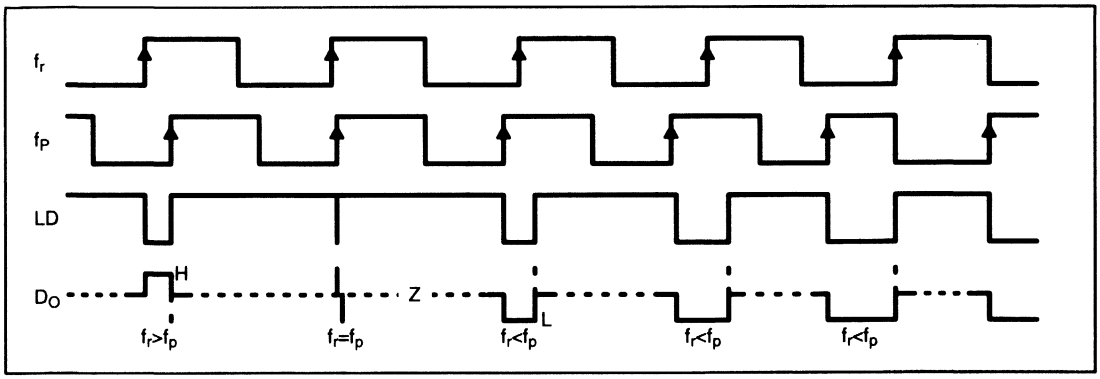
	FC=H or open				FC=L			
	D_O	ØR	ØP	f_{out}	D_O	ØR	ØP	f_{out}
$f_r > f_p$	H	L	L	(f_r)	L	H	Z	(f_p)
$f_r < f_p$	L	H	Z	(f_r)	H	L	L	(f_p)
$f_r = f_p$	Z	L	Z	(f_r)	Z	L	Z	(f_p)

Note: Z=(High impedance)

VCO CHARACTERISTICS



Depending upon VCO characteristics, FC pin should be set accordingly:
When VCO characteristics are like ①, FC should be set high or open circuit;
When VCO characteristics are like ②, FC should be set Low.



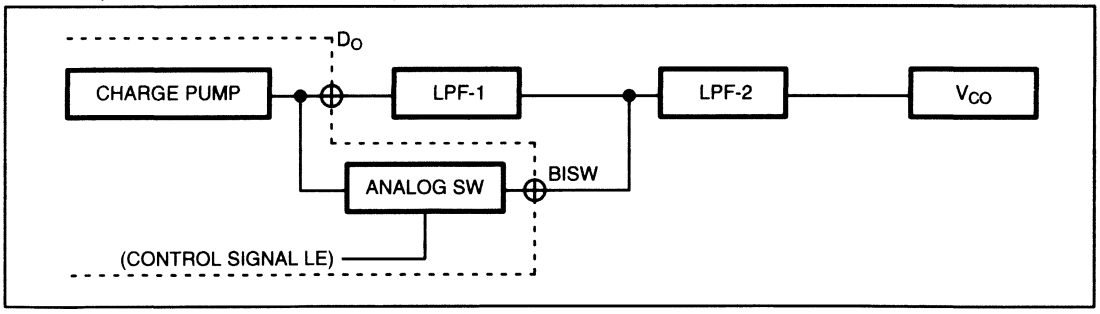
NOTES: Phase difference detection range: -2π to $+2\pi$
Spike appearance depends on charge pump characteristics. Also, the spike is output in order to diminish dead band.
When $f_r>f_p$ or $f_r<f_p$, spike might not appear depending upon charge pump characteristics.

ANALOG SWITCH

ON/OFF of analog switch is controlled by LE input signal. When the analog switch is ON, internal charge pump output (D_O) to be connected to BISW pin. When the analog switch is OFF, BISW pin is set to high-impedance state.

LE=H (Changing the divide ratio of internal prescaler) : Analog switch=ON
LE=L (Normal operating mode) : Analog switch=OFF

LPF time constant is decreased in order to insert a analog switch between LPF1 and LPF2 when channel of PLL is changing. Thus, lock up time is decreased, that is, fast lock up time is achieved.



RECOMMENDED OPERATING CONDITIONS

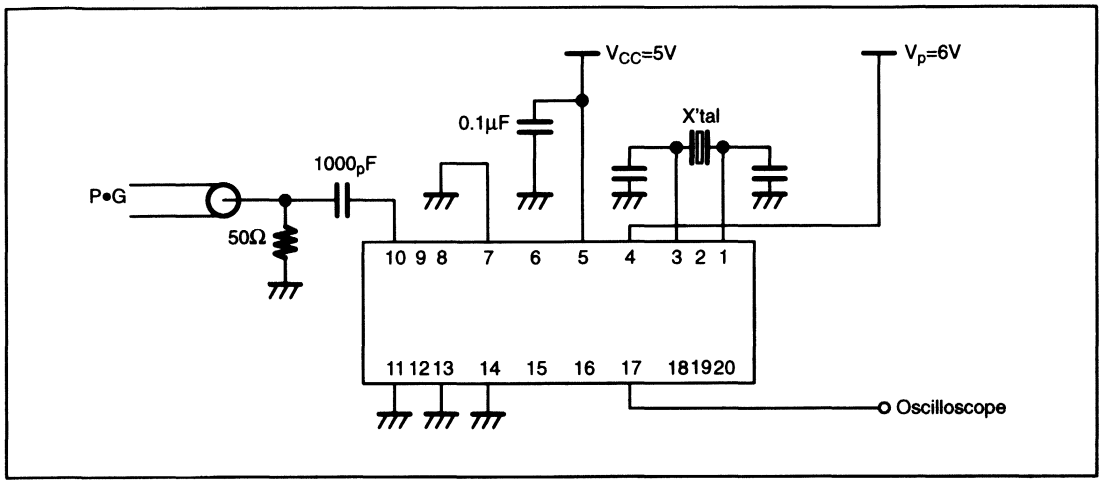
Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_P	V_{CC}	–	8.0	V
Input Voltage	V_I	GND	–	V_{CC}	V
Operating Temperature	T_A	–40	–	+85	°C

ELECTRICAL CHARACTERISTICS

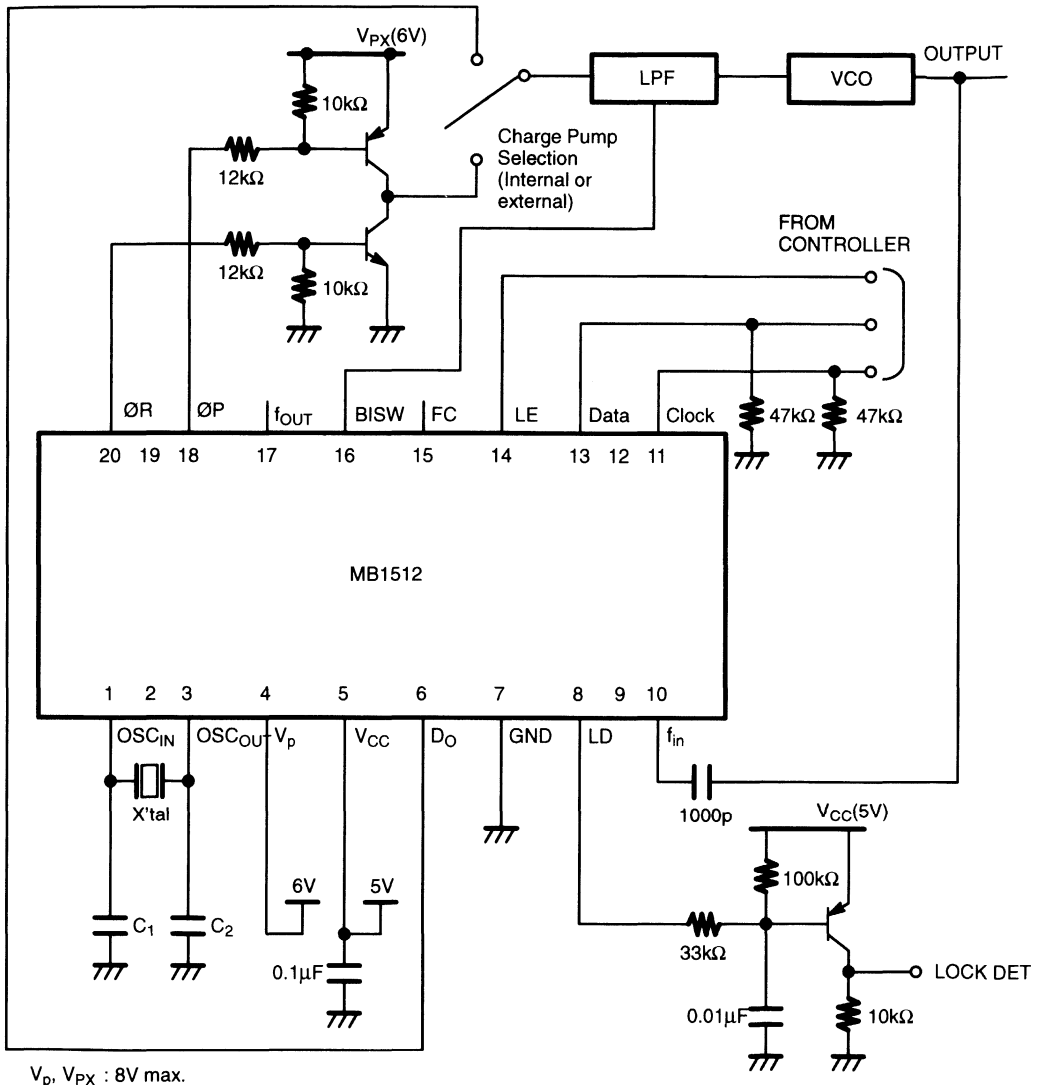
Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Power Supply Current		I_{CC}	Note 1	–	8.0	12.0	mA
Operating Frequency	f_{in}	f_{in}	Note 2	10	–	1100	MHz
	OSC_{IN}	f_{OSC}		–	12	20	MHz
Input Sensitivity	f_{in}	Vf_{in}		–10	–	6	dBm
	OSC_{IN}	V_{OSC}		0.5	–	–	V_{PP}
High-level Input Voltage	Except f_{in} and OSC_{IN}	V_{IH}		V_{CC}x0.7	–	–	V
Low-level Input Voltage		V_{IL}		–	–	V_{CC}x0.3	V
High-level Input Current	Data Clock	I_{IH}		–	1.0	–	µA
Low-level Input Current		I_{IL}		–	–1.0	–	µA
Input Current	OSC_{IN}	I_{OSC}		–	±50	–	µA
	LE, FC	I_{LE}		–	–60	–	µA
High-level Output Current	Except D_O and OSC_{OUT}	V_{OH}	V_{CC}=5V	4.4	–	–	V
Low-level Output Current		V_{OL}		–	–	0.4	V
N-channel Open Drain Cutoff Current	D_O, ØP	I_{OFF}	$V_{CC} \leq V_P \leq 8V$	–	–	1.1	µA
Output Current	Except D_O and OSC_{OUT}	I_{OH}		–1.0	–	–	mA
		I_{OL}		1.0	–	–	mA
Analog Switch On Resistor		R_{ON}		–	25	–	Ω

NOTE 1: f_{in}=1.1GHz, OSC_{IN}=12MHz, V_{CC}=5V. Inputs are grounded and outputs are open.
NOTE 2: AC coupling. Minimum operating frequency is measured when a capacitor 1000pF is connected.

TEST CIRCUIT



TYPICAL APPLICATION EXAMPLE



V_p, V_{PX} : 8V max.
C_1, C_2 : Depends on crystal oscillator
LE,FC : With internal pull up resistor
ØP : Open drain output

FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-21316-1E

ASSP

SERIAL INPUT PLL FREQUENCY SYNTHESIZER

MB1513

SERIAL INPUT PLL FREQUENCY SYNTHESIZER WITH POWER SAVING FUNCTIONS (1.1GHz)

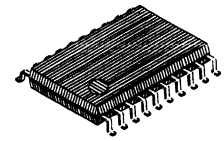
The Fujitsu MB1513 is a serial input phase-locked loop (PLL) frequency synthesizer with a pulse-swallow function. A stand-by mode is provided to limit power consumption during intermittent operation.

The MB1513 is configured of a 1.1 GHz dual-modules prescaler with selectable 128/129 divide ratio, a control signal generator, a 16-bit shift register, a 15-bit latch, a programmable reference divider (binary 14-bit programmable reference counter), a 1-bit switch counter, a phase comparator with phase conversion function, a charge pump, a crystal oscillator, a 19-bit shift register, an 18-bit latch, a programmable divider (binary 7-bit swallow counter and binary 11-bit programmable counter), analog switches, and an intermittent operation control circuit that selects the stand-by or operating mode depending on the power-save control input state (PS).

The MB1513 operates from a single +5 V supply. Fujitsu's advanced process technology achieves an I_{CC} of 8 mA, typical. The stand-by mode current consumption is just 100 µA.

FEATURES

- High operating frequency : f_{IN} = 1.1 GHz (V_{IN} = -10 dBm)
- Pulse-swallow function : High-speed dual-modules prescaler with selectable 128/129 divider ratio
- Low supply current : I_{CC} = 8 mA typ. at 5 V
- Power-saving stand-by mode:100 µA typ.
- Serial input, 18-bit programmable divider consisting of:
  Binary 7-bit swallow counter :0 to 127
  Binary 11-bit programmable counter :16 to 2,047
- Serial input 15-bit programmable reference divider consisting of:
  Binary 14-bit programmable reference counter: 8 to 16,383
  1-bit switch counter sets prescaler divide ratio
- On-chip analog switch for fast lockup
- On-chip charge pump minimizes system component count
- Wide operating temperature range: -40 to +85C°
- Plastic 20-pin shrink small outline package (Suffix: PFV)

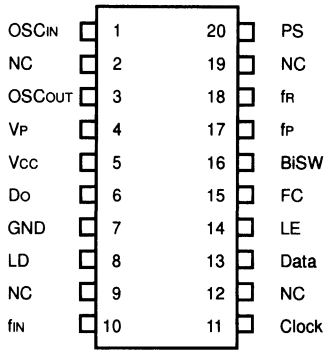


PLASTIC PACKAGE
(FPT-20P-M03)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

PIN ASSIGNMENT

(TOP VIEW)

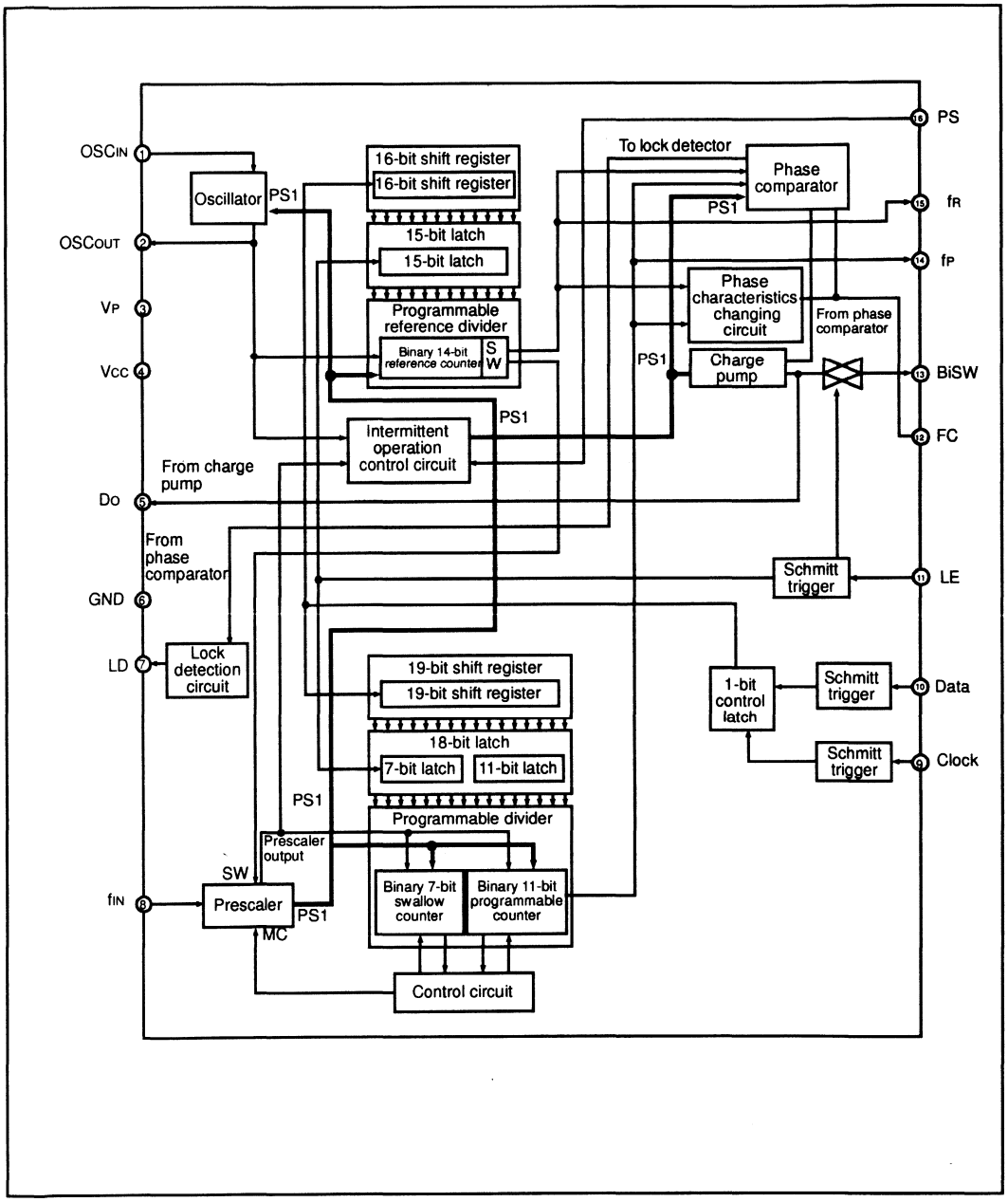


ABSOSUTE MAXIMUM RATINGS (See NOTE)

Ratings	Symbol	Value	Unit
Supply voltage	V_{CC}	-0.5 to +7.0	V
	V_P	$V_{CC} \leq V_P \leq 10.0$	V
Output voltage	V_O	-0.5 to V_{CC} +0.5	V
Output current	I_O	±10	mA
Storage temperature	Tstg	-55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ BLOCK DIAGRAM



■ PIN DESCRIPTION

Pin No.	Pin name	I/O	Description
1	OSC_{IN}	I	Programmable reference divider input Oscillator input An external crystal is connected to this pin
2	NC	-	No connection
3	OSC_{OUT}	O	Oscillator output An external is connected to this pin
4	V_P	-	Power supply input for charge pump and analog switch
5	V_{CC}	-	Power supply
6	D_O	O	Charge pump output The phase of charge pump is reversed depending on FC input
7	GND	-	Ground
8	LD	O	Phase comparator output The output level is high when LD is locked. The output level is low when LD is unlocked
9	NC	-	No connection
10	f_{IN}	I	Prescaler input An external VCO is AC-coupled to this pin
11	Clock	I	Clock input for 19-bit and 16-bit shift registers One bit of data is shifted into the registers on the rising edge of the clock Schmitt trigger circuit is involved
12	NC	-	No connection
13	Data	I	Binary serial data input The last bit of the data is a control bit When the control bit is high, data is transmitted to the 15-bit latch When the control bit is low, data is transmitted to the 18-bit latch Schmitt trigger circuit is involved
14	LE	I	Load enable signal input When LE is high, the contents of the shift register are transferred to a latch, depending on the control bit in the serial data. At the same time, an internal analog switch turns on and the output of the internal charge pump is connected to the BiSW pin Schmitt trigger circuit is involved
15	FC	I	Phase select input of phase comparator (with internal pull-up resistor) When FC is low, the characteristics of charge pump and phase comparator are reversed FC input signal is also used to control the fout pin (test pin) of f_R or f_P
16	BiSW	O	Analog switch output Usually, BiSW is in the high-impedance state. When the switch is on (LE is high), the charge pump is connected to the BiSW pin
17	f_P	O	Programmable cunter output monitor pin
18	f_R	O	Reference counter output monitor pin
19	NC	-	No connection
20	PS	I	Power save signal input Set low when the system is operating (Never use pin 20 as it is opened) PS = High: Operation mode PS = Low: Stand-by mode

■ FUNCTION DESCRIPTIONS

Pulse swallow function

The divide ratio can be calculated using the following equation:

$fvco = [(M \times N) + A] \times fosc \div R \quad (A < N)$

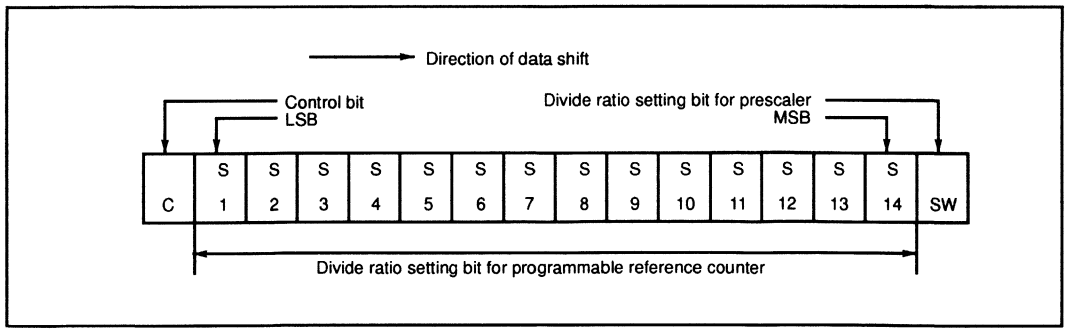
- fvco : Output frequency of external voltage controlled oscillator (VCO)
- N : Preset divide ratio of binary 11-bit programmable counter (16 to 2,047)
- A : Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$)
- fosc : Output frequency of the reference frequency oscillator
- R : Preset divide ratio of binary 14-bit programmable reference counter (8 to 16,383)
- M : Preset divide ratio of prescaler (128)

Serial data input

Serial data is input using the Data, Clock, and LE pins. Serial data controls the 15-bit programmable reference divider and 18-bit programmable divider separately.
Binary serial data is input to the Data pin.
One bit of data is shifted into the internal shift registers on the rising edge of the clock. When the load enable pin is high or open, stored data is latched, depending on the control as follows:

Control data	Destination of serial data
H	15 bit latch
L	18 bit latch

(a) Programmable reference divider ratio
The programmable reference divider consists of a 15-bit latch and a 14-bit reference counter. The 16-bit serial data format is shown below:



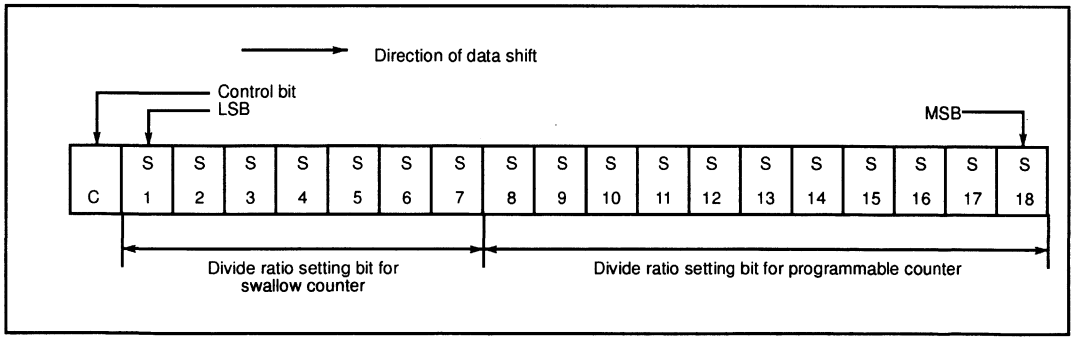
- 14-bit programmable reference counter divide ratio

Divide ratio R	S 14	S 13	S 12	S 11	S 10	S 9	S 8	S 7	S 6	S 5	S 4	S 3	S 2	S 1
8	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	1	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

(Divide ratio = 8 to 16,383)

Notes: 1. Divide ratios less than 8 are prohibited.
2. SW: This bit selects the divide ratio of the prescaler
   SW Low: 128 or 129
   (SW must be always be low.)
3. S1 to S14: These bits select the divide ratio of the programmable reference counter (8 to 16,383).
4. C: Control bit: Set high.
5. Input data MSB first.

(b) Programmable divider divide ratio
The programmable divider consists of a 19-bit shift register, an 18-bit latch, a 7-bit swallow counter, and an 11-bit programmable counter. The 19-bit serial data format is shown below:



• 7-bit swallow counter divide ratiow

Divide ratio A	S 7	S 6	S 5	S 4	S 3	S 2	S 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

(Divide ratio = 0 to 127)

• 11-bit programmable counter divide ratio

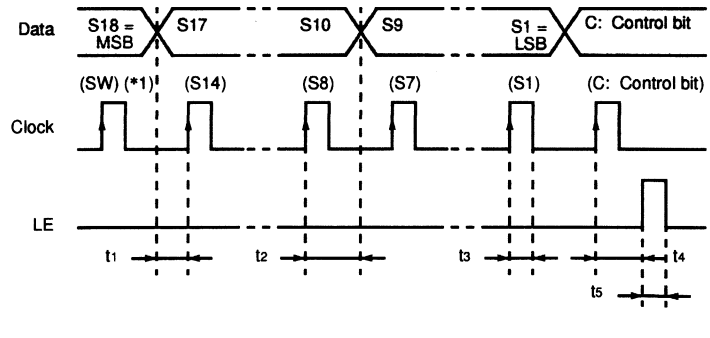
Divide ratio N	S 18	S 17	S 16	S 15	S 14	S 13	S 12	S 11	S 10	S 9	S 8
16	0	0	0	0	0	0	1	0	0	0	0
17	0	0	0	0	0	0	1	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

(Divide ratio = 16 to 2,047)

Notes: 1. Divide ratio less than 16 are prohibited for 11-bit programmable counter.
2. S1 to S7: These bits select the divide ratio of swallow counter (0 to 127).
3. S8 to S18: These bits select the divide ratio of programmable counter (16 to 2,047).
4. C: Control bit: (Set low)
5. Input data MSB first.

Serial data input timing

• t_1 (≥ 1µs) : Data setup time t_2 (≥ 1µs) : Data hold time t_3 (≥ 1µs) : Clock pulse width
t_4 (≥ 1µs) : LE setup time to the rising edge of last clock t_5 (≥ 1µs) : LE pulse width



*1 : Bits enclosed in parentheses are used when the divide ratio of the programmable reference divider is selected.

Note: One bit of data is shifted into the shift register on the rising edge of the clock.

Intermittent operation

Intermittent operation limits power consumption by shutting down or start the internal circuits according to its necessity. If device operation resumes uncontrolled, the error signal output from the phase comparator may exceed the limit due to an undefined phase relationship between the reference frequency (f_R) and the comparison frequency (f_P) and frequency lock is lost.
To prevent this, an intermittent operation control circuit is provided to decrease the variation in the locking frequency by forcibly correcting phase of both frequencies to limit the error signal output. This is done by the PS control circuit. If PS is set high, the circuit enter the operating mode. If PS is set low, operation stops and the device enters the stand-by mode. Each mode is explained below:

- Operating mode (PS = High)
  All circuits are operating, and PLL operation is normal.

- Stand-by mode (PS = Low)
  Circuits that do not affect operation are powered-down to save power.
  The current in the power save state is typically 100 μA.
  At this time, the levels of D_O and LD are the same as when the PLL is locked.
  Since D_O is placed in the high-impedance state and the input voltage of the voltage-controlled oscillator (VCO) is set to the voltage in the operating mode (when locked) by the time constant of the low-pass filter, the frequency output from the VCO (f_{VCO}) is kept at the locking frequency.

The operating and stand-by modes alternate repeatedly. This intermittent operation limits the error signal by forcibly correcting the phase of the reference and comparison frequencies to limit power consumption.
The device must be set in the stand-by mode (PS = low) when it is powered up.

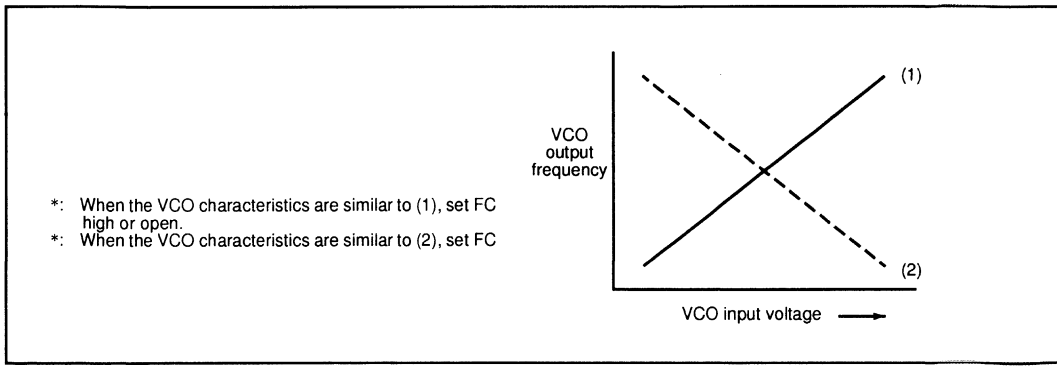
Relationship between FC input and phase characteristics

The FC pin controls the phase characteristics of the phase comparator. The internal charge pump output level (D_O) is reversed depending on the FC pin input level. The relationship between the FC input level and D_O is shown below:

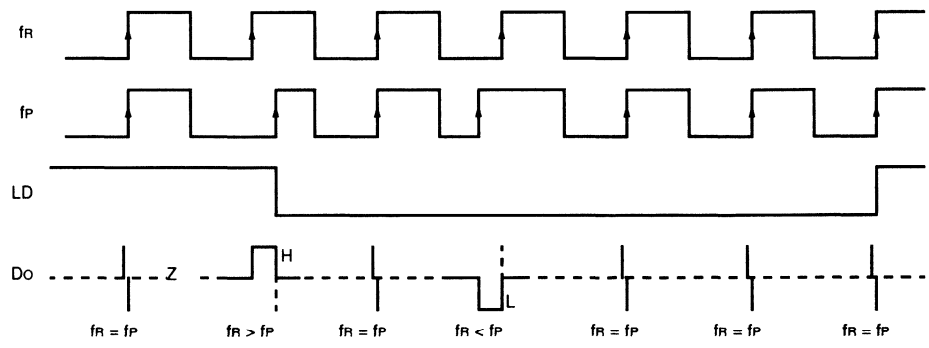
	FC = High or open	FC = Low
$f_R > f_P$	H	L
$f_R < f_P$	L	H
$f_R = f_P$	Z (*1)	Z (*1)

*1: High impedance

When designing a synthesizer, the FC pin setting depends on the VCO characteristics.



Phase comparator output waveform (FC = Hight)



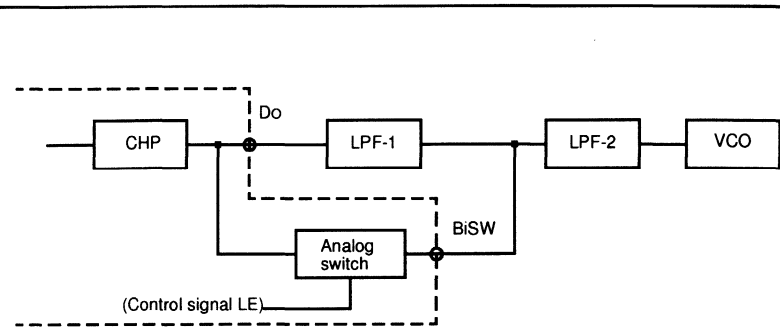
Notes:
1. Phase difference detection range: -2π to $+2\pi$
2. Spike appearance depends on the charge pump characteristics. The spike is output to diminish dead band.
3. When $f_R > f_P$ or $f_R < f_P$, spike might not appear, depending on the charge pump characteristics.
4. LD is low when the phase difference is tw or more. LD is high when the phase difference is tw or less for three or more continuous cycles (when f_{OSCIN} = 12.8 MHz, tw = 625 to 1,250 ns).

Analog switch

The LE signal turns the analog switch on or off. When the analog switch is turned on, the charge pump output (Do) is output through the BiSW pin. When it is turned off, the BiSW pin is in the high-impedance state.

When LE = high (when the divide ratio of the internal divider is changed): Analog switch = on
When LE = low (normal operating mode): Analog switch = off

The LPF time constant can be decreased by inserting an analog switch between LPF1 and LPF2. This decreases the lock-up time when the PLL channel is changed.



■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_P	$V_{CC} \leq V_P \leq 8.0$)			V
Input voltage	V_I	GND	-	V_{CC}	V
Operating temperature	T_A	-40	-	+85	°C

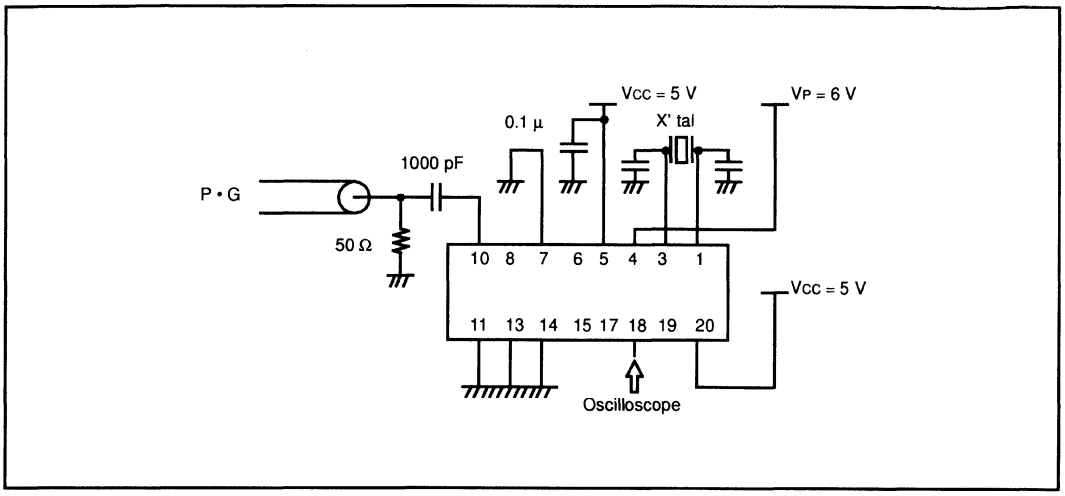
Notes: To protect against damage by electrostatic discharge, note the following handling precautions:

- Store and transport devices in conductive containers.
- Use properly grounded workstations, tools, and equipment.
- Turn off power before inserting or removing this device from a socket.
- When handling PC boards on which devices are mounted, protect leads of the device using conductive sheet.

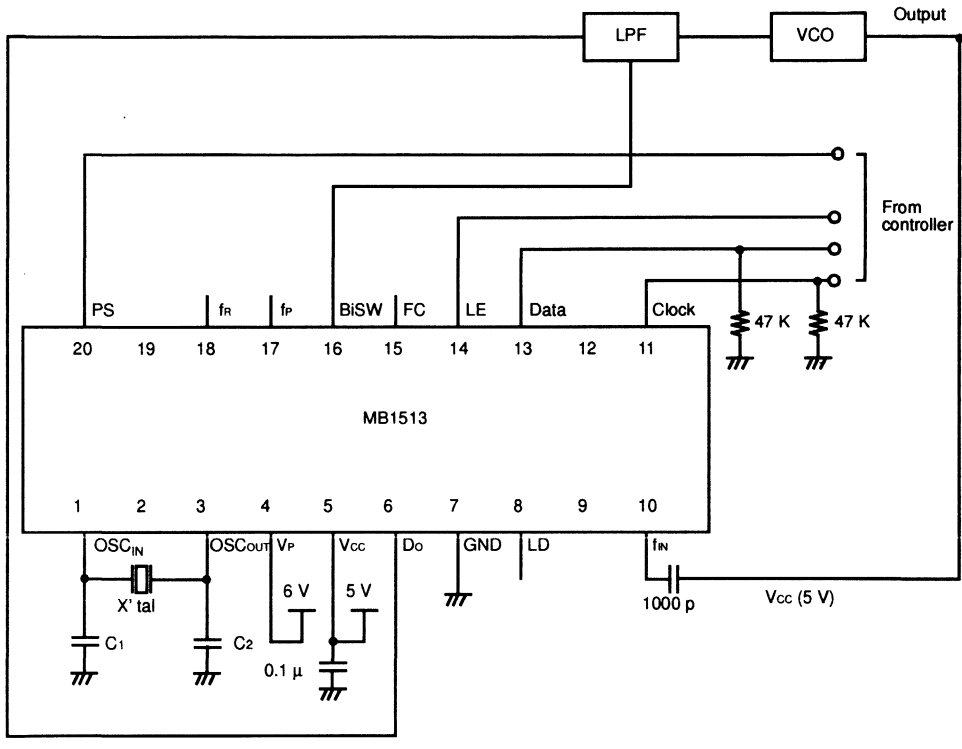
■ ELECTRICAL CHARACTERISTICS

Parameter		Symbol	Value			Unit	Conditions
			Min	Typ	Max		
Supply current		I_{CC}	-	8.0		mA	With f_{IN} = 1.1 GHz, OSC_{IN} = 12 MHz, V_{CC} = 5.0 V.
Stand-by current		IPS	-	100	-	µA	
Operating frequency	f_{IN}	f_{IN}	10	-	1100	MHz	AC coupling. The minimum operating frequency is measured with a 1000pF capacitor connected
	OSC_{IN}	f_{OSC}	-	12	20	MHz	
Input sensitivity	f_{IN}	$V_{f\,IN}$	-10	-	6	dBm	
	OSC_{IN}	V_{OSC}	0.5	-	-	Vp-p	
High-level input voltage	Except f_{IN} and OSC_{IN}	V_{IH}	V_{CC} × 0.7+0.4	-	-	V	
Low-level input voltage		V_{IL}	-	-	V_{CC} × 0.3-0.4	V	
High-level input current	Data Clock LE	I_{IH}	-	1.0	-	µA	
Low-level input current		I_{IL}	-	-1.0	-	µA	
	FC	I_{FC}	-	-60	-	µA	
Input current	OSC_{IN}	I_{OSC}	-	±50	-	µA	
High-level output voltage	Except D_O and OSC_{OUT}	V_{OH}	4.4	-	-	V	V_{CC} = 5 V
Low-level output voltage		V_{OL}	-	-	0.4	V	
High-impedance Cut off current	D_O	I_{OFF}	-	-	1.1	µA	V_{DO} = GND to 8 V $V_{CC} \leq V_P \leq 8$ V
Output current	Except D_O and OSC_{OUT}	I_{OH}	-1.0	-	-	mA	
		I_{OL}	1.0	-	-	mA	
Analog switch ON resistance		R_{ON}	-	25	-	Ω	

■ TEST CIRCUIT (FOR MEASURING PRESCALER INPUT SENSITIVITY)



■ APPLICATION EXAMPLE



V_P, V_{PX} : Maximum 8 V
C_1, C_2 : Depend on the crystal parameters

MEMO

FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-21329-2E

ASSP for DTS

Bi-CMOS

1.1 GHz PLL Frequency Synthesizer

MB15A03

■ DESCRIPTION

The MB15A03 is a PLL (phase locked loop) frequency synthesizer LSI operating at up to 1.1 GHz. It incorporates a dual-modulus prescaler allowing either of 64/65 and 128/129 frequency divisions to be selected. The LSI is configurable to serve as a PLL frequency synthesizer supporting a pulse swallow system.

The MB15A03 has a built-in power save function, achieving low power consumption.

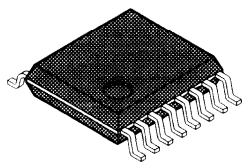
The MB15A03 best fits analog mobile telecommunications equipment.

■ FEATURES

- Operation at high speed: Up to 1.1 GHz
- Operation at low voltage: 2.7 to 3.6 V
- Low current consumption: Typical 6.5 mA (V_{CC} = 3 V)
- Built-in power save function: Typical 100 µA (V_{CC} = 3V)
- Dual-modulus prescaler divide ratio: 64/65 or 128/129
- Reference divider
  Binary 14-bit reference counter (divide ratio of 6 to 16,383)
- Comparative dividers
  Binary 7-bit swallow counter (divide ratio of 0 to 127)
  Binary 11-bit programmable counter (divide ratio of 5 to 2,047)
- Internal phase comparator with phase conversion features
- Internal digital lock detection circuit for PLL lock/unlock detection
- Operating temperature range: –40 to +85°C

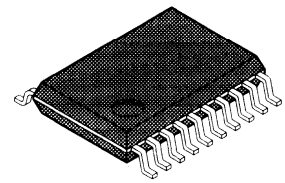
■ PACKAGES

16-pin Plastic SSOP



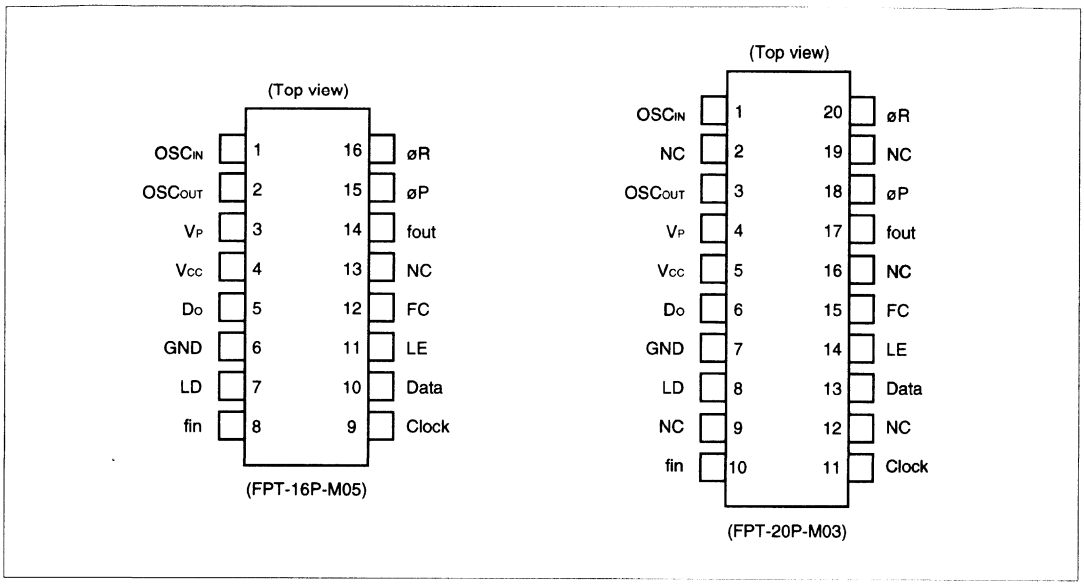
(FPT-16P-M05)

20-pin Plastic SSOP



(FPT-20P-M03)

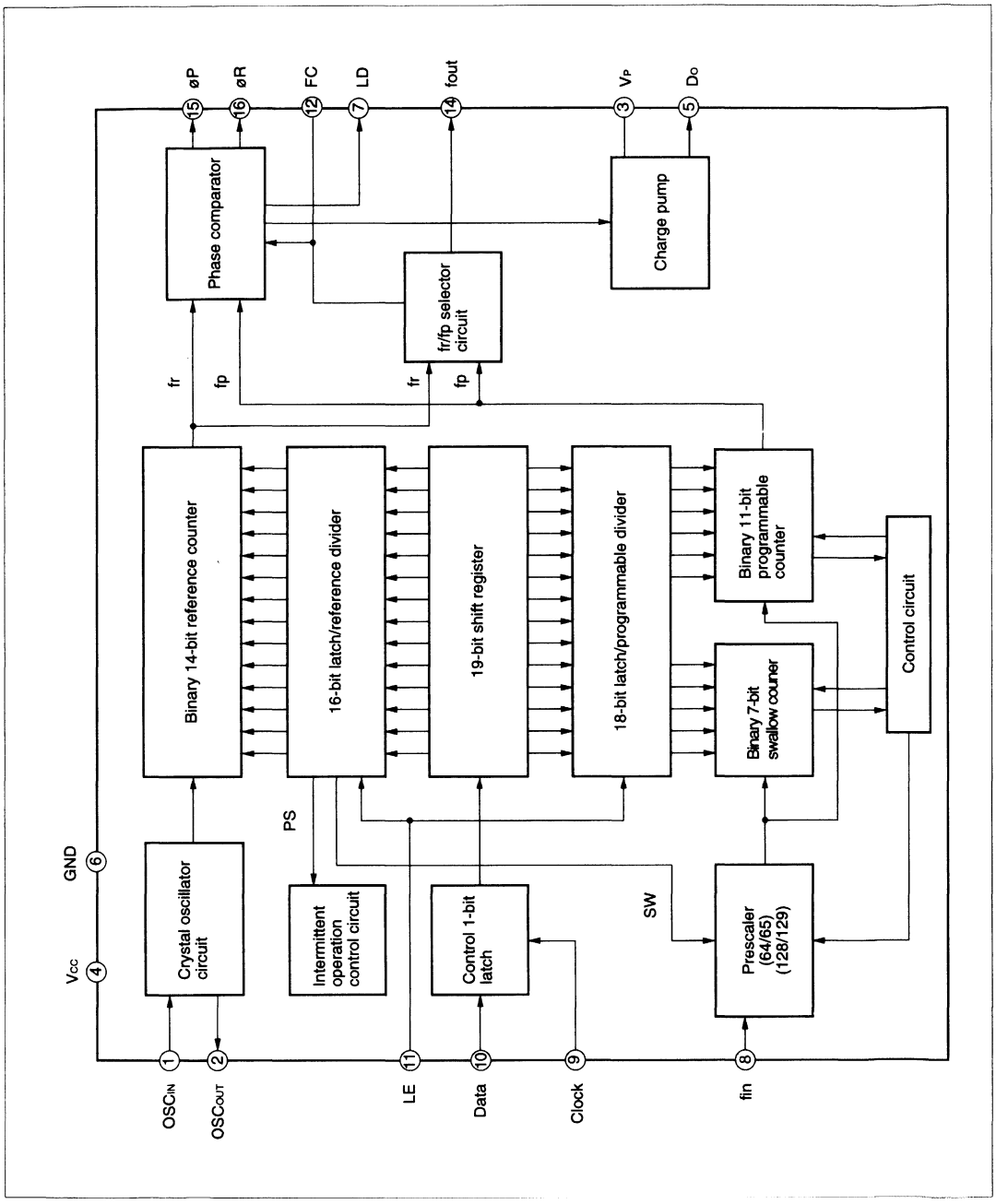
■ PIN ASSIGNMENTS



■ PIN DESCRIPTIONS

Pin No.		Symbol	I/O	Function
SSOP-16	SSOP-20			
1	1	OSC_{IN}	I	Crystal oscillator connection pin serving as a reference divider input pin (Oscillator circuit input pin)
2	3	OSC_{OUT}	O	Crystal oscillator connection pin (Oscillator circuit output pin)
3	4	V_P	—	Power supply pin for charge pump output
4	5	V_{CC}	—	Power supply pin
5	6	D_O	O	Internal charge pump output pin The phase characteristic is inverted depending on the FC pin setting.
6	7	GND	—	GND pin
7	8	LD	O	Lock detector output pin When locked: LD = "H", When unlocked: LD = "L"
8	10	fin	I	Prescaler input pin The pin must be AC-coupled for input.
9	11	Clock	I	Clock input pin for 19-bit shift registers The shift resister reads data at the rise of the clock pulse.
10	13	Data	I	Binary-coded serial data input pin The last bit in the data is a control bit. Control bit = "H": Sends data to the 16-bit latch. "L": Sends data to the 18-bit latch.
11	14	LE	I	Load enable signal input pin When LE = "H", the pin sends the contents of the shift register to the latch according to the control bit.
12	15	FC	I	Phase comparator phase switching pin When FC = "L", the pin inverts characteristics of the charge pump and the phase comparator. It also switches the fout pin (test pin) output between fr and fp.
14	17	fout	O	Phase comparator input monitor pin The pin outputs the reference divider output (fr) or programmable divider output (fp) signal depending on the FC pin input level. FC = "H": Equivalent to fr output FC = "L": Equivalent to fp output This pin is an N-channel open-drain output.
15	18	øP	O	Phase comparator output pin for external charge pump The phase characteristic is inverted depending on the FC pin setting. This pin is an N channel open-drain output.
16	20	øR	O	Phase comparator output pin for external charge pump The phase characteristic is inverted depending on the FC pin setting. This pin is a CMOS output.
13	2, 9, 12, 16, 19	N.C.	—	No, connection

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min.	Max.	
Power supply voltage	V_{CC}	−0.5	5.0	V
	V_P	V_{CC}	5.5	V
Output voltage	V_O	−0.5	V_{CC} + 0.5	V
Output current	I_O	−10	10	mA
Open-drain voltage	V_{OOP}	−0.5	6.0	V
Storage temperature	Tstg	−55	+125	°C

Note: Permanent device damage may occur if the above absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Power supply voltage	V_{CC}	2.7	3.0	3.6	V
	V_P	V_{CC}	—	5.0	V
Input voltage	V_{IN}	GND	—	V_{CC}	V
Operating temperature	Ta	−40	—	+85	°C

Note: Although the MB15A03 contains an antistatic element to prevent electrostatic breakdown and the circuitry has been improved in electrostatic protection, observe the following precautions when handling the device:

- When storing or carrying the device, put it in a conductive case.
- This is static-sensitive device; take proper anti-ESD precautins. Ensure that personnel and equipment are properly grounded. Cover workbenches with grounded conductive mats.
- Before fitting the device into or removing it from the socket, turn the power supply off.
- Protect leads with conductive sheet when handling or transporting PC boads with devices.

■ ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.7 V to 3.6 V, Ta = −40°C to +85°C)

Parameter		Symbol	Condition	Value			Unit
				Min.	Typ.	Max.	
Power supply current*1		I_{CC}	—	—	6.5	—	mA
Power save current		I_{PS}	—	—	100	—	µA
Operating frequency	fin*2	fin	—	300	—	1100	MHz
	OSC_{IN}	f_{OSC}	—	—	12	20	MHz
Input sensitivity	fin	V_{fin}	50 Ω system	−10	—	6	dBm
	OSC_{IN}	V_{OSC}	—	0.5	—	—	V_{P-P}
High-level input voltage	Data, Clock, LE, FC	V_{IH}	—	0.7 × V_{CC}	—	—	V
Low-level input voltage		V_{IL}	—	—	—	0.3 × V_{CC}	V
High-level input current	Data, Clock	I_{IH}	—	—	—	1.0	µA
Low-level input current		I_{IL}*3	—	−1.0	—	—	µA
Input current	OSC_{IN}	I_{OSC}*3	—	—	±50	—	µA
High-level output voltage	Excluding D_O and OSC_{OUT}	V_{OH}*4	—	2.1	—	—	V
Low-level output voltage		V_{OL}*5	—	—	—	0.4	V
High-impedance cutoff current	D_O, fout, øP	I_{OFF}*6	—	—	—	1.1	µA
Output currrent	Excluding D_O and OSC_{OUT}	I_{OH}*3	V_{CC} = 3.0 V	−1.0	—	—	mA
		I_{OL}		—	—	1.0	mA

*1: Assuming the PLL lock conditions: fin = 1.1 GHz, f_{OSC} = 12 MHz, V_{CC} = 3.0 V
*2: The fin pin must be AC-coupled. The minimum operating frequency assumes coupling at 1000 pF.
*3: The minus sign (−) signifies the direction of the signal flowing from the IC.
*4: Assuming V_{CC} = 3.0 V and I_{OH} = −1 mA
*5: Assuming V_{CC} = 3.0 V and I_{OL} = 1 mA
*6: V_{CC} = 3.6 V, V_P = V_{CC} to 5.0 V, V_{OOP} = GND to 6.0 V

■ FUNCTIONAL DESCRIPTIONS

1. Pulse Swallow Function

For the pulse swallow function, use the following equations to select their respective setting values:

$$f_{VCO} = [(P \times N) + A] \times f_{OSC} + R$$

f_{VCO}	:	Output frequency of externally connected VCO
P	:	Prescaler divide ratio (64 or 128)
N	:	Divide ratio of 11-bit programmable counter (5 to 2047)
A	:	Divide ratio of 7-bit swallow counter (0 to 127, where A < N)
f_{OSC}	:	Reference oscillation frequency (OSC_{IN} input frequency)
R	:	Divide ratio of 14-bit programmable reference counter (6 to 16383)

2. Serial Data Input Method

Serial data is processed using three input pins (Data, Clock, and LE pins) to control the 16-bit reference divider and the 18-bit programmable divider separately.

Input binary-coded serial data to the Data pin.

Serial data is input to the internal shift register in sequence at the rise of each clock pulse. When the load enable signal input pin has a high level, the input data is transferred to the latch depending on the control bit.

Control bit = "H" → Transfer to the 16-bit latch
Control bit = "L" → Transfer to the 18-bit latch

(1) Serial Data Format

• **Reference divider**

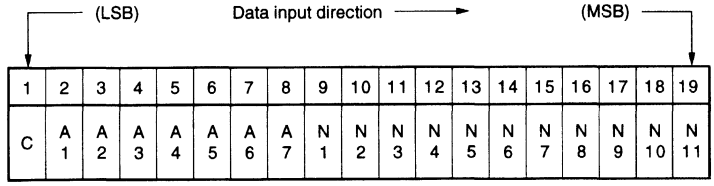
(LSB) Data input direction → (MSB)

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
C	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	SW	PS

R1 to R4: These bits select the divide ratio of the programmable reference counter (6 to 16383)
SW: This bit selects the divide ratio of prescaler
PS: Power save control bit
C: Control bit

Note: Start data input with MSB first.

• **Programmable divider**



1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
C	A1	A2	A3	A4	A5	A6	A7	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11

A1 to A7: Swallow counter divide ratio setting bits (Set value: 0 to 127)
N1 to N11: Programmable counter divide ratio setting bits (Set value: 5 to 2047)
C: Control bit

Note: Start data input with MSB first.

(2) Data Settings

• **Setting the binary 14-bit reference counter (R1 to R14)**

Divide ratio	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1
6	0	0	0	0	0	0	0	0	0	0	0	1	1	0
7	0	0	0	0	0	0	0	0	0	0	0	1	1	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: The divide ratio must not be less than 6.

• **Setting the binary 11-bit programmable counter (N1 to N11)**

Divide ratio	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1
5	0	0	0	0	0	0	0	0	1	0	1
6	0	0	0	0	0	0	0	0	1	1	0
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

Note: The divide ratio must not be less than 5.

- **Setting the binary 7-bit swallow counter (A1 to A7)**

Divide ratio	A7	A6	A5	A4	A3	A2	A1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

- **Selecting the prescaler divide ratio (SW)**

Divide ratio	SW
64/65	1
128/129	0

- **Power save/ intermittent operation control (PS)**

Mode	PS
Normal mode	1
Power save mode	0

Note: Be sure to reset the PS bit to 0 immediately after turning the power on.

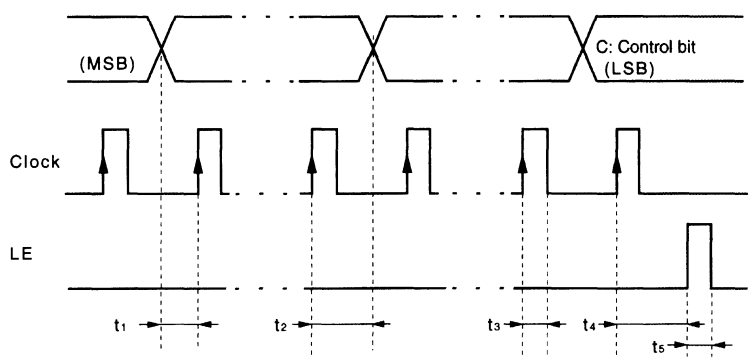
It is possible to operates internal circuits only when required and halts them when not required, lessening power consumption of the entire circuitry (intermittent operation).

However, letting the LSI simply start operating the circuit which has been halted results in a problem that excessive error signal output from the phase comparator unlocks the PLL. This is because the reference frequency (fr) and comparative frequency (fp) input to the phase comparator have an undefined phase relationship even when they are completely the same.

To solve this problem, the MB15A03 provideds intermittent operation control to suppress variation in the locked frequency by forced phase adjustment upon return from the halt state.

(3) Serial Data Input Timing

t_1, t_4 > 100 ns, t_2 > 1000 ns, t_3 > 300 ns, t_5 > 800 ns



Note: Serial data is fetched at the rise of each clock pulse.

3. Relationships between FC Pin Inputs and Phase Characteristics

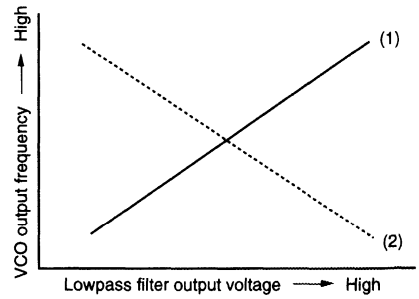
The FC pin is the phase switching pin for the phase comparator. Controlling the FC pin input allows the characteristics of the internal charge pump output (D_O) and external charge pump outputs (øR and øP outputs) to be selected. In addition, the phase comparator input monitor pin (fout) is also controlled via the FC pin.
The following table relation between FC pin inputs and D_O, øR, øP, and fout:

Phase comparator input	FC: "H"				FC: "L"			
	D_O	øR	øP	fout	D_O	øR	øP	fout
fp < fr	H	L	L	fr	L	H	Z	fp
fr < fp	L	H	Z		H	L	L	
fp = fr	Z	L	Z		Z	L	Z	

Z: High impedance

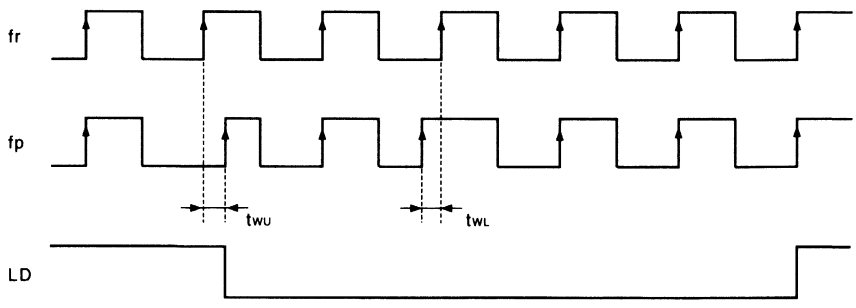
When designing a PLL frequency synthesizer, control the FC pin depending on the lowpass filter and VCO polarities.

When the LPF/VCO polarity is (1)
(FC: "H")
When the LPF/VCO polarity is (2)
(FC: "L")

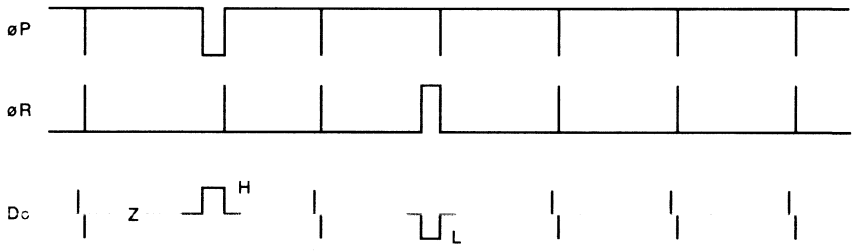


Note: When using an active lowpass filter, pay attention to its polarity.

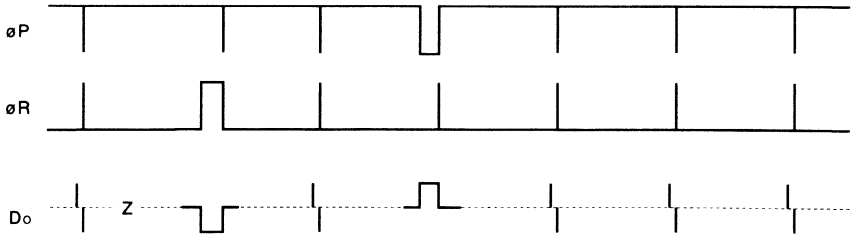
■ PHASE COMPARATOR OUTPUT WAVEFORMS



• When the FC bit = "H"



• When the FC bit = "L"

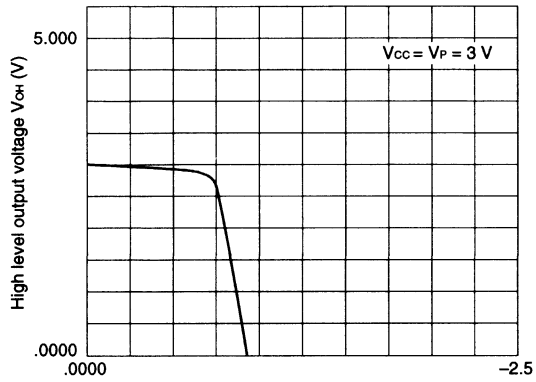


Notes: • A phase error is detected between -2π and $+2\pi$. The phase comparator conversion gain is $V_P/4\pi$.
• The LD output goes low when it becomes phase difference t_{WU} or more. The LD output goes high when it remains equal to or smaller than t_{WL} for three cycles or more.
• t_{WU} and t_{WL} are determined by the OSC_{IN} input frequency as follows:
$t_{WU} \geq 8/f_{OSC}$ [s] ..... When f_{OSC} = 12.8 MHz: $t_{WU} \geq 625$ ns
$t_{WL} \leq 16/f_{OSC}$ [s] ..... When f_{OSC} = 12.8 MHz: $t_{WL} \leq 1250$ ns

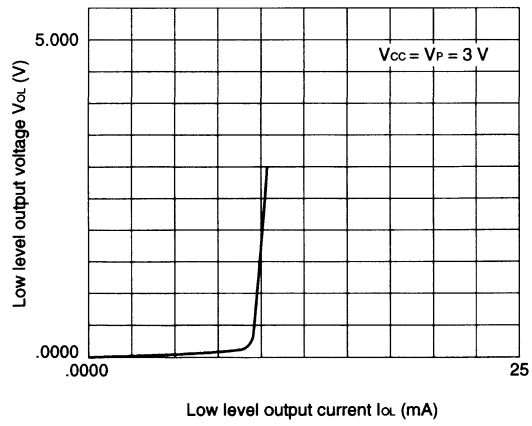
■ TYPICAL CHARACTERISTIC CURVES

1. D_O Output Current Characteristics

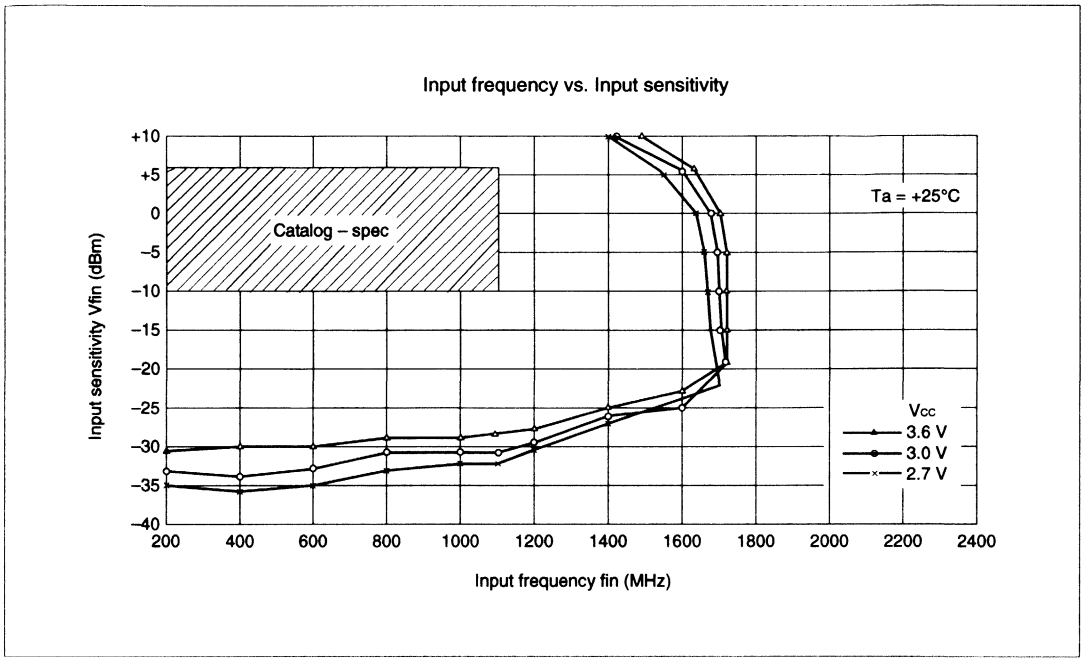
I_{OH} vs. V_{OH} characteristics



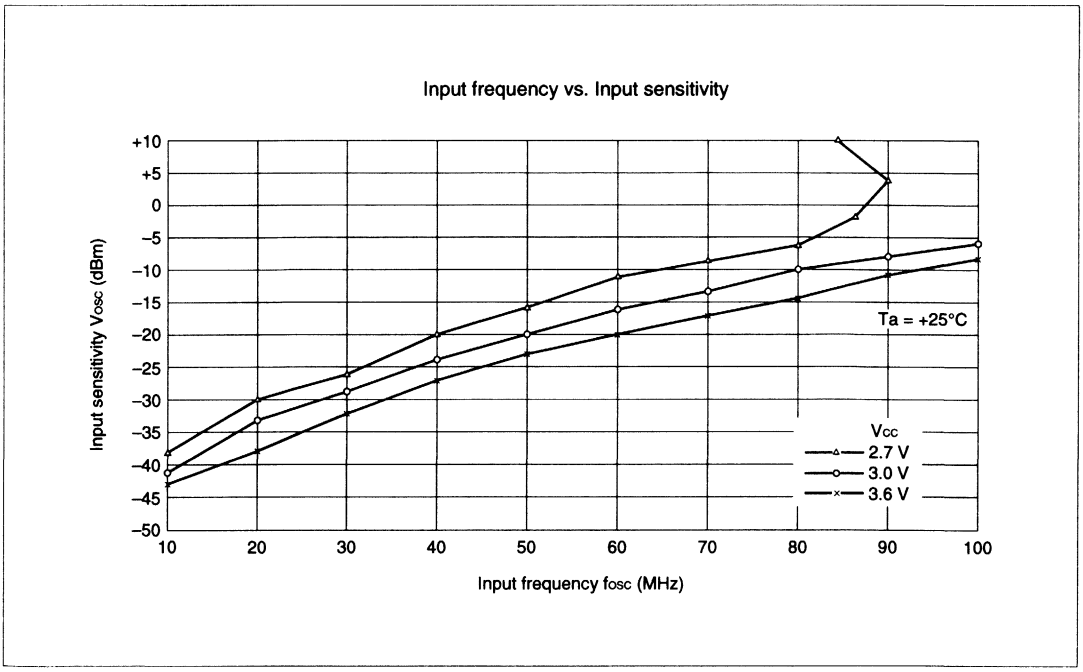
I_{OL} vs.V_{OL} characteristics



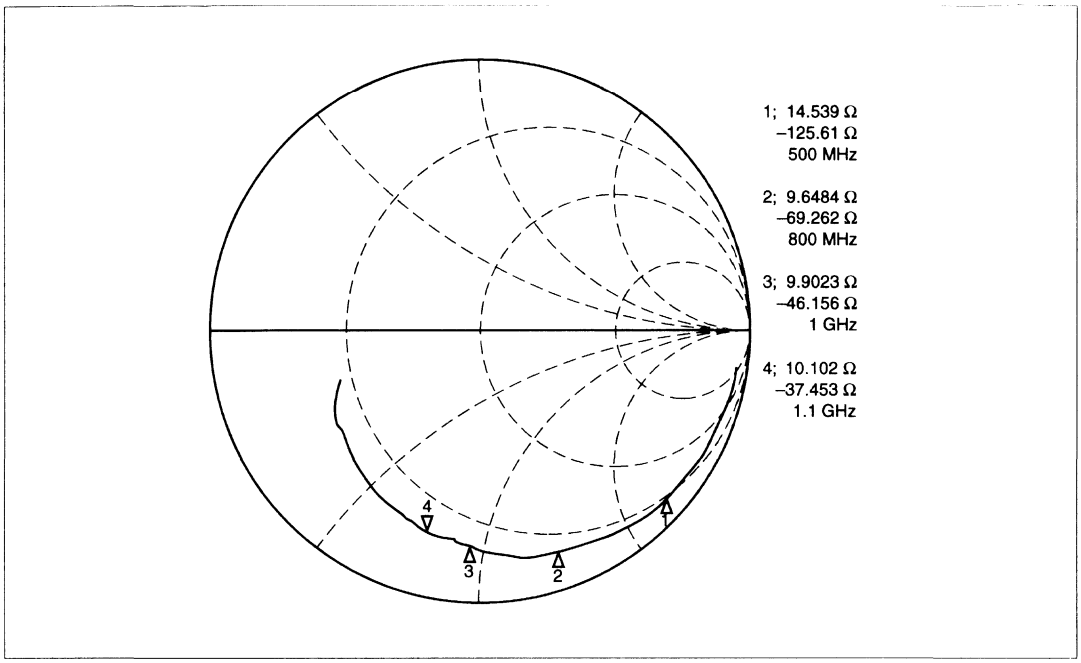
2. fin Input Sensitivity Characteristics



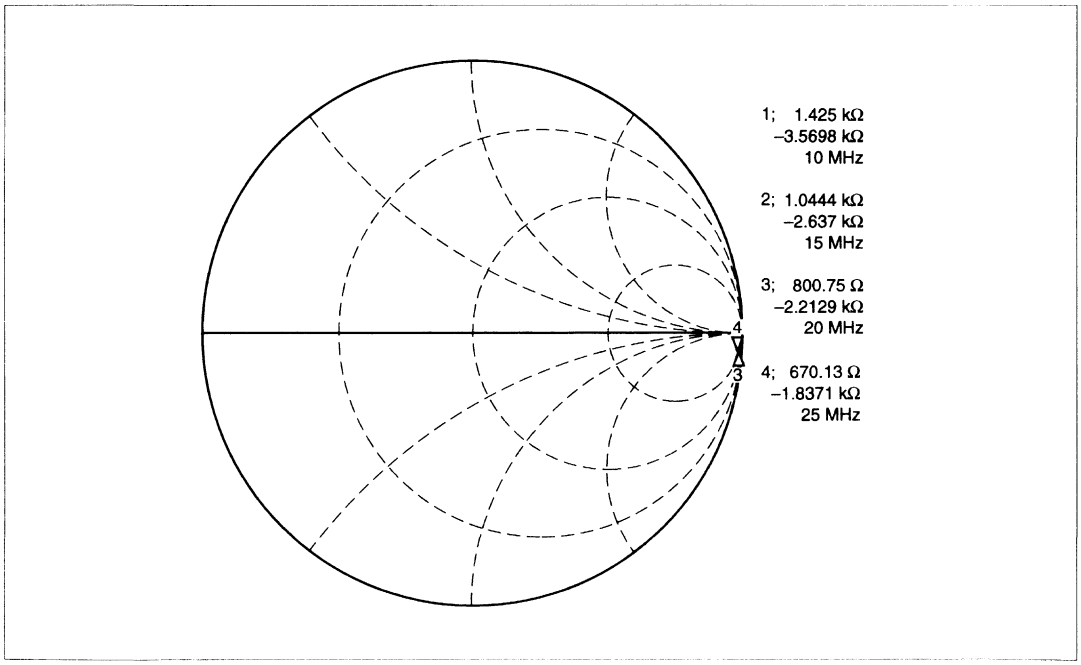
3. OSC_{IN} Input Sensitivity Characteristics



4. fin Input Impedance Characteristics



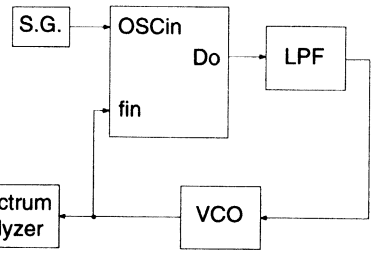
5. OSC_{IN} Input Impedance Characteristics



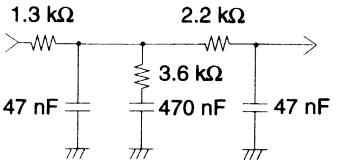
■ REFERENCE INFORMATION

Typical plots measured with the test circuit are shown below. Each plots show lock up time, phase noise, and reference leakage.

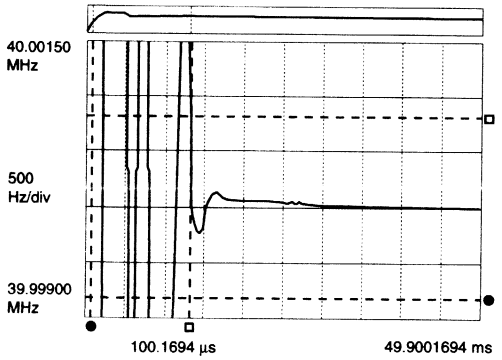
Test Circuit



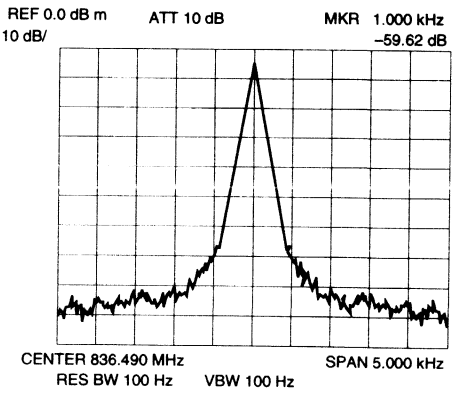
- f_{VCO} = 836.49 MHz
- K_V = 12 MHz/V
- f_r = 30 kHz
- f_{OSC} = 15.36 MHz
- LPF



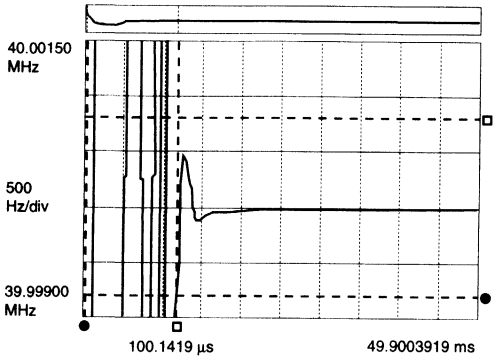
PLL Lock Up Time = 12.8 ms
(824.010 MHz → 848.97 MHz, within ±800 Hz)



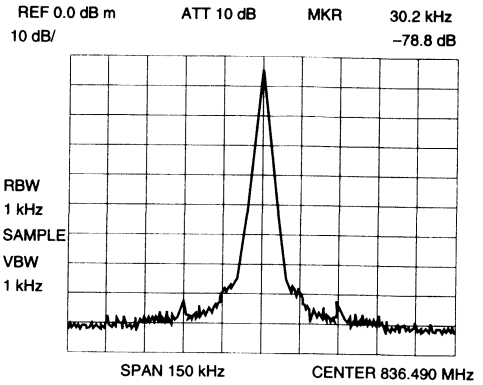
PLL Phase Noise
@ within loop band = 79.6 dBc/Hz



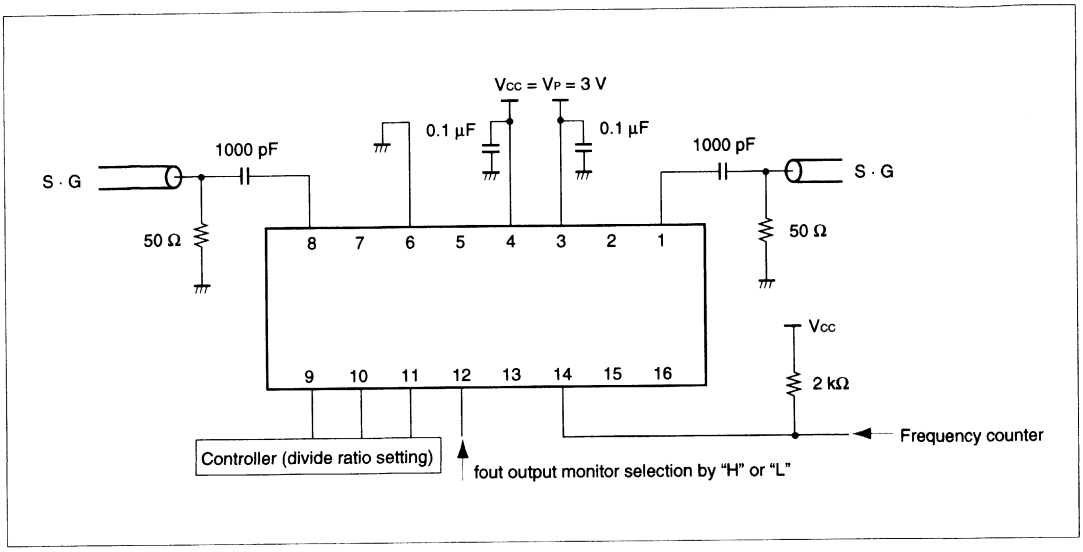
PLL Lock Up Time = 11.6 ms
(848.97 MHz → 824.010 MHz, within ±800 Hz)



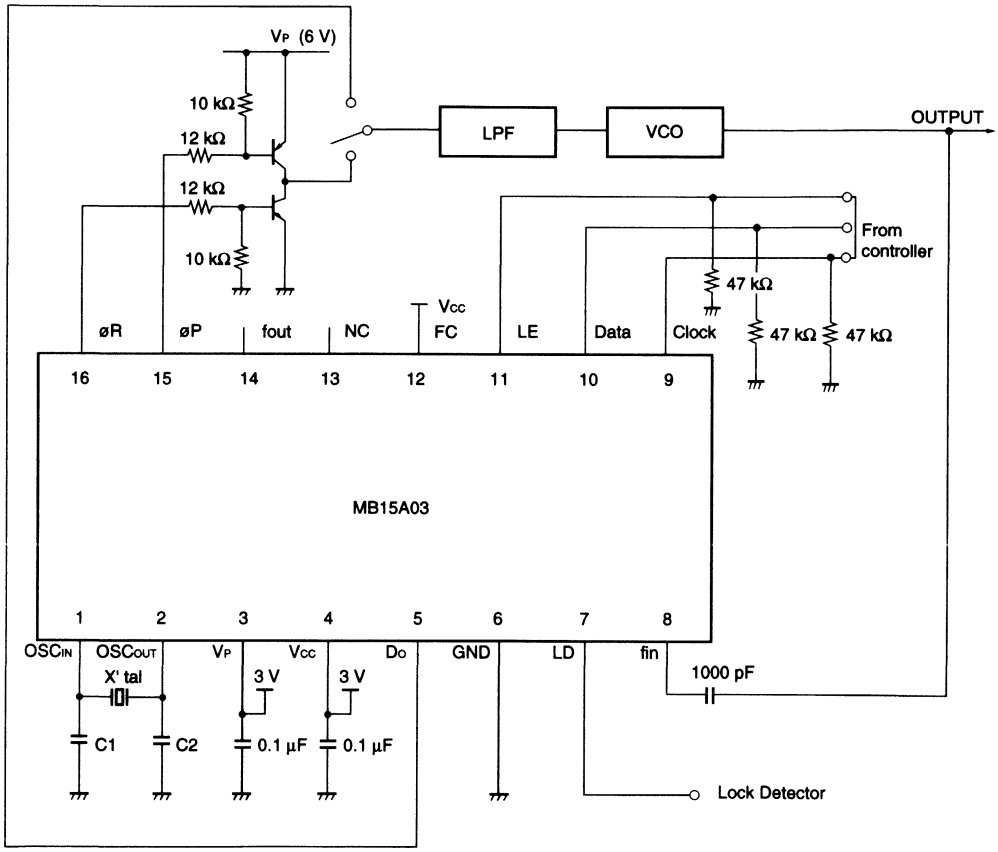
PLL Reference Leakage
@ 30 kHz offset = 78.8 dBc



■ TEST CIRCUIT EXAMPLE (fin/OSC_{IN} Input Sensitivity Measurement)



■ APPLICATION EXAMPLE (16-pin Package)



VP: 5 V max.
C1, C2: Depending on the crystal oscillator
Clock, Data LE: When input pins are open, please insert the pull down resistor.

■ ORDERING INFORMATION

Part number	Package	Remarks
MB15A03PFV1	16-pin, Plastic SSOP (FPT-16P-M05)	
MB15A03PFV2	20-pin, Plastic SSOP (FPT-20P-M03)	

FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-21339-1E

ASSP
Dual Serial Input PLL Frequency Synthesizer
On-Chip 1.1 GHz Prescaler

MB15U10

■ DESCRIPTION

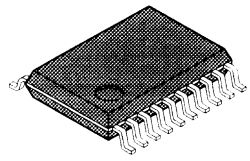
The Fujitsu MB15U10 is a dual serial input phase-locked loop (PLL) frequency synthesizer and is ideally suitable for mobile communications such as cellular phones.
The MB15U10 has two PLL frequency synthesizer circuits on a single chip: one for transmission and the other for reception (PLL1 and PLL2).
It can operate from a +2.6V to 5.5V supply. Fujitsu's advanced technology achieves an Icc of 7 mA (typical) as well as 10 µA (max.) at power saving mode.

■ FEATURES

- Two PLLs' for transmission/reception
- Low current consumption : I_{CC} = 7 mA typ. at 3 V
- Power saving funtion : I_{PS} = 10 µA max.
- Divide ratio setting with serial data input :
  Binary 12-bit reference counter:6 to 4,095
  Binary 17-bit main counter: 1,024 to 131,071
  *Main counters can be programmed individually each other.
- On-chip constant current source charge pumps
- Adjustable charge pump output current with an external resistor
- Lock detection function
- Phase matching circuit helps fast intermittent operation
- Plastic 20-pin SSOP (shrink small outline) package

■ PACKAGE

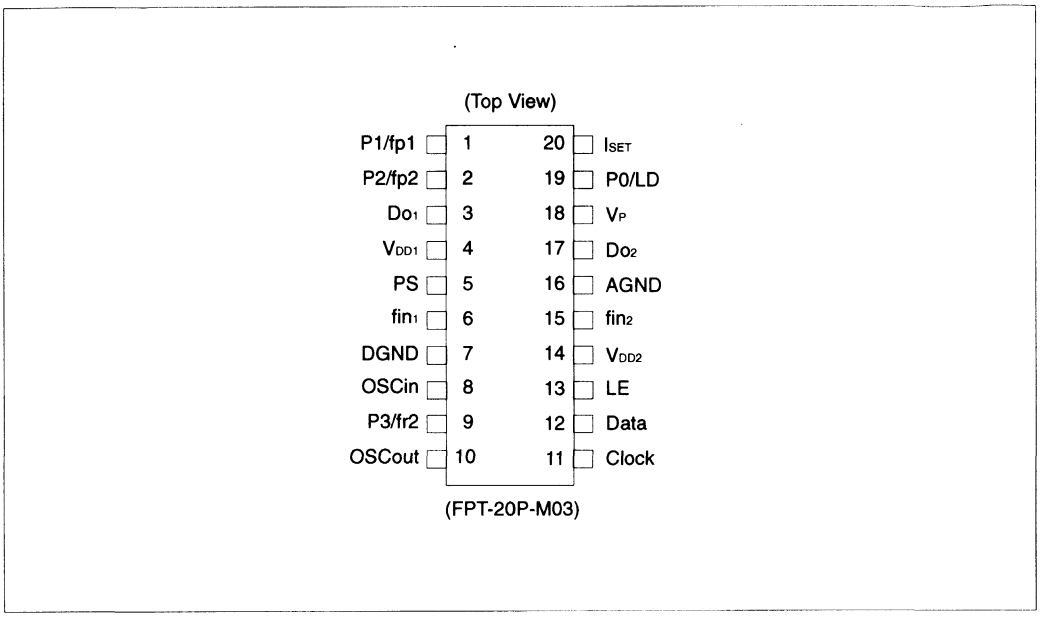
20-pin, Plastic SSOP



(FPT-20P-M03)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

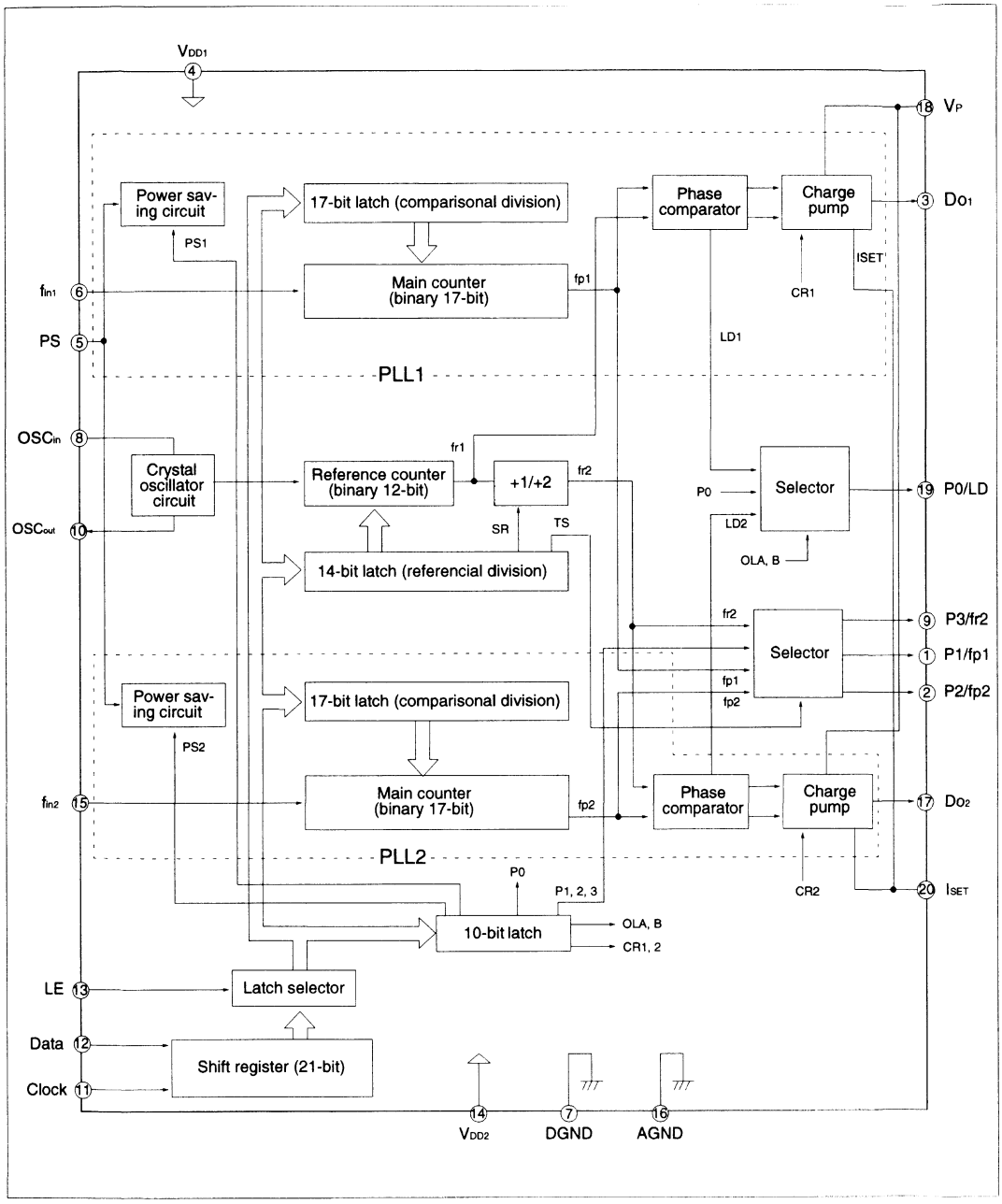
■ PIN ASSIGNMENT



■ PIN DESCRIPTION

Pin No.	Pin name	Descriptions
1	P1/fp1	Data output / fp1 monitoring output (Open drain output)
2	P2/fp2	Data output / fp2 monitoring output (Open drain output)
3	D_{O1}	Charge pump output (PLL1)
4	V_{DD1}	Power supply for digital blocks (PLL1)
5	PS	Power saving mode control (input "L" : power saving mode)
6	f_{in1}	RF input (PLL1)
7	DGND	Ground for digital blocks
8	OSCin	Crystal oscillator or TCXO input
9	P3/fr2	Data output / fr2 monitoring output (Open drain output)
10	OSCout	Crystal oscillator output
11	Clock	Clock input
12	Data	Data input
13	LE	Load enable of serial input data (input "H" : Data is shifted into a latch.)
14	V_{DD2}	Power supply for digital blocks (PLL2)
15	f_{in2}	RF input (PLL2)
16	AGND	Ground for the charge pumps
17	D_{O2}	Charge pump output (PLL2)
18	V_P	Power supply for charge pump
19	P0/LD	Data output / lock detector output (Open drain output) Output is selected by "OLA" and "OLB" bits in a serial data
20	I_{SET}	Charge pump output current adjustment (A resistor is connected.)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Remark
Power supply voltage	$V_{DD1, 2}$	−0.3 to +6.0	V	
	V_P	V_{DD} to 6.0	V	
Output voltage	V_O	−0.3 to V_{DD} +0.3	V	
Output current	I_O	±10	mA	
Storage temperature	Tstg	−55 to +125	°C	

Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Remark
		Min	Typ	Max		
Power supply voltage	V_{DD1}, V_{DD2}	2.6	–	5.5	V	
	V_P	V_{DD}	–	6.0	V	
Input voltage	V_I	GND	–	V_{DD}	V	
Operating temperature	Ta	−30	–	+85	°C	

Notes: To protect against damage by electrostatic discharge, note the following handling precautions:
- Store and transport devices in conductive containers.
- Use properly grounded workstations. tools, and equipment.
- Turn off power before inserting or removing this device into or from a socket.
- Protect leads with conductive sheet, when transporting a board mounted device.

■ ELECTRICAL CHARACTERISTICS

Ta = 25°C

Parameter		Symbol	Value			Unit	Condition
			Min	Typ	Max		
Power supply current ($I_{DD1} + I_{DD2}$)		I_{DD}	–	7.0	9.0	mA	*1
			–	11.0	13.5	mA	*2
Stand by current	$V_{DD1,2}$	I_{PS}	–	–	10	µA	
Operating frequency	$fin_{1,2}$	fin	90	–	1100	MHz	
	OSC_{in}	f_{OSC}	3	12.8	35	MHz	
Input sensitivity	$fin_{1,2}$	V_{fin}	–13	–	+1	dBm	50Ω, Vcc = 2.6 to 3.5V
	$fin_{1,2}$	V_{fin}	–7	–	+1	dBm	50Ω, Vcc = 3.5 to 5.5V
	OSC_{in}	V_{OSC}	0.5	–	–	Vp-p	
High-level input voltage	Data, Clock, LE, PS	V_{IH}	$V_{DD} \times 0.7$	–	–	V	
Low-level input voltage		V_{IL}	–	–	$V_{DD} \times 0.3$	V	
High-level input current	Data, Clock, LE, PS	I_{IH}	–	–	1.0	µA	
Low-level input current		I_{IL}	–1.0	–	–	µA	
Input current	OSC_{in}	I_{OSC}	–100	–	100	µA	
Low-level output voltage	P0 to P3	V_{OL}	–	–	0.4	V	Open drain output
Set output voltage	I_{SET}	V_{SET}	–	1.2	–	V	R_{SET} = 5kΩ to 60kΩ
High-impedance cut off current	Do, P0 to P3	I_{OFF}	–	–	1.1	µA	
Output current	$Do_{1,2}$	I_{DOH1}	1.4	1.9	2.4	mA	R_{SET} = 7kΩ connected. CR1, 2 bits = "1" V_{DD} = 3.0V, V_P = 5.0V
		I_{DOL1}	1.4	1.9	2.4	mA	
	$Do_{1,2}$	I_{DOH0}	0.7	0.96	1.2	mA	R_{SET} = 7kΩ connected. CR1, 2 bits = "0" V_{DD} = 3.0V, V_P = 5.0V
		I_{DOL0}	0.7	0.96	1.2	mA	
	P0 to P3	I_{OL}	1.0	–	–	mA	Open drain

Note: *1 ; f_{IN} = 1.1 GHz, OSC_{IN} = 12.8 MHz, V_{DD} = 3.0 V. In locked state.
*2 ; f_{IN} = 1.1 GHz, OSC_{IN} = 12.8 MHz, V_{DD} = 5.0 V. In locked state.

■ FUNCTIONAL DESCRIPTIONS

Serial Data Input

Serial data is processed using the Data, Clock, and LE pins. Serial data controls the programmable reference divider, programmable divider (PLL1) and programmable divider (PLL2) separately by means of address setting.
Binary serial data is entered via the Data pin.
One bit of data is shifted into the internal shift register on the rising edge of the clock. When the load enable pin is high, stored data is latched.

a) Serial data input format

(MSB) ← Direction of data input → (LSB)

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
X	X	X	P0	OLA	OLB	CR1	CR2	X	X	PS1	PS2	P3	P2	P1	X	X	0	0	0	1
MA16	MA15	MA14	MA13	MA12	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0	0	1	0	0
0	0	0	TS	SR	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0	1	0	1
MB16	MB15	MB14	MB13	MB12	MB11	MB10	MB9	MB8	MB7	MB6	MB5	MB4	MB3	MB2	MB1	MB0	0	1	1	0
Auxiliary bit for test (no need at ordinary use)																	0	0	0	0

← Data setting → ← Address →

MA0 to 16	: Divide ratio setting bits of the main counter (PLL1)	[See Table 1]
MB0 to 16	: Divide ratio setting bits of the main counter (PLL2)	[See Table 2]
R0 to 11	: Divide ratio setting bits of the reference counter	[See Table 3]
SR	: Divide ratio select bit of reference frequency (PLL1 and PLL2)	[See Table 4]
P0 to 3	: Setting bits of P0 to P3 output pins	[See Table 5]
OLA, B	: Select bits of P0/LD pin output	[See Table 6]
CR1, 2	: Select bits of charge pump output current	[See Table 7]
PS1, 2	: Power saving mode control bits	[See Table 8]
TS	: Test bits (Set "0" at ordinary use.)	[See Table 9]
X	: Dummy bits (Set "0" or "1".)	
0	: Set "0"	

b) Data setting description

• Table 1 : MA0 to MA16 : Divide ratio of the binary 17-bit main counter (PLL1)

Divide Ratio (MA)	MA16	MA15	MA14	MA13	MA12	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
1024	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
1025	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•

Note: • Divide ratios less than 1,024 are prohibited. (Divide ratio = 1,024 to 131,071)

• Table 2 : MB0 to MB16 : Divide ratio of the binary 17-bit main counter (PLL2)

Divide Ratio (MB)	MB16	MB15	MB14	MB13	MB12	MB11	MB10	MB9	MB8	MB7	MB6	MB5	MB4	MB3	MB2	MB1	MB0
1024	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
1025	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•

Note: • Divide ratios less than 1,024 are prohibited. (Divide ratio = 1,024 to 131,071)

• Table 3 : R0 to R11 : Divide ratio of the binary 12-bit reference counter

Divide Ratio (R)	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
6	0	0	0	0	0	0	0	0	0	1	1	0
7	0	0	0	0	0	0	0	0	0	1	1	1
•	•	•	•	•	•	•	•	•	•	•	•	•

Note: • Divide ratios less than 6 are prohibited. (Divide ratio = 6 to 4,095)

• Table 4 : Divide ratio select bit of reference frequency (PLL1 and PLL2)

SR	Divide ratio of reference frequency (PLL1)	Divide ratio of reference frequency (PLL2)
0	R	R
1	R	2R

Note: R = Programmed value with R0 to R11 bits

• Table 5 : P0 to P3 ; P0 to P3 outputs control

PX bit	PX output (19, 1, 2, 9 pins)
0	ON ("L")
1	OFF ("Z")

Notes: X = 0 to 3

• Table 6 : OLA, OLB ; 19-pin output selection

OLA	OLB	19-pin output
0	0	P0 signal
0	1	Lock detect signal (PLL2)
1	0	Lock detect signal (PLL1)
1	1	Lock detect signal (PLL1 and PLL2)

• Table 7 : CR1, CR2 ; Charge pump output current selection

CR1, 2	Charge pump output current
0	I_{DO}
1	$2I_{DO}$

Notes: PLL1 and PL2 can be controlled individually.

• Table 8 : PS ; Power saving control

PS1, 2	Operating mode
0	Power saving mode
1	Operation

Notes: PLL1 and PL2 can be controlled individually.

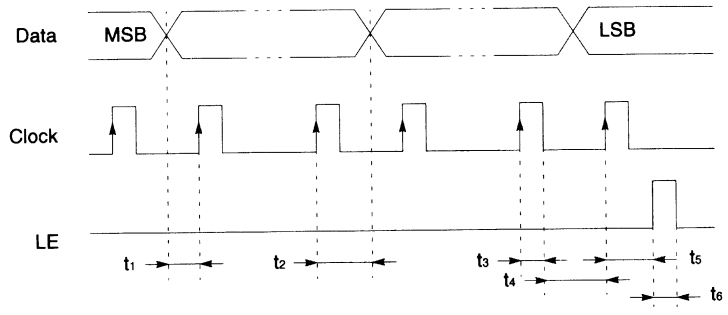
• Table 9 : TS ; Test bit (Set to "0" at ordinary use.)

TS	1-pin	2-pin	9-pin
0	Output P1 signal	Output P2 signal	Output P3 signal
1	Outputs fp1	Outputs fp2	Outputs fp3

Notes: Reference frequency and comparison frequency can be monitored via P1 to P3 pins.

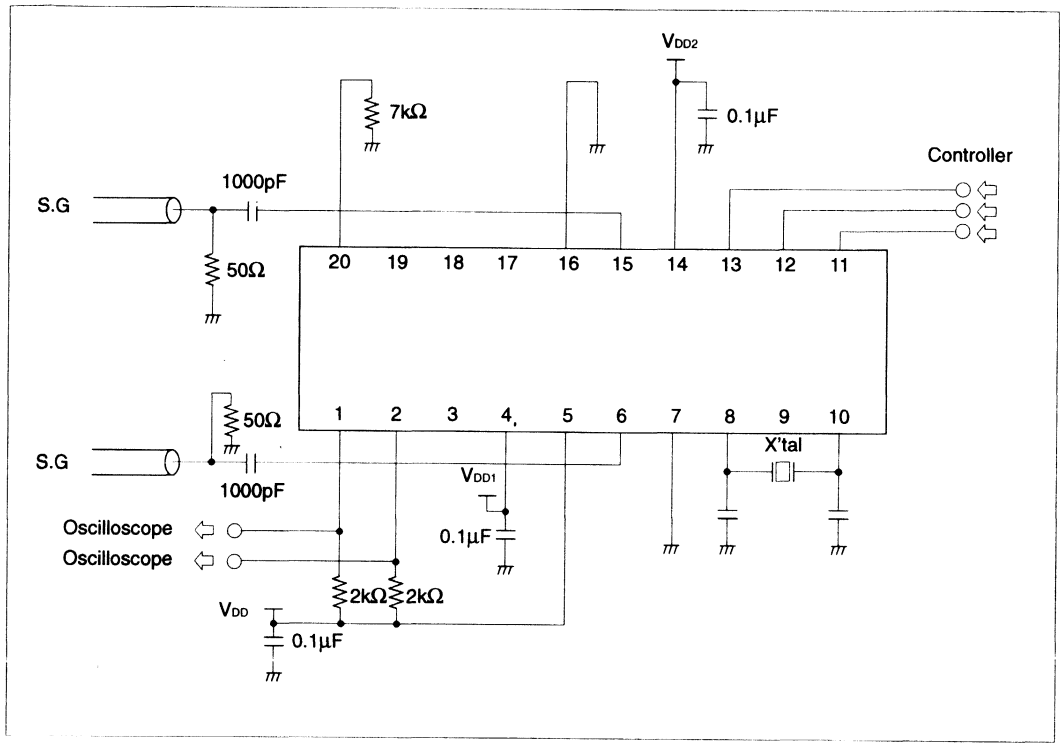
Serial Data Input Timing

- t_1 (≥ 20 ns), t_2 (≥ 20 ns), t_3 (≥ 50 ns), t_4 (≥ 50 ns), t_5 (≥ 20 ns), t_6 (≥ 1000 ns)



Note: One bit of data is shifted into the shift register on the rising edge of the clock.

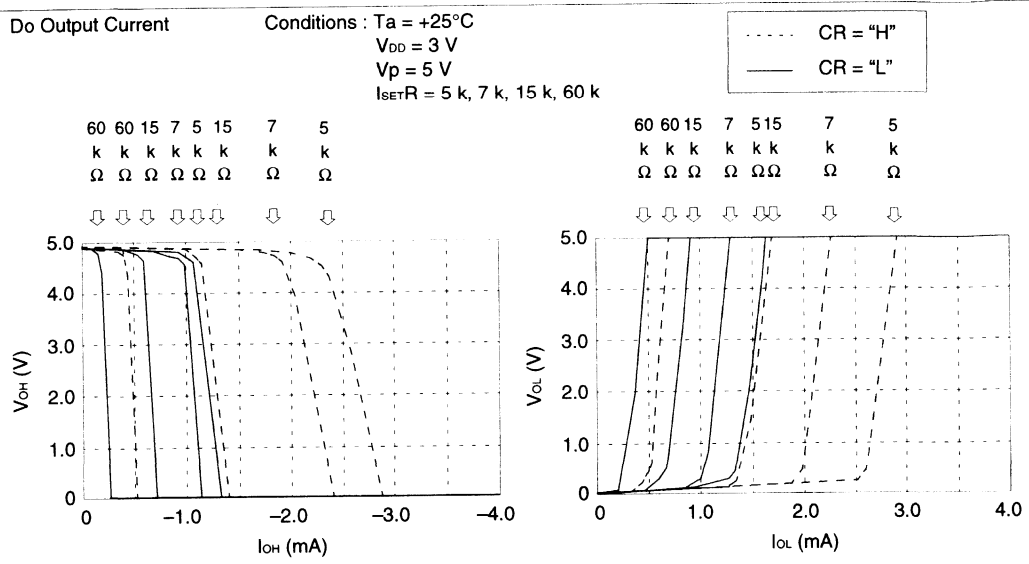
■ TEST CIRCUIT (for Measuring fin Input Sensitivity)



■ TYPICAL CHARACTERISTICS

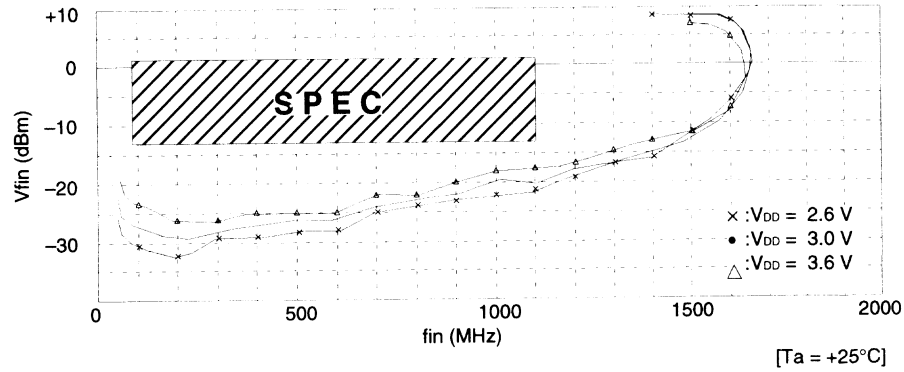
Do Output Current

Conditions : Ta = +25°C
V_{DD} = 3 V
Vp = 5 V
$I_{SET}R$ = 5 k, 7 k, 15 k, 60 k

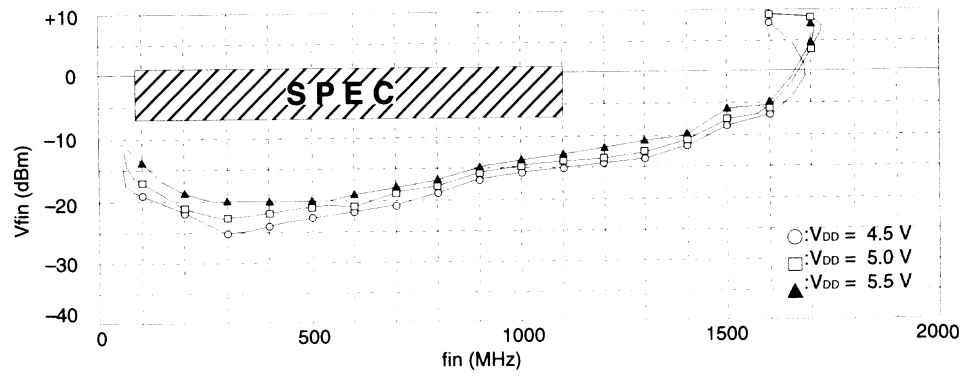


fin Input Sensitivity

[Ta = +25°C]



[Ta = +25°C]



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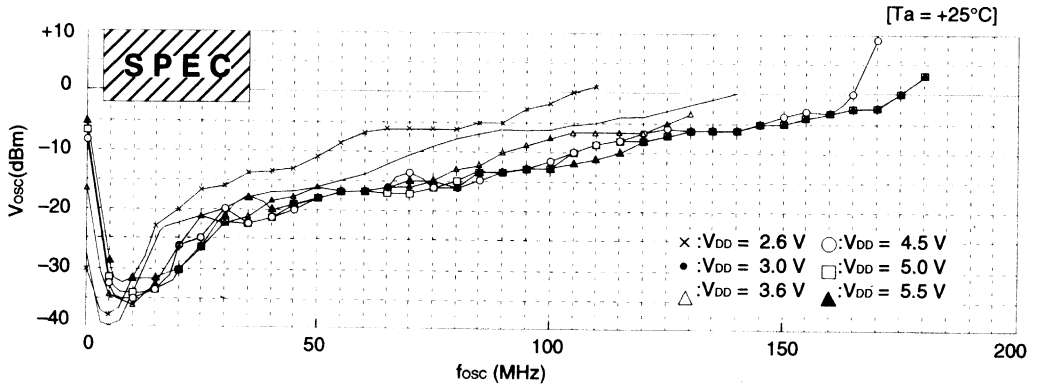
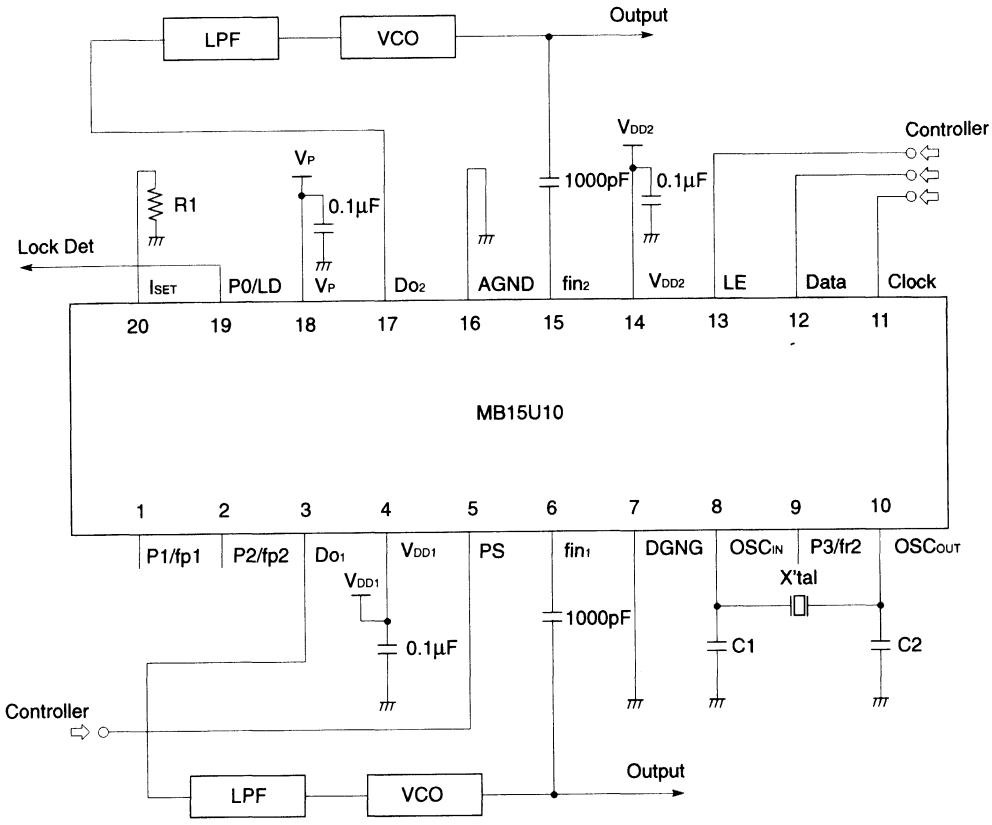
OSCin Input Sensitivity



■ APPLICATION EXAMPLE

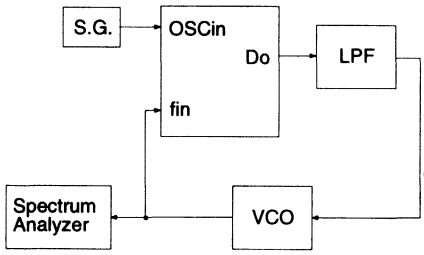


R1	: Values(5 to 60 kΩ) are used to determine the output current for charge pump.
C1, C2	: Determined by the crystal oscillator
Clock, Data, LE	: Insert pull down/pull up resistors to prevent oscillation when the terminals are left open.
PS	: When not in use, insert a pull up resistor with respect to the power supply.

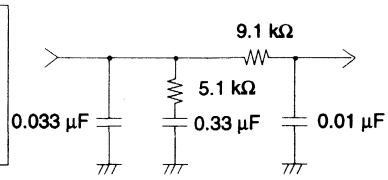
■ REFERENCE INFORMATION

Typical plots measured with the test circuit are shown below.
Each plots shows lock up time, phase noise, and reference leakage.

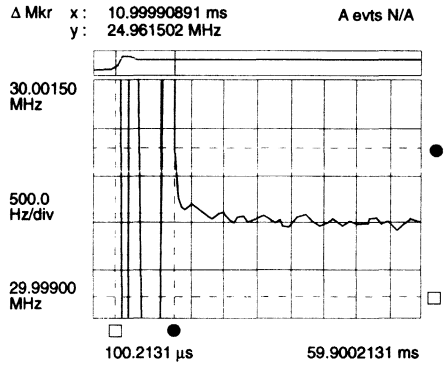
Test Circuit

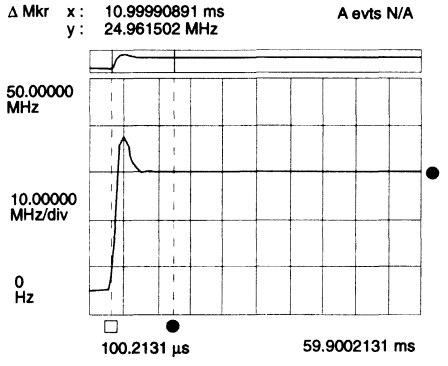


- f_{VCO} = 836.490 MHz
- K_V = 12 MHz/V
- f_r = 30 kHz
- f_{OSC} = 15.36 MHz
- LPF

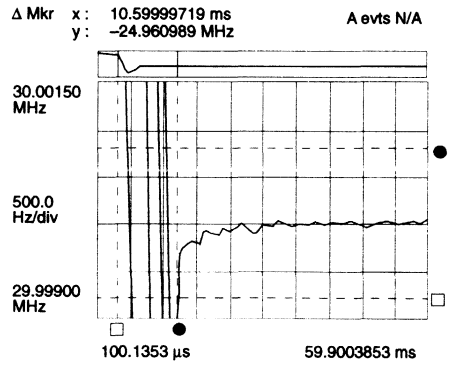


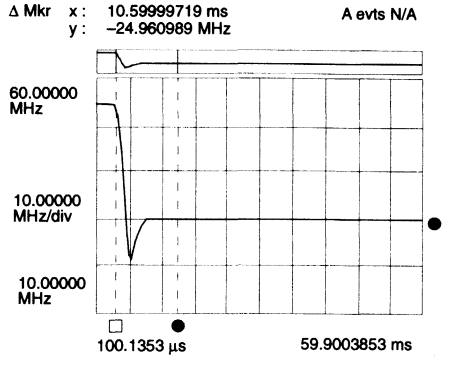
PLL Lock Up Time = 11.0 ms
(824.01 MHz → 848.97 MHz, within ±800 Hz)





PLL Lock Up Time = 10.6 ms
(848.97 MHz → 824.01 MHz, within ±800 Hz)





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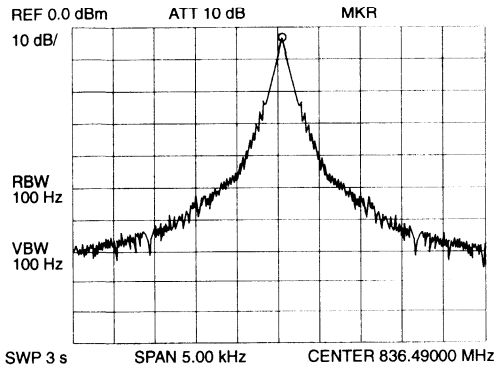
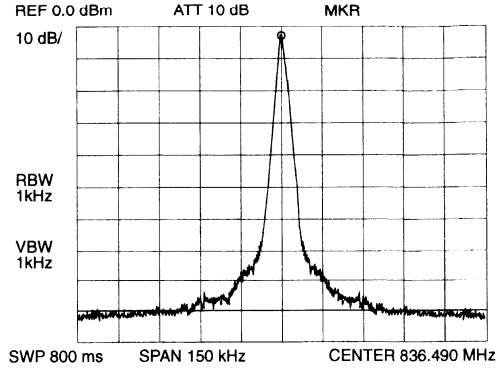
PLL Phase Noise (Tx mode)

@±1 kHz offset at 836.49 MHz = 75 dBc/Hz

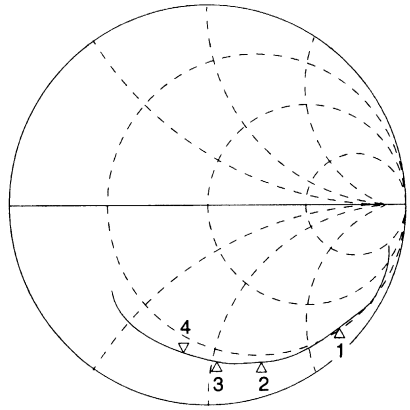


PLL Reference Leakage (Tx mode)

@±30 kHz offset at 836.49 MHz = 82 dBc



fin Input Impedance



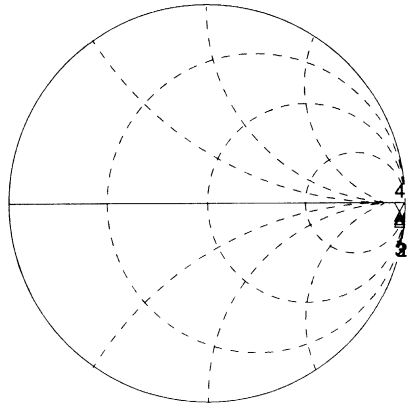
1: 20.93 Ω
−130.75 Ω
500 MHz

2: 11.281 Ω
−71.824 Ω
800 MHz

3: 11.871 Ω
−51.166 Ω
1 GHz

4: 11.627 Ω
−42.119 Ω
3.4352 pF
1.1 GHz

OSCin Input Impedance



1: 1.5699 kΩ
−2.6509 kΩ
10 MHz

2: 889.63 Ω
−2.0951 kΩ
15 MHz

3: 537.31 Ω
−1.6434 kΩ
20 MHz

4: 342.19 Ω
−1.3733 kΩ
4.6357 pF
25 MHz

■ ORDERING INFORMATION

Part number	Package	Remarks
MB15U10PFV	20pin, Plastic SSOP (FPT-20P-M03)	

MEMO

FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-21335-1E

ASSP

Dual Serial Input PLL Frequency Synthesizer

MB15B03

■ DESCRIPTION

The Fujitsu MB15B03 is a serial input Phase Locked Loop (PLL) frequency synthesizer with a 1.1GHz and a 300MHz prescalers. A 64/65 or a 128/129 for the 1.1GHz prescaler, and a 16/17 or a 32/33 for 300MHz prescaler can be selected that enables pulse swallow operation.

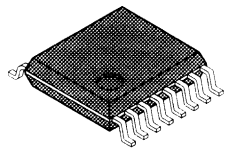
Furthermore, a super charger circuit is included to provide a fast tuning as well as low noise performance. As a result of this, MB15B03 is ideally suitable for digital mobile communications, such as GSM.

■ FEATURES

- High frequency operation RF synthesizer : 1.1GHz max.
  IF synthesizer : 300MHz max.
- Low power supply voltage: V_{CC} = 2.7 to 3.6V
- Very low power supply current : I_{CC} = 10 mA typ. (V_{CC} = 3V)
- Power saving function : I_{PS1} = I_{PS2} = 100 µA typ. (V_{CC} = 3V)
- Serial input 14-bit programmable reference counter: R = 6 to 16,383
- Serial input 18-bit programmable divider consisting of:
  - Binary 7-bit swallow counter: 0 to 127
  - Binary 11-bit programmable counter: 5 to 2,047
- On-chip high performance charge pump circuit and phase comparator, achieving high-speed lock-up and low phase noise
- Wide operating temperature: Ta = −40 to 85°C
- Plastic 16-pin SSOP package (FPT-16P-M05)

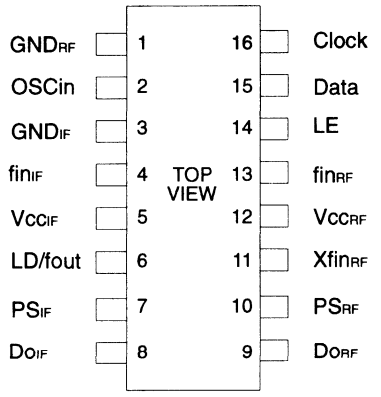
■ PACKAGE

16-pin, Plastic SSOP



(FPT-16P-M05)

■ PIN ASSIGNMENT

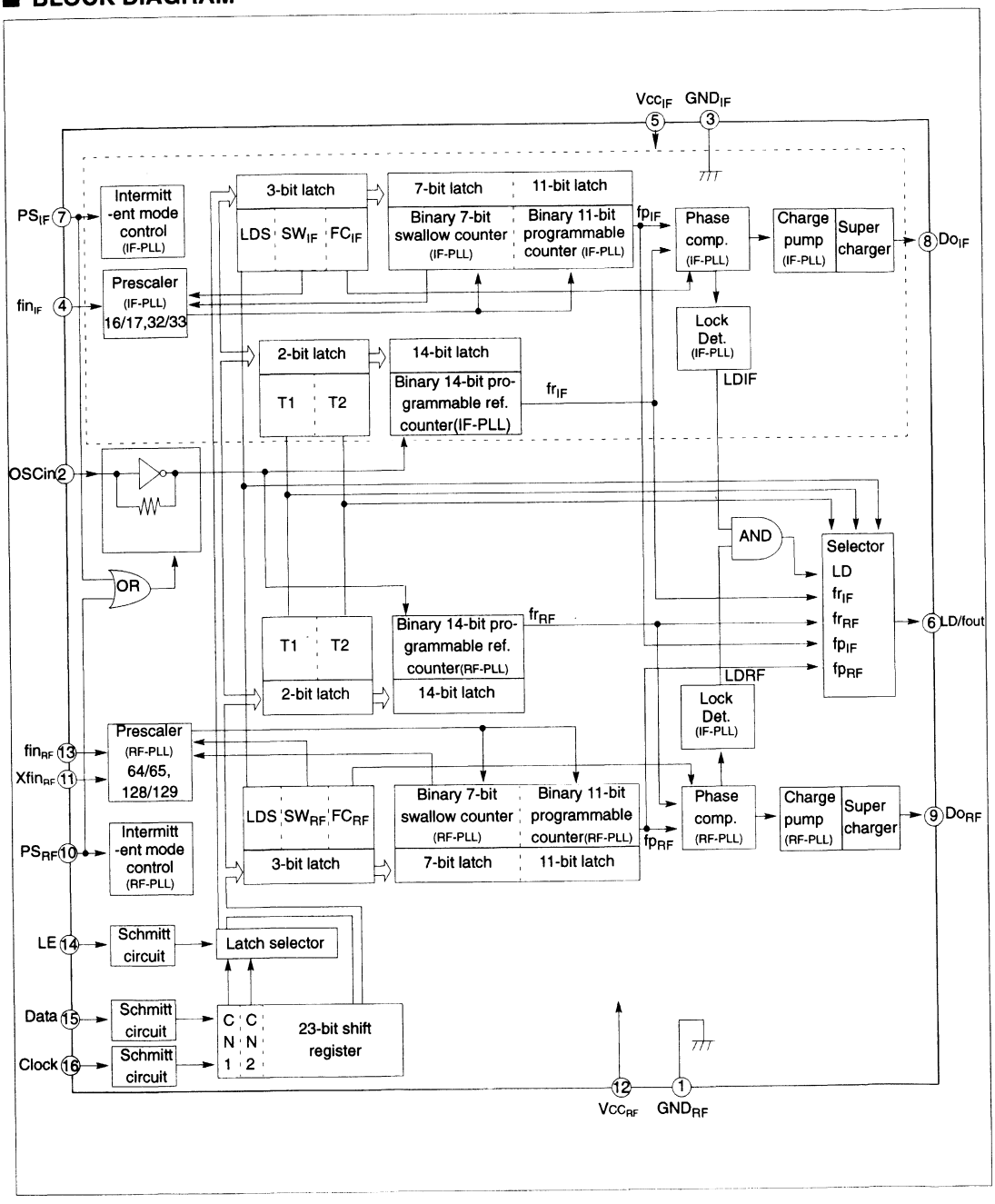


(FPT-16P-M05)

■ PIN DESCRIPTIONS

Pin No.	Pin name	I/O	Descriptions
1	V_{CC}	–	Ground for RF-PLL section.
2	OSCin	I	The programmable reference divider input. TCXO should be connected with a coupling capacitor.
3	GND_{IF}	–	Ground for the IF section.
4	fin_{IF}	I	Prescaler input pin for the IF-PLL. The connection with VCO should be AC coupling.
5	Vcc_{IF}	–	Power supply voltage input pin for the IF-PLL section. When power is OFF, latched data of the IF-PLL is cancelled.
6	LD/fout	O	Lock detect signal output (LD) / phase comparator monitoring output (fout) The output signal is selected by a LDS bit in a serial data. LDS bit = "H" ; outputs fout signal LDS bit = "L" ; outputs LD signal
7	PS_{IF}	I	Power saving mode control for the IF-PLL section. This pin must be set at "L" at Power-ON. (Open is prohibited.) PS_{IF} = "H" ; Normal mode PS_{IF} = "L" ; Power saving mode
8	Do_{IF}	O	Charge pump output for the IF-PLL section. Phase characteristics of the phase comparator can be reversed by the FC-bit.
9	Do_{RF}	O	Charge pump output for the RF-PLL section. Phase characteristics of the phase comparator can be reversed by the FC-bit.
10	PS_{RF}	I	Power saving mode control for the RF-PLL section. This pin must be set at "L" at Power-ON. (Open is prohibited.) PS_{RF} = "H" ; Normal mode PS_{RF} = "L" ; Power saving mode
11	$Xfin_{RF}$	I	Prescaler complimentary input for the RF-PLL section. This pin should be grounded via a capacitor.
12	Vcc_{RF}	–	Power supply voltage input pin for the RF-PLL section, the shift register and the oscillator input buffer. When power is OFF, latched data of RF-PLL is cancelled.
13	fin_{RF}	I	Prescaler input pin for the RF-PLL. The connection with VCO should be AC coupling.
14	LE	I	Load enable signal input (with the schmitt trigger circuit.) When LE is "H", data in the shift register is transferred to the corresponding latch according to the control bit in a serial data.
15	Data	I	Serial data input (with the schmitt trigger circuit.) A data is transferred to the corresponding latch (IF-ref counter, IF-Prog. counter, RF-ref. counter, RF-prog. counter) according to the control bit in a serial data.
16	Clock	I	Clock input for the 23-bit shift register (with the schmitt trigger circuit.) One bit data is shifted into the shift register on a riging edge of the clock.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Remark
Power supply voltage	V_{CC}	−0.5 to +5.0	V	
Output voltage	V_{OUT}	−0.5 to V_{CC} +0.5	V	
Output current	I_{OUT}	±10	mA	
Storage temperature	T_{STG}	−55 to +125	°C	

Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Note
		Min	Typ	Max		
Power supply voltage	Vcc	2.7	3.0	3.6	V	Vcc_{IF} = Vcc_{RF}
Input voltage	Vi	GND	–	V_{CC}	V	
Operating temperature	Ta	−40	–	+85	°C	

Handling Precautions

- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover workbenches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

■ ELECTRICAL CHARACTERISTICS

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Power supply current *1		Icc_{IF}	fin_{IF} = 300MHz, fosc = 12MHz	–	3.5	4.6	mA
		Icc_{RF}	fin_{RF} = 1100MHz, fosc = 12MHz	–	6.5	8.5	
Power saving current *2		Ips_{IF}	Vcc_{IF} current at PS_{IF} ="L"	–	100	–	µA
		Ips_{RF}	Vcc_{RF} current at $PS_{IF/RF}$ ="L"	–	100	–	
Operating frequency	fin_{IF}	fin_{IF}	IF-PLL	50	–	300	MHz
	fin_{RF}	fin_{RF}	RF-PLL	100	–	1100	
	OSCin	f_{OSC}	min. 500mVp-p	–	12.8	23	
Input sensitivity	fin_{IF}	$Vfin_{IF}$	IF-PLL, 50Ω termination (Refer to the test circuit.)	–10	–	+2	dBm
	fin_{RF}	$Vfin_{RF}$	RF-PLL, 50Ω termination (Refer to the test circuit.)	–10	–	+2	dBm
	OSCin	V_{OSC}		500	–	–	mVp-p
Input voltage	Data, Clock, LE, PS	V_{IH}		Vcc×0.7 +0.4	–	–	V
		V_{IL}		–	–	Vcc×0.3 –0.4	
Input current	Data, Clock, LE, PS	I_{IH}		–	–	+1.0	µA
		I_{IL}		–1.0	–	–	
	OSCin	OSCin		–100	–	+100	
Output voltage	LD	V_{OH}	Vcc = 3.0V, I_{OH} = –1.0mA	2.2	–	–	V
		V_{OL}	Vcc = 3.0V, I_{OL} = 1.0mA	–	–	0.4	
High impedance cutoff current	Do	I_{OFF}		–	–	0.3	µA
Output current	LD	I_{OH}	Vcc = 3.0V	–1.0	–	–	mA
		I_{OL}	Vcc = 3.0V	–	–	1.0	
	Do	I_{DOH}	Vcc = 3.0V, V_{DOH} = 2.0V, Ta = 25°C	–12	–	–3.5	mA
		I_{DOL}	Vcc = 3.0V, V_{DOL} = 1.0V Ta = 25°C	6	–	18	

*1: Conditions ; $Vcc_{IF/RF}$ = 3V, Ta = 25°C, in locking state.

*2: Conditions ; $Vcc_{IF/RF}$ = 3V, Ta = 25°C, in power saving state.

■ FUNCTIONAL DESCRIPTIONS

The divide ratio can be calculated using the following equation:

$f_{VCO} = \{(P \times N) + A\} \times f_{OSC} \div R \quad (A < N)$

f_{VCO}: Output frequency of external voltage controlled ocillator (VCO)
P: Preset divide ratio of dual modulus prescaler (16 or 32 for IF-PLL, 64 or 128 for RF-PLL)
N: Preset divide ratio of binary 11-bit programmable counter (5 to 2,047)
A: Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$)
f_{OSC}: Reference oscillation frequency
R: Preset divide ratio of binary 14-bit programmable reference counter (6 to 16,383)

Serial Data Input

Serial data is entered using three pins, Data pin, Clock pin, and LE pin. Programmable dividers of IF/RF-PLL sections, programmable reference dividers of IF/RF PLL sections are controlled individually.
Serial data of binary data is entered through Data pin.
On rising edge of clock, one bit of serial data is transferred into the shift register. When load enable signal is high, the data stored in the shift register is transferred to one of latch of them depending upon the control bit data setting.

Table.1 Control Bit

Control bits		Destination of serial data
CN1	CN2	
L	L	The programmable reference counter for the IF-PLL.
H	L	The programmable reference counter for the RF-PLL.
L	H	The programmable counter and the swallow counter for the IF-PLL
H	H	The programmable counter and the swallow counter for the RF-PLL

Shift Register Configuration

Programmable Reference Counter

LSB ↓ Data Flow → MSB ↓

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
CN1	CN2	T1	T2	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14

CNT1, 2 : Control bit (Table. 1)
R1 to R14 : Divide ratio setting bits for the programmable reference counter (6 to 16,383) (Table. 2)
T1, 2 : Test purpose bit (Table. 3)

Programmable Counter

LSB ↓ Data Flow → MSB ↓

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
CN1	CN2	LDS	SW	FC	A1	A2	A3	A4	A5	A6	A7	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11

CN1, 2	: Control bit	(Table. 1)
N1 to N11	: Divide ratio setting bits for the programmable counter (5 to 2,047)	(Table. 4)
A1 to A7	: Divide ratio setting bits for the swallow counter (0 to 127)	(Table. 5)
SW	: Divide ratio setting bit for the prescaler	(Table. 6)
	(16/17 or 32/33 for the IF-PLL, 64/65 or 128/129 for the RF-PLL)	
FC	: Phase control bit for the phase detector	(Table. 7)
LDS	: LD/fout signal select bit	(Table. 8)

Table.2 Binary 14-bit Programmable Reference Counter Data Setting

Divide Ratio (R)	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1
6	0	0	0	0	0	0	0	0	0	0	0	1	1	0
7	0	0	0	0	0	0	0	0	0	0	0	1	1	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: • Divide ratio less than 6 is prohibited.

Table.3 Test Purpose Bit Setting

T1	T2	LD/fout pin state
L	L	Outputs fr_{IF}
H	L	Outputs fr_{RF}
L	H	Outputs fp_{IF}
H	H	Outputs fp_{RF}

Table.4 Binary 11-bit Programmable Counter Data Setting

Divide Ratio (N)	N 11	N 10	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1
5	0	0	0	0	0	0	0	0	1	0	1
6	0	0	0	0	0	0	0	0	1	1	0
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

Note: • Divide ratio less than 5 is prohibited.

Table.5 Binary 7-bit Swallow Counter Data Setting

Divide Ratio (N)	A 7	A 6	A 5	A 4	A 3	A 2	A 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

Note: • Divide ratio (A) range = 0 to 127

Table.6 Prescaler Data Setting

		SW = "H"	SW = "L"
Prescaler divide ratio	IF-PLL	16/17	32/33
	RF-PLL	64/65	128/129

Table.7 Phase Comparator Phase Switching Data Setting

	FC = H	FC = L
fr > fp	H	L
fr = fp	Z	Z
fr < fp	L	H
VCO Polarity	①	②

Note: •Z = High-impedance
•Depending upon the VCO and LPF polarity, FC bit should be set.

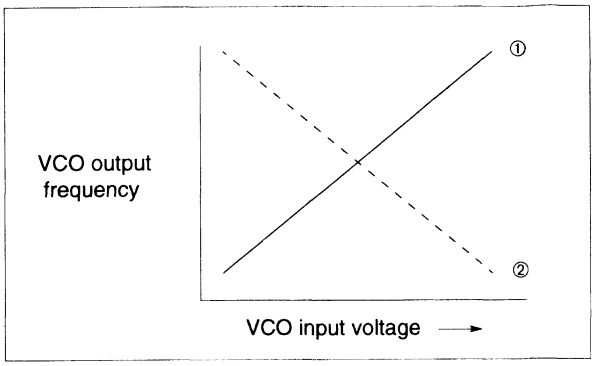
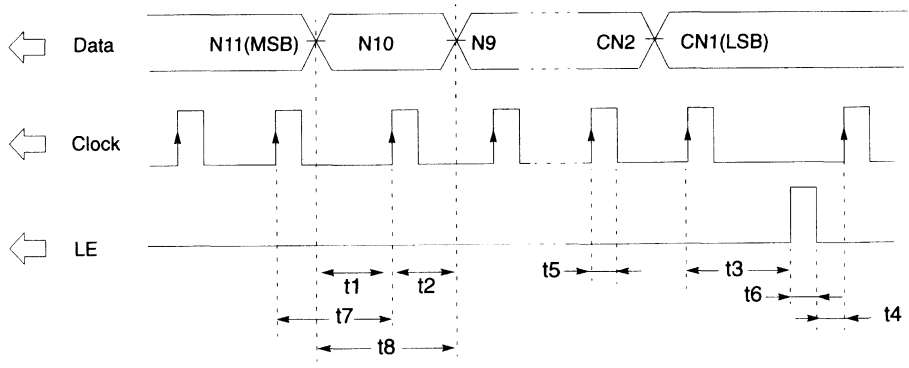


Table.8 LD/fout Output Select Data Setting

LDS	LD/fout output signal
H	fout ($fr_{IF/RF}$, $fp_{IF/RF}$) signals
Z	LD signal

Serial Data Input Timing

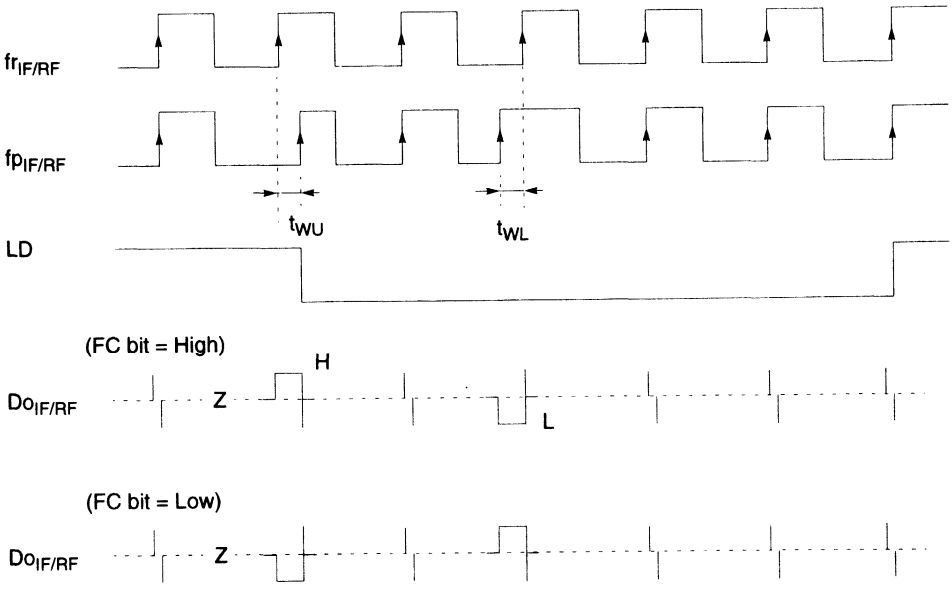


On rising edge of the clock, one bit of the data is transferred into the shift register.

Parameter	Min.	Typ.	Max.	Unit
t1	30	–	–	ns
t2	30	–	–	ns
t3	30	–	–	ns
t4	30	–	–	ns

Parameter	Min.	Typ.	Max.	Unit
t5	100	–	–	ns
t6	100	–	–	ns
t7	200	–	–	ns
t8	200	–	–	ns

■ PHASE DETECTOR OUTPUT WAVEFORM



LD Output Logic Table

IF-PLL section	RF-PLL section	LD output
Locking state / Power saving	Locking state / Power saving	H
Locking state / Power saving	Unlocking state	L
Unlocking state	Locking state / Power saving	L
Unlocking state	Unlocking state	L

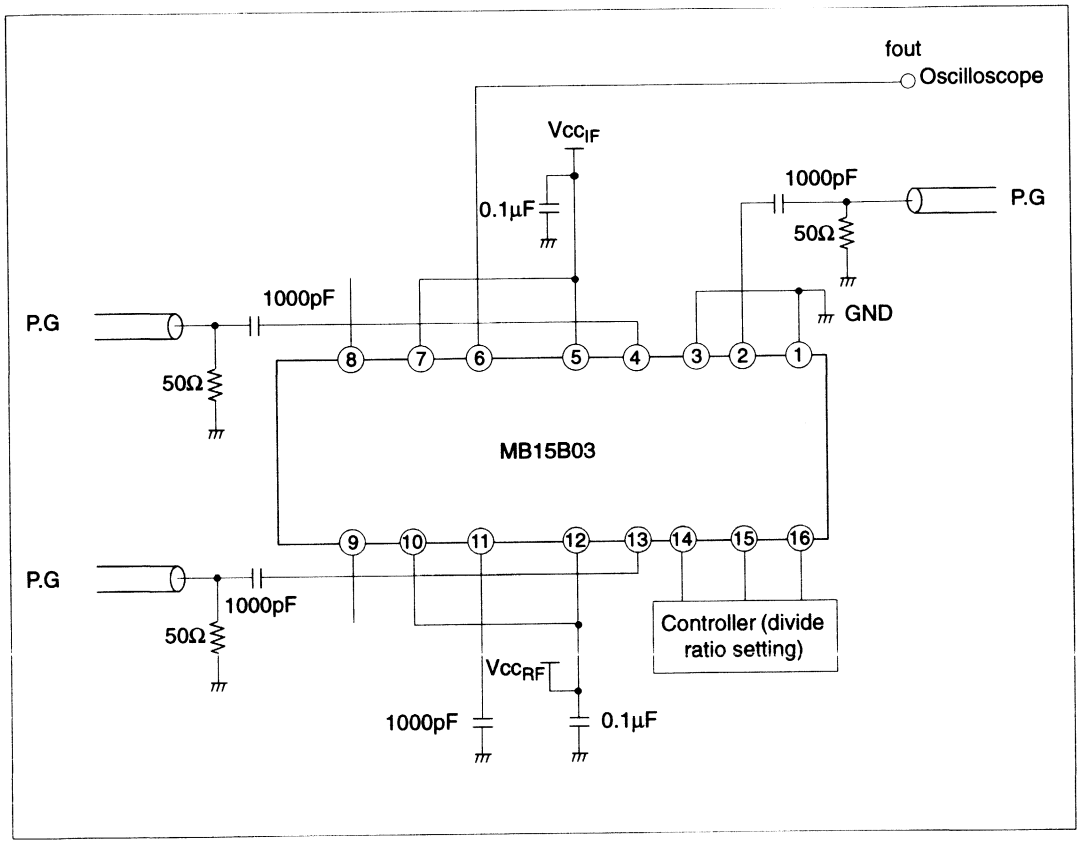
Note: • Phase error detection range = -2π to $+2\pi$
• Pulses on $Do_{IF/RF}$ signals are output to prevent dead zone.
• LD output becomes low when phase error is t_{WU} or more.
• LD output becomes high when phase error is t_{WL} or less and continues to be so for three cycles or more.
• t_{WU} and t_{WL} depend on OSCin input frequency as follows.
$t_{WU} \geq 8/fosc$: i.e. $t_{WU} \geq 625ns$ when foscin = 12.8 MHz
$t_{WL} \leq 16/fosc$: i.e. $t_{WL} \leq 1250ns$ when foscin = 12.8 MHz

Power Saving Mode (Intermittent mode control circuit)

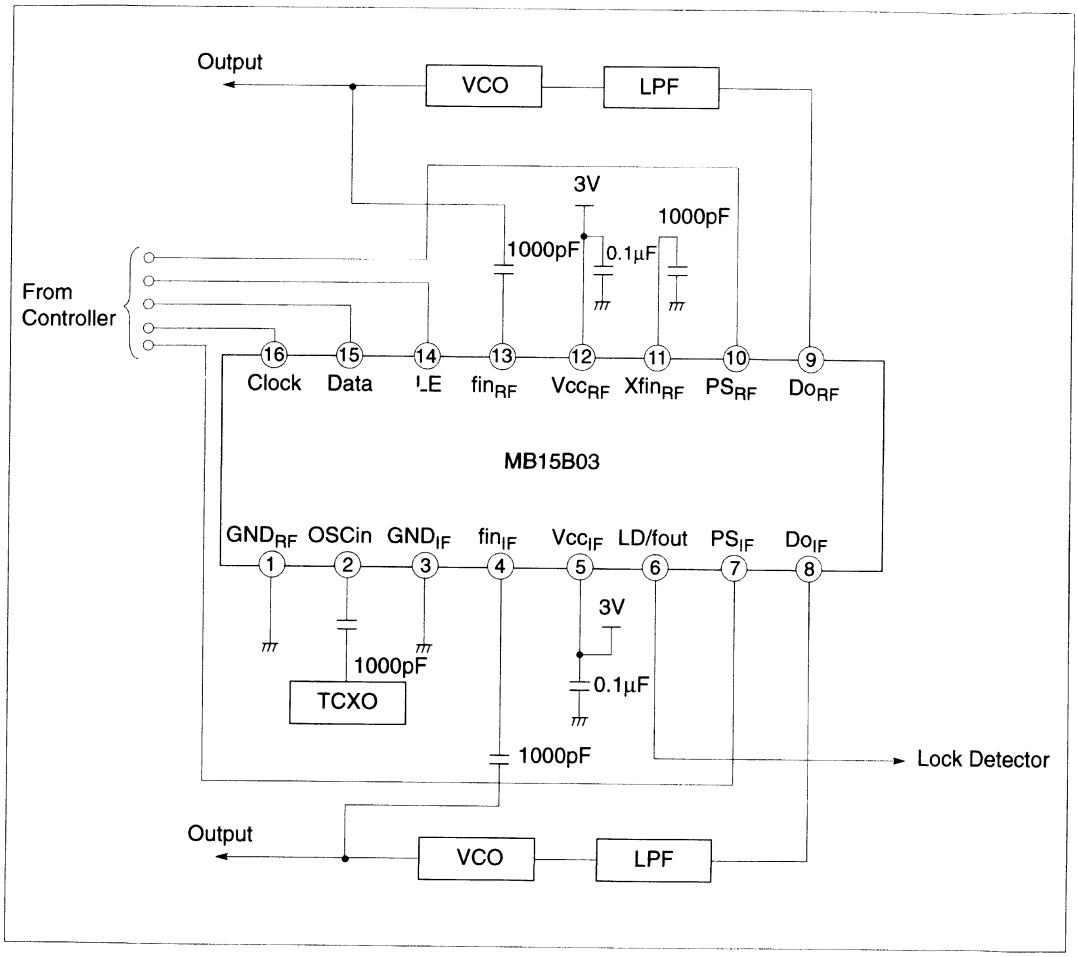
Setting a $PS_{IF(RF)}$ pin to Low, IF-PLL(RF-PLL) enters into power saving mode resultatly current consumption can be limited to 100μA (typ.). Setting PS pin to High, power saving mode is released so that the device works normally.
In addition, the intermittent operation control circuit is included which helps smooth start up from stand by mode.
In general, the power consumption can be saved by the intermittent operation that powering down or waking up the synthesizer. Such case, if the PLL is powered up uncontrolled, the resulting phase comparator output signal is unpredictable due to an undefined phase relation between reference frequency (f_r) and comparison frequency (f_p) and may in the worst case take longer time for lock up of the loop.
To prevent this, the intermittent operation control circuit enforces a limited error signal output of the phase detector during power up, thus keeping the loop locked.
PS pin must be set "L" at Power-ON.
During the power saving mode, the corresponding section except for indispensable circuit for the power saving function stops working, then current consumption is reduced to 100μA per one PLL section.
At that time, the Do and LD become the same state as when a loop is locking. That is, the Do becomes high impedance.
A VCO control voltage is naturally kept at the locking voltage which defined by a LPF's time constant. As a result of this, VCO's frequency is kept at the locking frequency.

PS_{IF}	PS_{RF}	IF-PLL counters	RF-PLL counters	OSC input buffer
L	L	OFF	OFF	OFF
H	L	ON	OFF	ON
L	H	OFF	ON	ON
H	H	ON	ON	ON

■ TEST CIRCUIT (Prescaler Input/Programmable Reference Divider Input SensitivityTest)



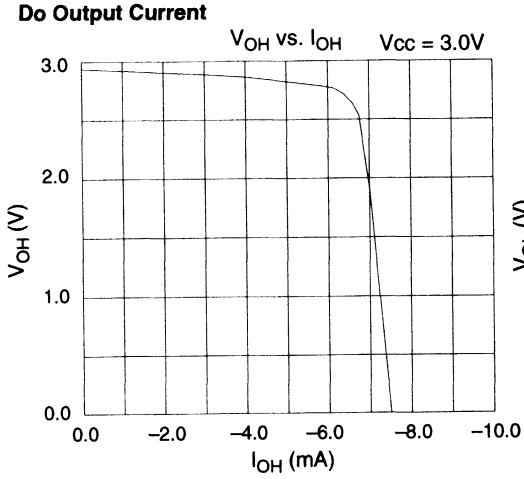
■ APPLICATION EXAMPLE

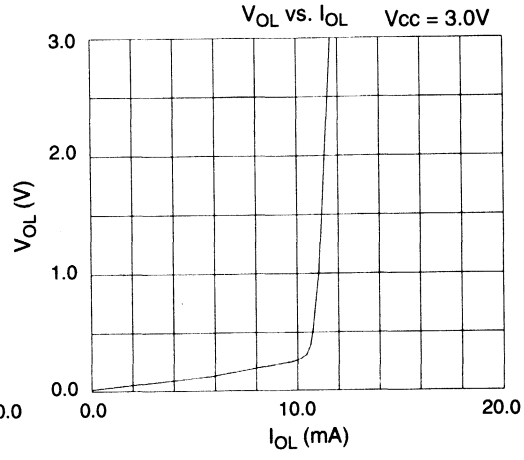


Note: Clock, Data, LE : Involves a schmitt circuit.
(When inputs are open, pull up/down resistor is necessary to prevent self-oscillation.)

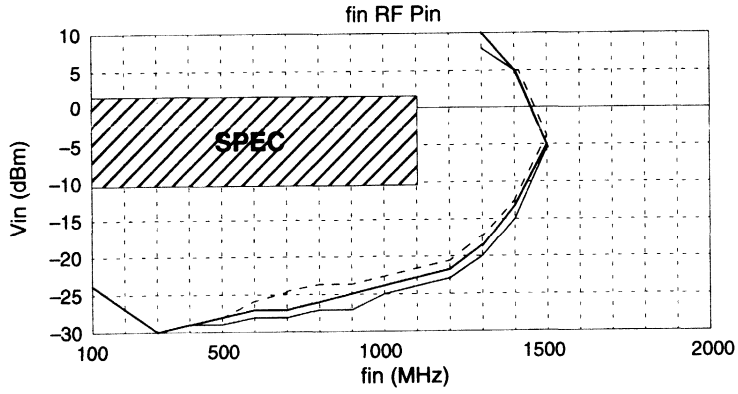
■ TYPICAL CHARACTERISTICS

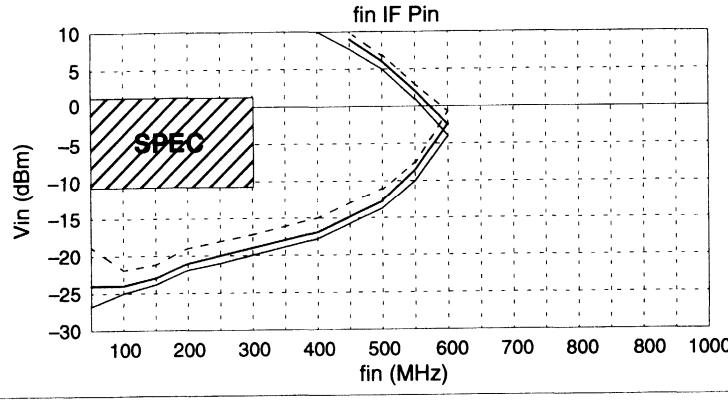
Do Output Current





fin Input Sensitivity





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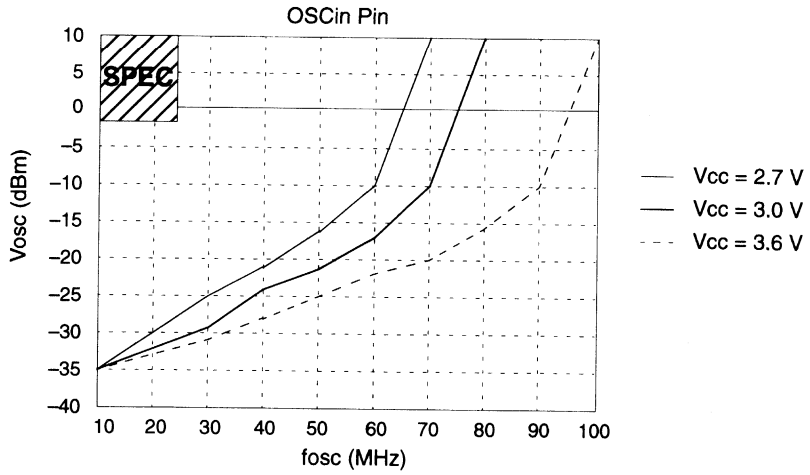
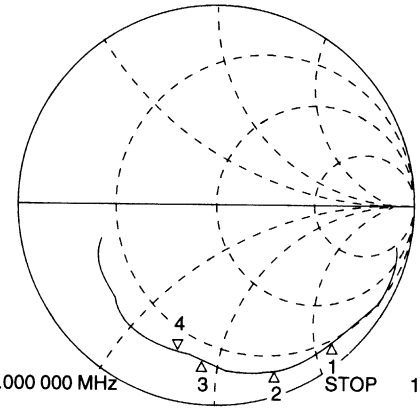
OSCin Input Sensitivity

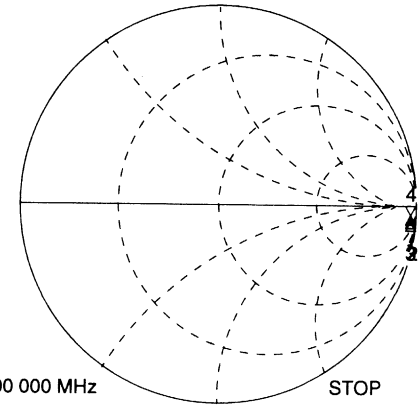


Input Impedance

fin_{RF} Pin



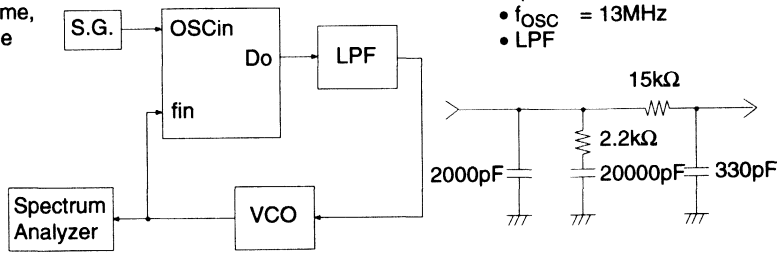
OSCin Pin



■ REFERENCE INFORMATION

Typical plots measured with the test circuit are shown below.
Each plots show lock up time, phase noise, and reference leakage.

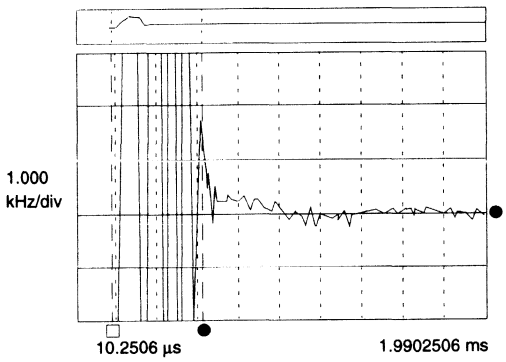
Test Circuit

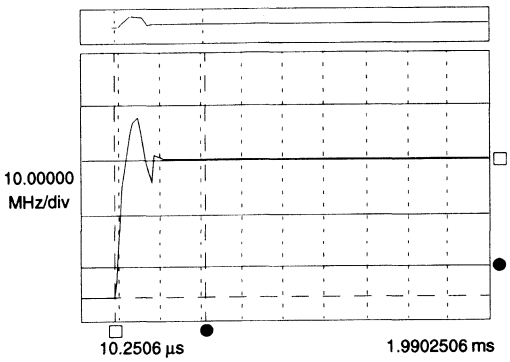


- f_{VCO} = 1018MHz
- K_V = 20MHz/V
- f_r = 200kHz
- f_{OSC} = 13MHz
- LPF

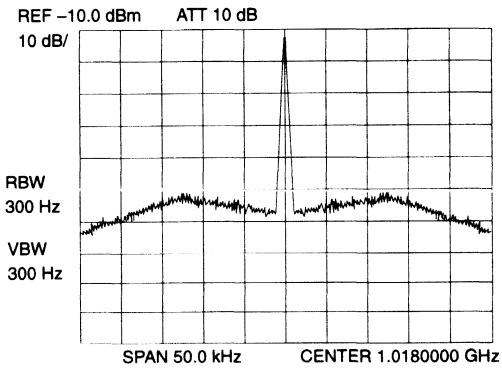
PLL Lock Up Time

1005.000MHz → 1031.000MHz, within ± 1kHz
Lch → Hch 420µs

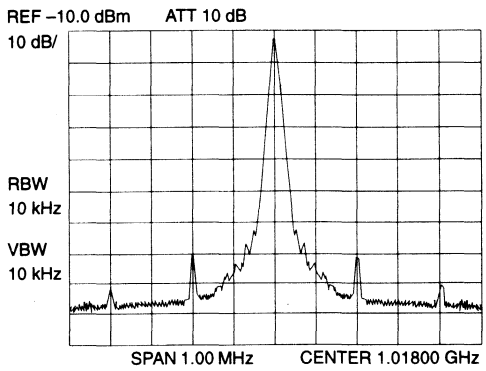




PLL Phase Noise
@ within loop band = 74dBc/Hz



PLL Reference Leakage
@ 200kHz offset = 68dBc



■ ORDERING INFORMATION

Part number	Package	Remarks
MB15B03PFV	16-pin, Plastic SSOP (FPT-16P-M05)	

FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-21331-1E

ASSP for DTS

Bi-CMOS

1.1 GHz/400 MHz PLL Frequency Synthesizer

MB15B11

■ DESCRIPTION

The MB15B11 is a pulse swallow PLL (Phase Locked Loop) frequency synthesizer LSI. The MB15B11 has dual PLLs, for the 1.1 GHz and 400 MHz bands respectively, and is optimized for systems using IF modulation such as analog cellular.
With a supply voltage of 3 V (Typ.) and supply current of 9.5 mA (Typ.), the device enables equipment to operate with low power consumption.

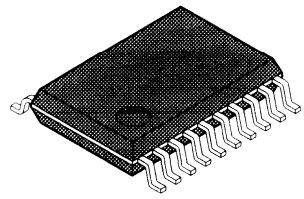
■ FEATURES

- Dual internal pulse swallow PLLs
  PLL 1: 400 MHz band
  PLL 2: 1.1 GHz band
- Division ratio set by serial input
  Reference divider: Binary 14-bit reference counter (divide by 8 to 16,383)
  Programmable divider: 1.1 GHz band prescaler (64/65, 128/129), 400 MHz band prescaler (32/33, 64/65)
  Division ratio of the binary 7-bit swallow counter (0 to 127)
  Division ratio of the binary 11-bit programmable counter (16 to 2,047)
  * The programmable dividers for PLL1 and PLL2 can be set independently.
- Low voltage operation: 2.7 V to 3.5 V
  The charge pump section uses a separate supply (up to 6.0 V).
- Low current consumption: 9.5 mA (Typ.)

(Continued)

■ PACKAGE

20-pin, Plastic SSOP

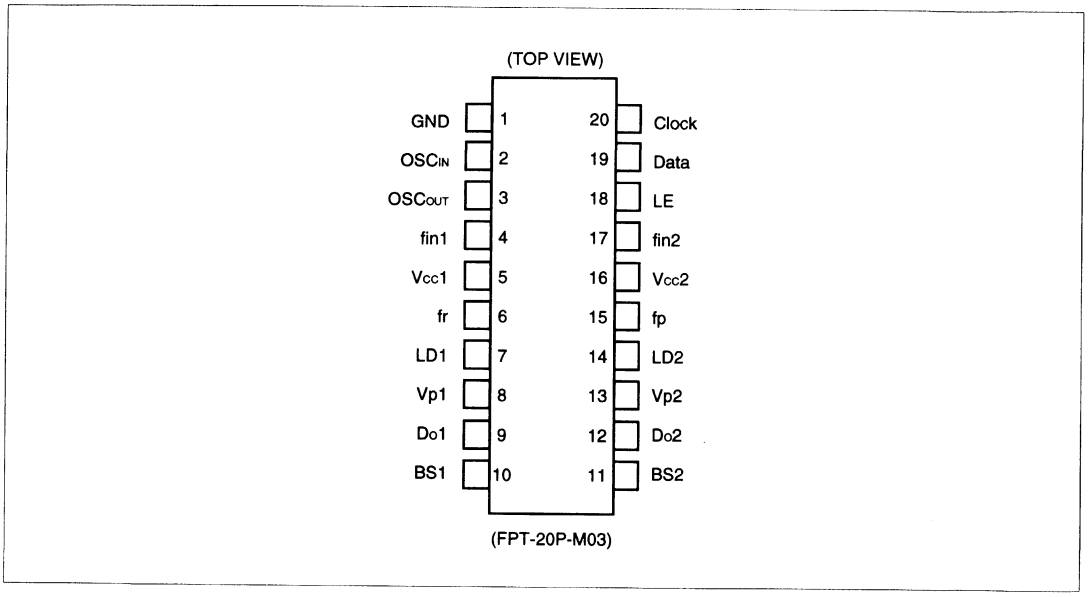


(FPT-20P-M03)

(Continued)

- Built-in power saving function
  Power saving current: PLL1 = 100 µA, PLL2 = 100 µA
- Charge pump characteristics based on application
  Separate internal charge pumps are provided for transmit and receive operation.
  Transmit (PLL1): Low sensitivity charge pump (for ease of modulation)
  Receive (PLL2): High sensitivity charge pump (enables fast lockup time)
- Internal analog switch
  An internal analog switch is provided to achieve a faster PLL lockup time.
- Phase comparator supports phase conversion
- Wide operating temperature range: Ta = −30°C to +80°C

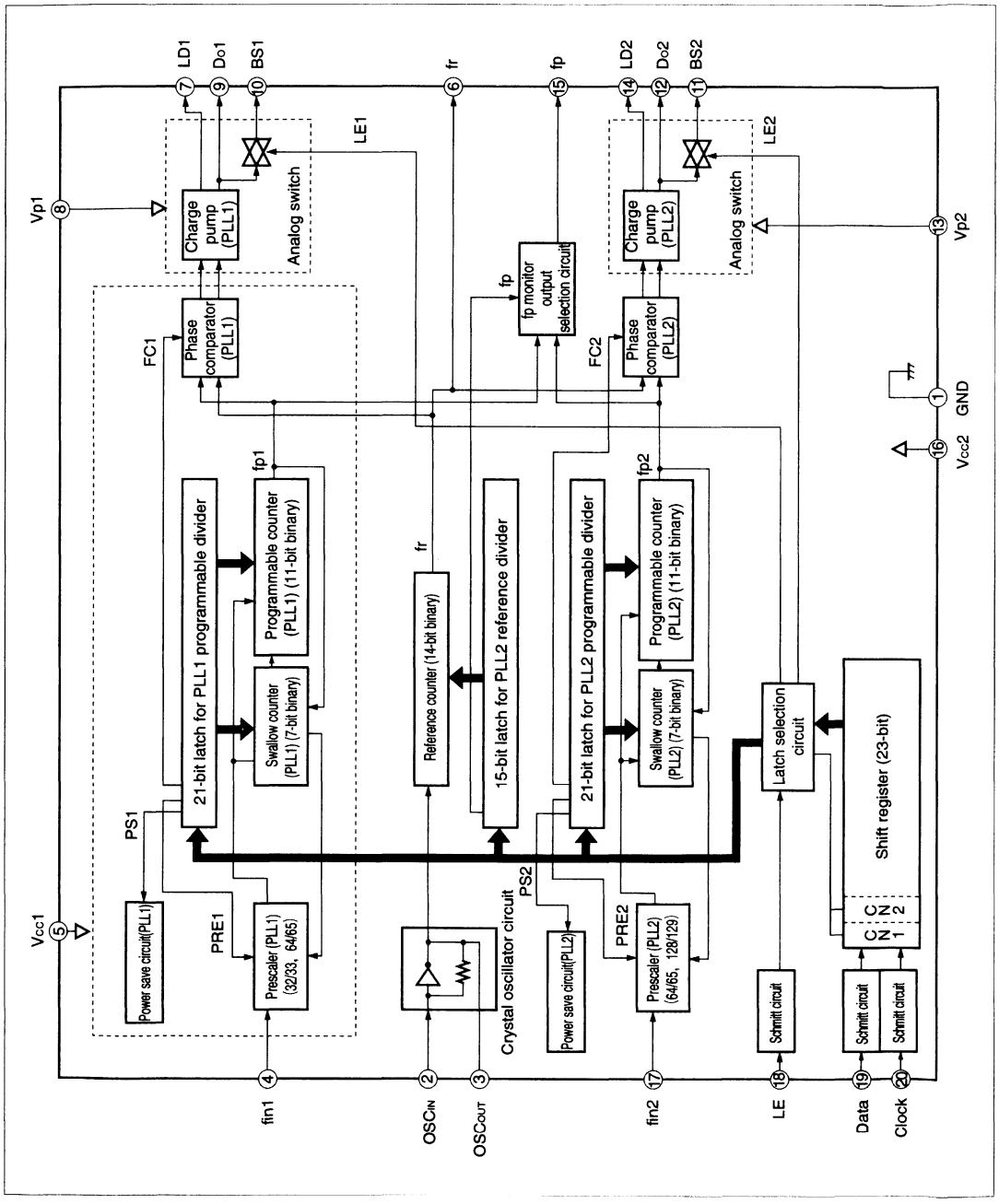
■ PIN ASSIGNMENT



■ PIN DESCRIPTIONS

Pin No.	Symbol	I/O	Function
1	GND	—	Ground.
2	OSC_{IN}	I	Crystal oscillator connection pins and reference divider input pins (OSC_{IN} = oscillator circuit input pin, OSC_{OUT} = oscillator circuit output pin).
3	OSC_{OUT}	O	
4	fin_1	I	PLL1 prescaler input pin. The input should be AC coupled.
5	V_{CC1}	—	PLL1 supply pin. The PLL1 latch data is lost when the power is off.
6	fr	O	Output monitor pin for the reference divider.
7	LD_1	O	Lock detect output pin for PLL1. LD = "H" when locked and LD = "L" when unlocked.
8	V_{P1}	—	Power supply pin for the PLL1 charge pump output and analog switch output.
9	D_{O1}	O	PLL1 charge pump output pin. The FC bit in the data inverts the phase characteristics.
10	BS_1	O	PLL1 analog switch output pin. When the switch is on (when the LE pin = "H"), this pin outputs the charge pump state. Otherwise stays at high impedance.
11	BS_2	O	PLL2 analog switch output pin. When the switch is on (when the LE pin = "H"), this pin outputs the charge pump state. Otherwise stays at high impedance.
12	D_{O2}	O	PLL2 charge pump output pin. The FC bit in the data inverts the phase characteristics.
13	V_{P2}	—	Power supply pin for the PLL2 charge pump output and analog switch output.
14	LD_2	O	Lock detect output pin for PLL2. LD = "H" when locked and LD = "L" when unlocked.
15	fp	O	Compare divider monitor output pin. The FP bit setting in the data selects between outputting the PLL1 or PLL2 division output. When the FP bit = "H", outputs for PLL1 (fp1) When the FP bit = "L", outputs for PLL2 (fp2)
16	V_{CC2}	—	Supply pin for PLL2, reference divider, shift register, and crystal oscillator circuit. The PLL2 and reference counter latch data is lost when the power is off.
17	fin_2	I	PLL2 prescaler input pin. The input should be AC coupled.
18	LE	I	Input pin for the load enable signal (with Schmitt trigger circuit). When LE = "H", the contents of the shift register are moved to the latches specified by the serial data control bit values. At the same time, the internal analog switch turns on and the charge pump output signals are output from the BS pins.
19	Data	I	Serial data input pin (with Schmitt trigger circuit). The data move destination (reference divider, PLL1 programmable divider, or PLL2 programmable divider) is selected by the data's control bit values.
20	Clock	I	Clock input pin for the 23-bit shift register (with Schmitt trigger circuit). Data is read on the rising edge of clock pulses.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	−0.5	+5.0	V	
	V_P	V_{CC}	7.0	V	
Output voltage	V_O	−0.5	V_{CC} + 0.5	V	
Output current	I_O	−10	+10	mA	
Storage temperature	Tstg	−55	+125	°C	

Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
Power supply voltage	V_{CC}	2.7	3.0	3.5	V	$V_{CC}1 = V_{CC}2$
	V_P	V_{CC}	—	6.0	V	
Input voltage	V_I	GND	—	V_{CC}	V	
Operating temperature	Ta	−30	—	+80	°C	

Handling Precautions

- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover workbenches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

■ ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.7 V to 3.5 V, Ta = −30°C to +80°C)

Parameter		Symbol	Value			Unit	Remarks
			Min.	Typ.	Max.		
Power supply current		I_{CC1}	—	3.5 (0.1)	—	mA	PLL1, V_{CC} = 3.0 V, Ta = 25°C, PLL locked Figures in parentheses ( ) are for power saving mode.
		I_{CC2}	—	6.0 (0.1)	—	mA	PLL2, V_{CC} = 3.0 V, Ta = 25°C, PLL locked Figures in parentheses ( ) are for power saving mode.
Operating frequency	fin1	fin1	100	—	400	MHz	PLL1, 1000 pF, AC coupled
	fin2	fin2	100	—	1100	MHz	PLL2, 1000 pF, AC coupled
	OSC_{IN}	fosc	—	12.8	20.0	MHz	
Input sensitivity	fin1	V_{fin1}	−10	—	4	dBm	PLL1, 50 Ω, AC coupled
	fin2	V_{fin2}	−10	—	4	dBm	PLL2, 50 Ω, AC coupled
	OSC_{IN}	V_{OSC}	0.5	—	—	V_{P-P}	
Input voltage	Other than fin, OSC_{IN}	V_{IH}	0.7 × V_{CC}+0.4		—	V	
		V_{IL}	—	—	0.3 × V_{CC}−0.4	V	
Input current	Data, Clock LE	I_{IH}	—	1.0	—	µA	
		I_{IL}*	—	−1.0	—	µA	
	OSC_{IN}	I_{OSC}	—	±50	—	µA	
Output voltage	Other than D_O, OSC_{OUT}	V_{OH}	2.2	—	—	V	V_{CC} = 3.0 V
		V_{OL}	—	—	0.4	V	
High impedance cut-off current	D_O, BS	I_{OFF}	—	—	1.1	µA	V_P = V_{CC} to 6.0 V V_{OOP} = GND to 6.0 V
Output current	Other than D_O, OSC_{OUT}	I_{OH}*	−1.0	—	—	mA	
		I_{OL}	1.0	—	—	mA	
	D_{O1}	I_{OH1}*	—	−1	—	mA	V_P = 6.0 V, Ta = 25°C, V_{OH1} = 5 V
		I_{OL1}	—	12	—	mA	V_{CC} = 3.0 V, Ta = 25°C, V_{OL1} = 1 V
	D_{O2}	I_{OH2}*	—	−3	—	mA	V_P = 6.0 V, Ta = 25°C, V_{OH2} = 5 V
		I_{OL2}	—	6	—	mA	V_{CC} = 3.0 V, Ta = 25°C, V_{OL2} = 1 V
Analog switch on resistance		R_{ON}	—	50	—	Ω	

* : A minus sign indicates the current is flowing out of the device.

■ FUNCTION DESCRIPTION

1. Pulse Swallow Function

The divide ratio can be calculated using the following equation:

$$f_{VCO} = [(P \times N) + A] \times f_{OSC} \div R$$

f_{VCO}	:	Output frequency of external voltage controlled oscillator (VCO)
N	:	Preset divide ratio of binary 11-bit programmable counter (16 to 2,047)
A	:	Preset divide ratio of binary 7-bit swallow counter (0 to 127, and A < N)
f_{OSC}	:	Reference oscillation frequency (OSC_{IN} input frequency)
R	:	Preset divide ratio of reference counter (8 to 16,383)
P	:	Prescaler divide ratio. PLL1 (32 or 64) / PLL2 (64 or 128)

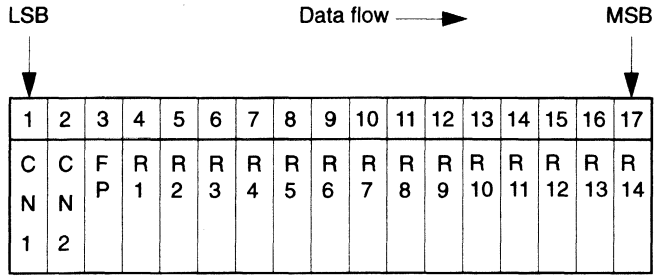
2. Serial Data Input

Serial data is entered using three pins, Data pin, Clock pin, and LE pin. Reference divider, PLL1 programmable divider, and PLL2 programmable divider are controlled individually.
Serial data of binary data is entered through Data pin.
On rising edge of clock, one bit of serial data is transferred into the shift register. When load enable signal is high, the data stored in the shift register is transferred to one of latch of them depending upon the control bit data setting.

Control data	Reference counter	PLL1 programmable counter	PLL2 programmable counter
CN1	L	L	H
CN2	L	H	H

(1) Shift register configuration

Programmable Reference Counter



R1 to R14	:	Divide ratio setting bits for the programmable reference counter (8 to 16,383)
FP	:	Test purpose bit (selects fp1 or fp2 monitor output)
CN1, 2	:	Control bits

Note: Data input with MSB first.

(Continued)

(Continued)

Programmable Counter

LSB → Data flow → MSB

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
CN1	CN2	PS	PRE	FC	A1	A2	A3	A4	A5	A6	A7	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11

N1 to N11 : Divide ratio setting bits for the programmable counter (16 to 2,047)
A1 to A7 : Divide ratio setting bits for the swallow counter (0 to 127)
FC : Phase switching bit for the phase comparator
PRE : Prescaler divide ratio setting bit
PS : Power saving control bit
CN1, 2 : Control bits

Note: Data input with MSB first.

(2) Data setting

• Binary 14-bit reference counter

Divide ratio (R)	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1
8	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	1	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•

Note: Divide ratio less than 8 is prohibited. (Setting range = 8 to 16,383)

• Binary 11-bit programmable counter

Divide ratio (N)	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1
16	0	0	0	0	0	0	1	0	0	0	0
17	0	0	0	0	0	0	1	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•

Note: Divide ratio less than 16 is prohibited. (Setting range = 16 to 2,047)

• Binary 7-bit swallow counter setting

Divide ratio (A)	A7	A6	A5	A4	A3	A2	A1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•

(Setting range = 0 to 127)

• PRE: Prescaler divide ratio setting

	PRE = "H"	PRE = "L"
PLL1 prescaler divide ratio	Divide by 32/33	Divide by 64/65
PLL2 prescaler divide ratio	Divide by 64/65	Divide by 128/129

Note: PLL1 and PLL2 are set from the serial data when setting their respective programmable divide ratios.

• PS: Power saving control

	PS = "H"	PS = "L"
PLL1	ON	OFF
PLL2/common circuits	ON	OFF

Notes: • PLL1 and PLL2 are set from the serial data when setting their respective compare divider values.
• The common circuits are the crystal oscillator circuit and reference counter.
• Set PS = "L" once when turning on the power.

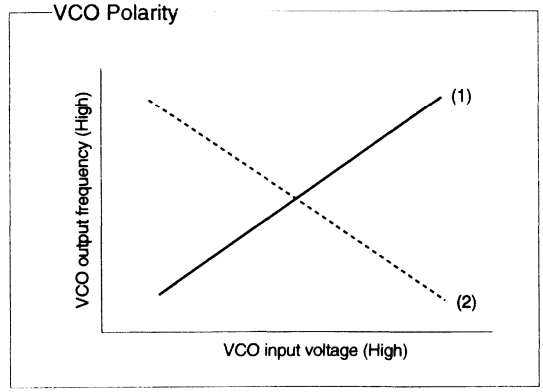
Intermittent operation reduces the overall circuit power consumption by only operating the internal circuit when required (the circuit halts when not required). However, simply switching the circuit from the halted to the operating state will result in a large error signal output from the phase comparator. This is because the phase relationship between the reference frequency (fr) and compare frequency (fp) inputs to the phase comparator is undefined during such a startup condition, even if the two frequencies are the same. As a result, the PLL will lose its locked state. To prevent this problem, an intermittent operation control circuit is provided to forcibly align the phases on startup and therefore minimize the variation in the locked frequency.

• FC: Phase switching bit for the phase comparator
Sets the charge pump output polarity (D_O) as follows.

	FC = "H"	FC = "L"
fr > fp	H	L
fr < fp	L	H
fr =fp	Z	Z
VCO polarity	(1)	(2)

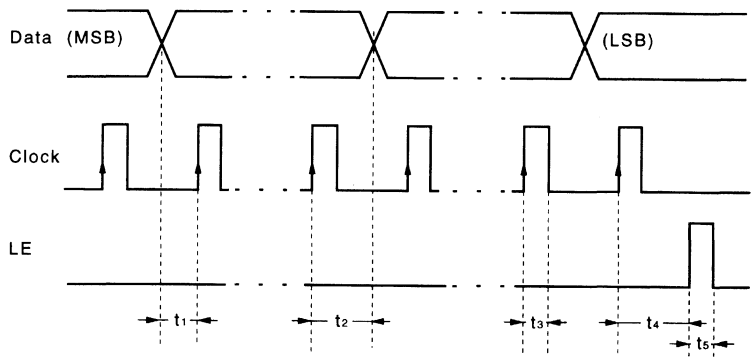
Z: High impedance

Notes: • When designing the PLL frequency synthesizer, set the FC bit according to the VCO polarity.
• PLL1 and PLL2 are set from the serial data when setting their respective compare divider values.
• Take note of the polarity when using an active low pass filter.



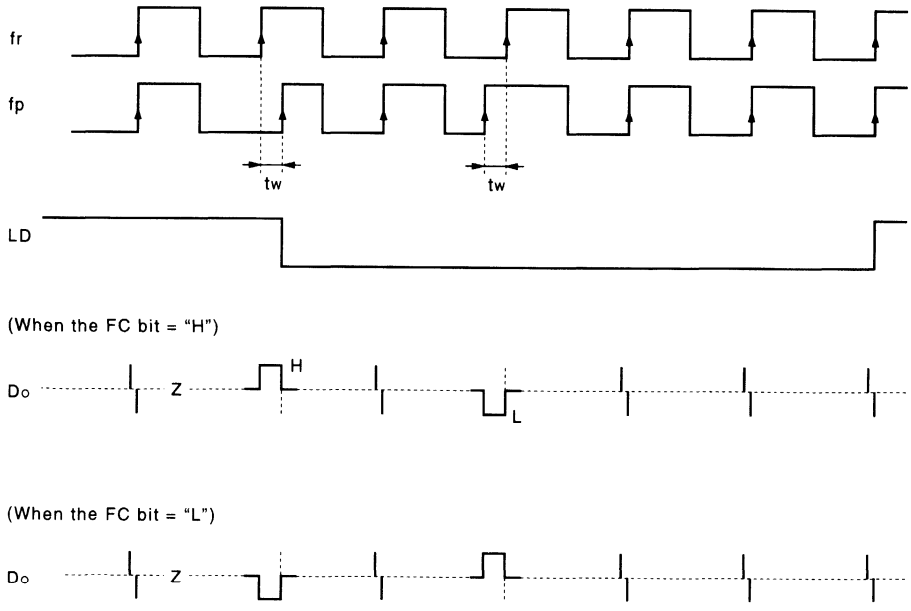
(3) Serial data input timing

- $t_1 > 100ns$, $t_2 > 1000ns$, $t_3 > 300ns$, $t_4 > 100ns$, $t_5 > 800ns$



Note: Data is loaded on the rising edge of the clock.

3. Output Waveform of the Phase Comparator



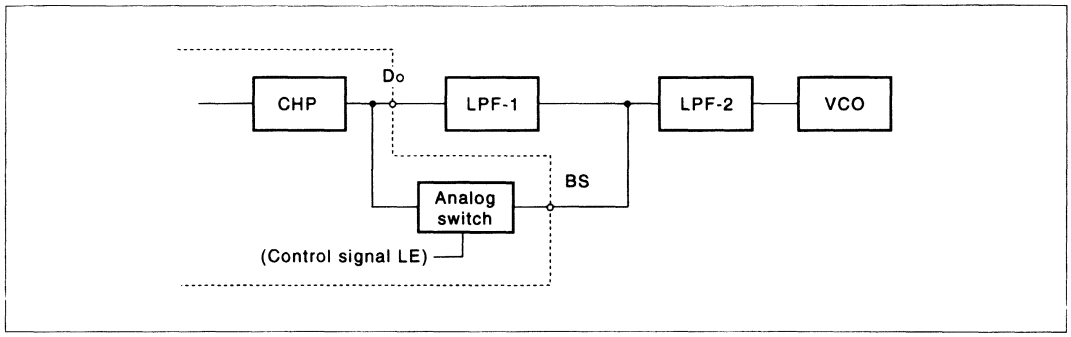
Notes:
- The phase detection range is -2π to $+2\pi$.
- The LD output goes to "L" when the phase error is more than tw and to "H" when the phase error stays less than tw for more than three cycles.
  (tw = 625 ns to 1250 ns for fosc = 12.8 MHz)

4. Analog Switch

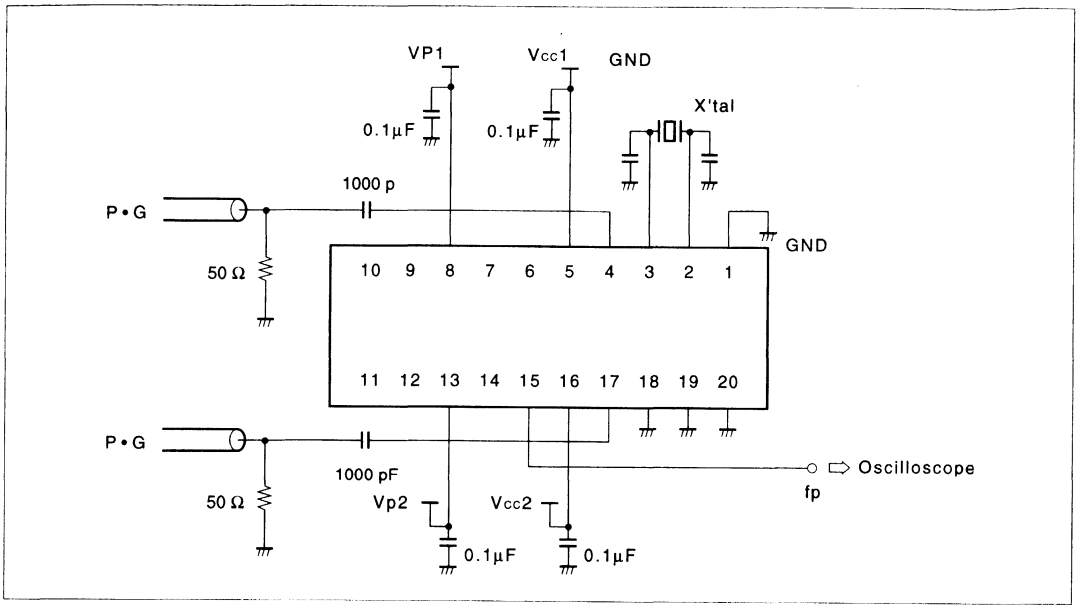
The analog switch is set on or off by the control data and LE signal settings. When the switch is on, the charge pump outputs (D_{O1} and D_{O2}) are output from the BS1 and BS2 pins. (The pins go to high impedance when the switch is off.)

	Setting the PLL1 programmable divider (CN1 = "L", CN2 = "H")		Setting the PLL2 programmable divider (CN1 = "H", CN2 = "H")	
	LE = "H"	LE = "L"	LE = "H"	LE = "L"
PLL1 Analog switch	On	Off	Off	Off
PLL2 Analog switch	Off	Off	On	Off

As in the example shown in the figure below, placing the analog switch midway through the LPF (LPF1 + LPF2) allows the LPF time constant to be reduced during PLL channel switching so as to reduce the lockup time.



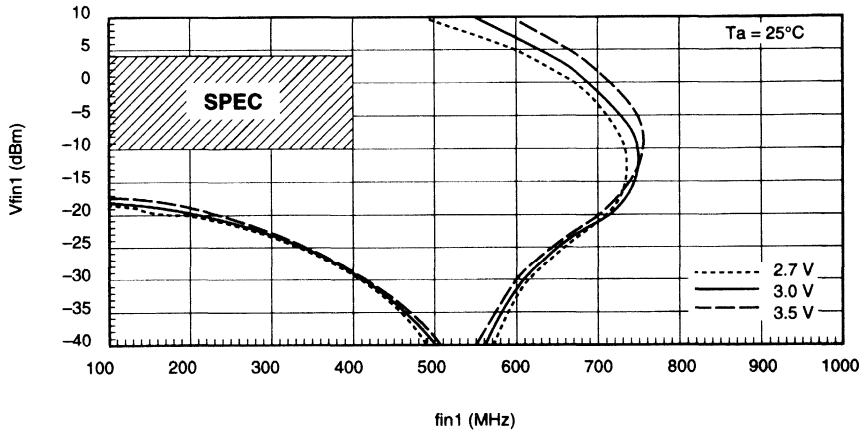
■ TEST CIRCUIT (For measuring the input sensitivity of the prescaler)



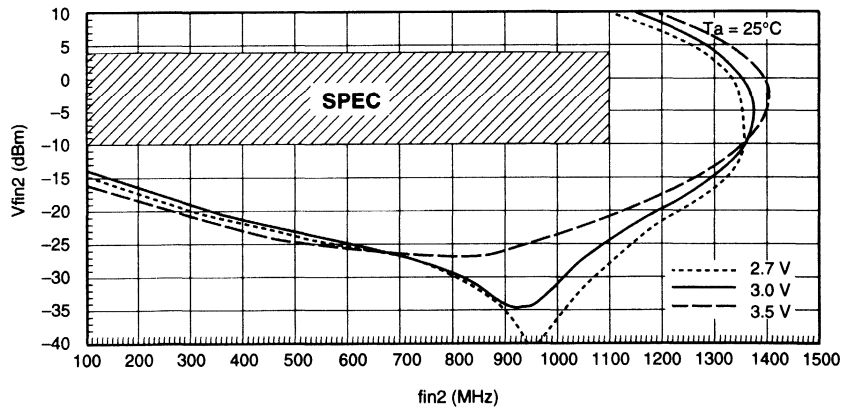
■ TYPICAL CHARACTERISTIC CURVES

1. fin Input Sensitivity Characteristics

PLL1 input sensitivity vs. Input frequency

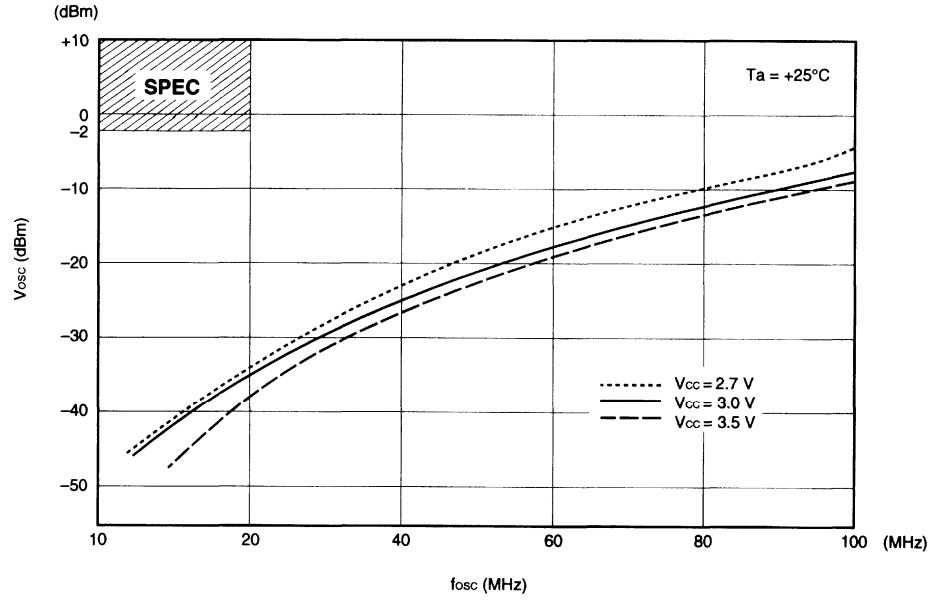


PLL2 input sensitivity vs. Input frequency



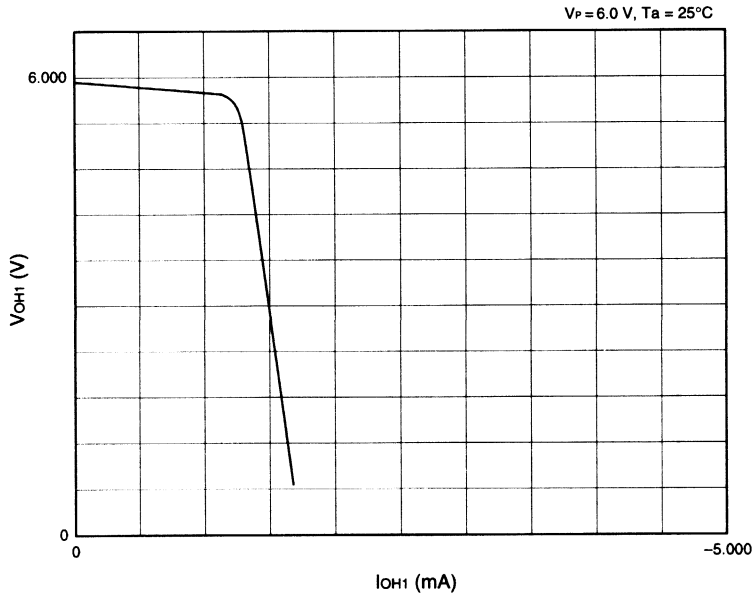
2. OSC_{IN} Input Sensitivity Characteristics

Input sensitivity vs. Input frequency

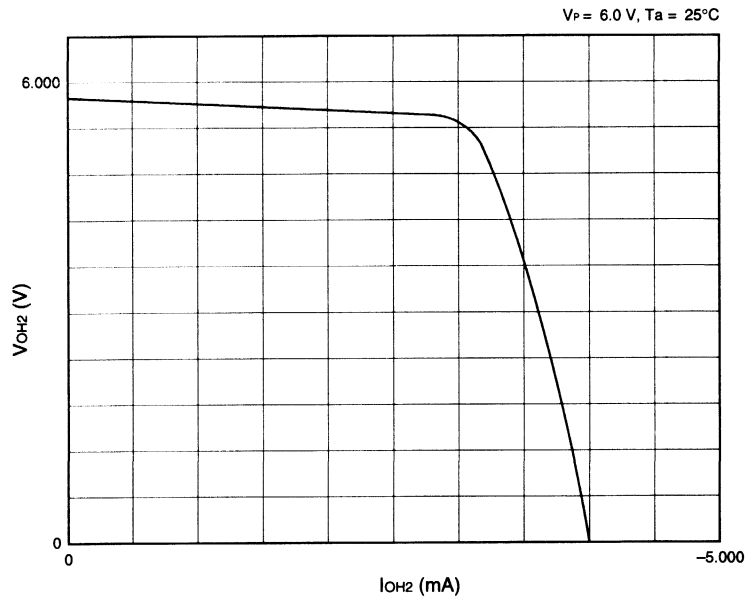


3. D_O Output Current Characteristics

"H" level output current vs. "H" level output voltage (PLL1)



"H" level output current vs. "H" level output voltage (PLL2)



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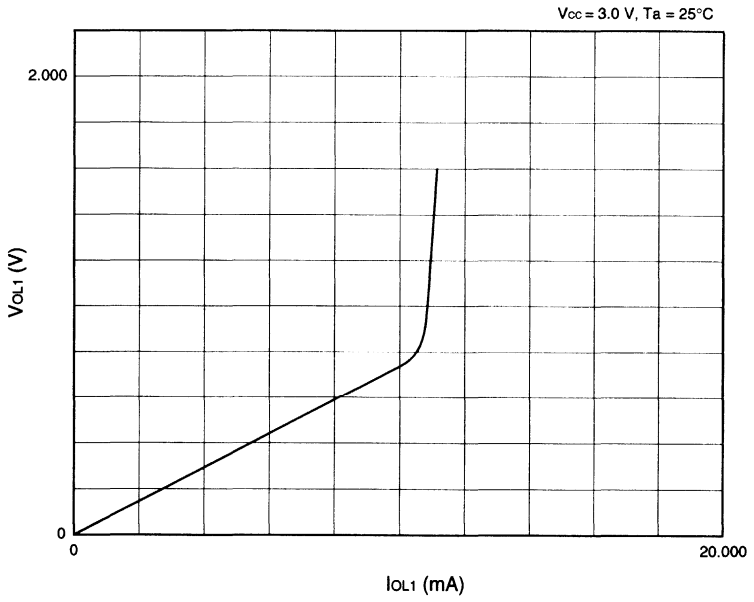
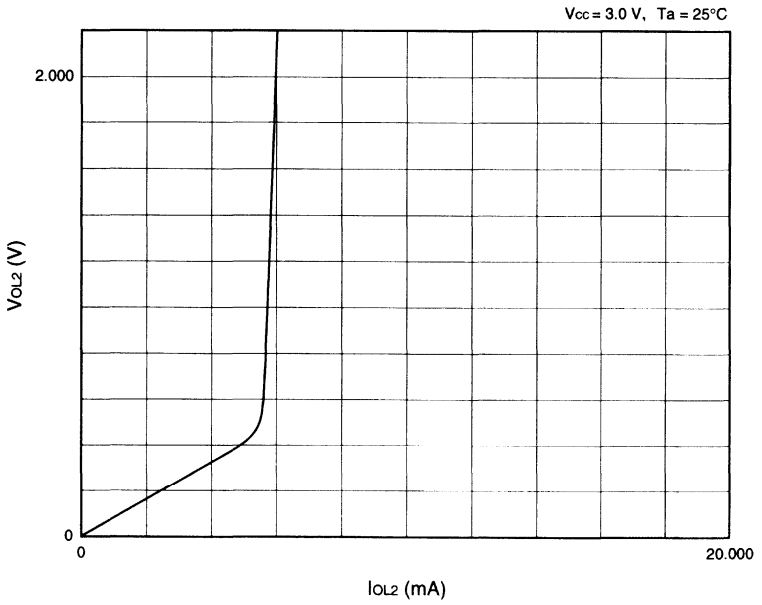
"L" level output current vs. "L" level output voltage (PLL1)



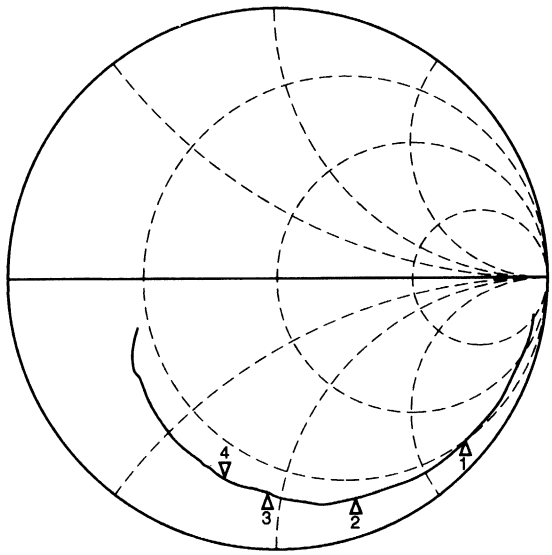
"L" level output current vs. "L" level output voltage (PLL2)



4. Input Impedance Characteristics

fin Input Impedance Characteristic

fin



1; 14.539Ω
−125.61Ω
500 MHz

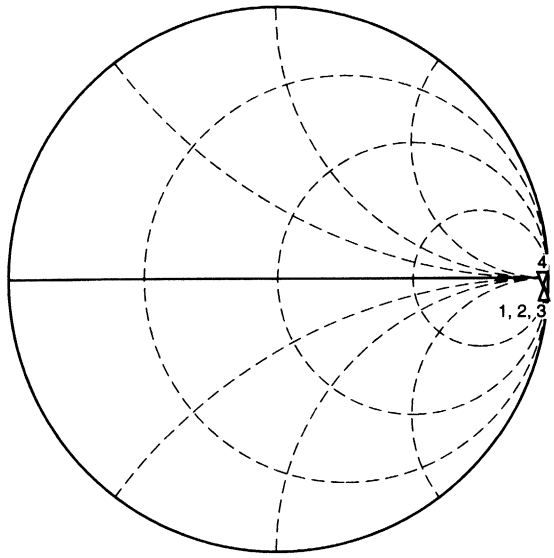
2; 9.6484Ω
−69.262Ω
800 MHz

3; 9.9023Ω
−46.156Ω
1 GHz

4; 10.102Ω
−37.453Ω
1.1 GHz

OSC_{IN} Input Impedance Characteristic

OSC_{IN}



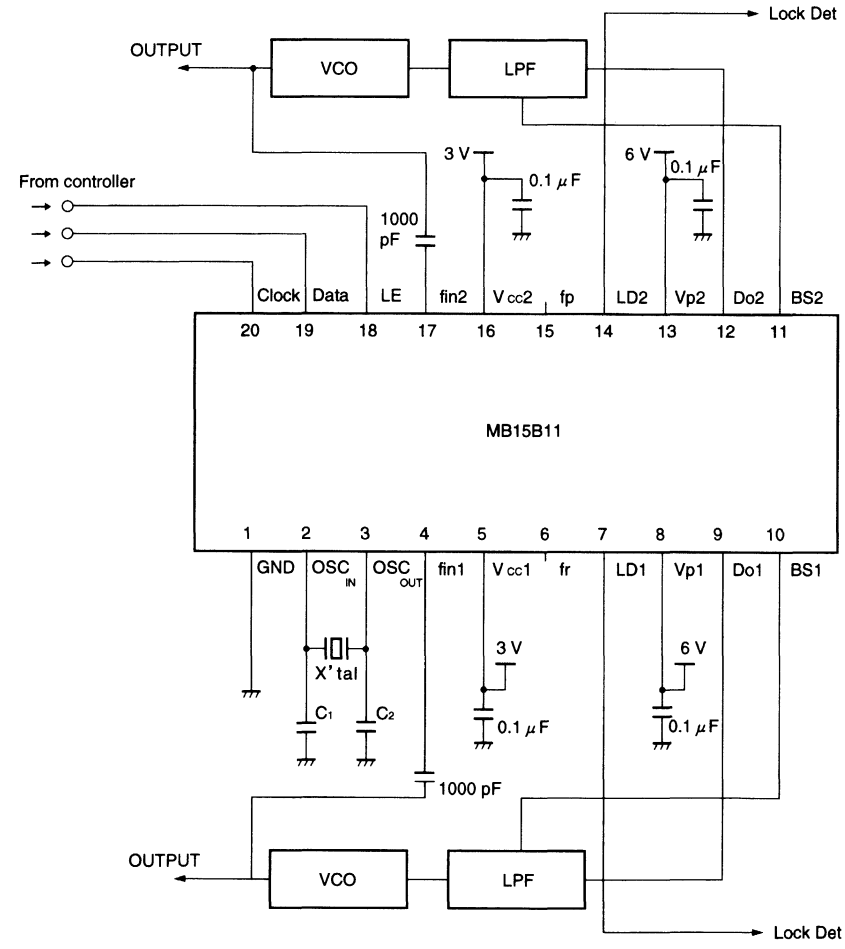
1; 1.425 kΩ
−3.5698 kΩ
10 MHz

2; 1.0444 kΩ
−2.637 kΩ
15 MHz

3; 800.75Ω
−2.2129 kΩ
20 MHz

4; 670.13Ω
−1.8371 kΩ
25 MHz

■ APPLICATION EXAMPLE



X'tal :12.8 MHz
Clock, Data, LE : Internal schmitt trigger circuits (Insert a pull-down resistor if an input is open.)
C1, C2 : Determined by the crystal oscillator.
Vp1, Vp2 : Up to 6 V

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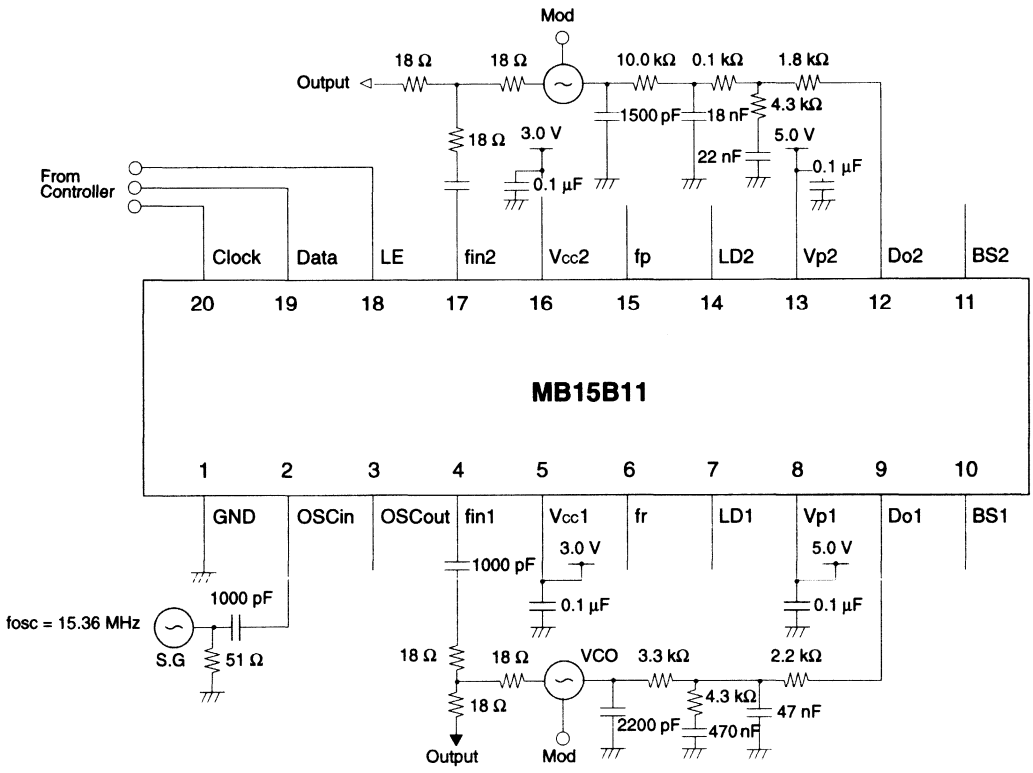
AMPS Application



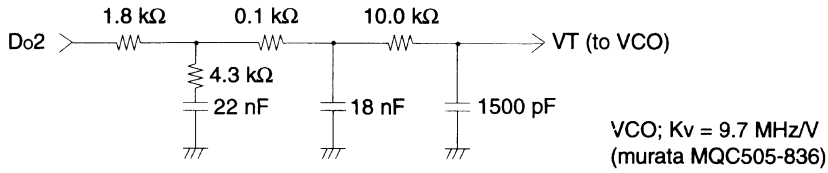
■ APPLICATION INFORMATION (AMPS)

PLL Characteristics (Rx mode)

fr = 30 kHz/V_{CC} = 3.0 V, Vp = 5.0 V, V_{VCO} = 5.0 V

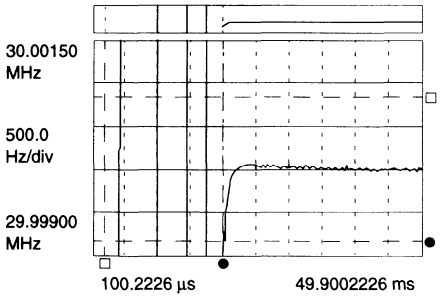
Paramater		Measured Value	Conditions
Hopping Time	Lch → Hch	18.4 mS	825.6 MHz → 850.5 MHz, Within ± 800 Hz
	Hch ← Lch	16.4 mS	850.5 MHz → 825.6 MHz, Within ± 800 Hz
Spurious Level		79 dBc	± 30 kHz Offset at 835.20 MHz
Phase Noise		73 dBc/Hz	± 1 kHz Offset at 835.20 MHz

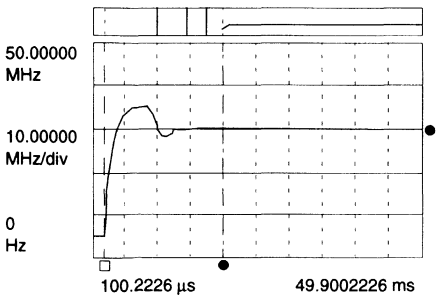
Loop Filter Schematics (Rx mode)



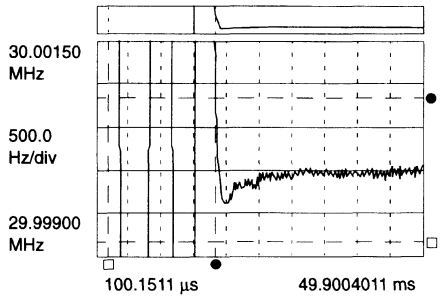
PLL Hopping Time (Rx mode)

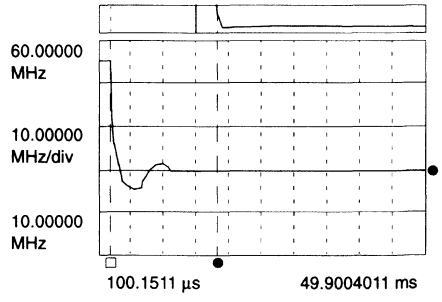
825.60 MHz → 850.50 MHz, Within ± 800 Hz
Lch → Hch 18.4 mS





850.50 MHz → 825.60 MHz, Within ± 800 Hz
Hch → Lch 16.4 mS





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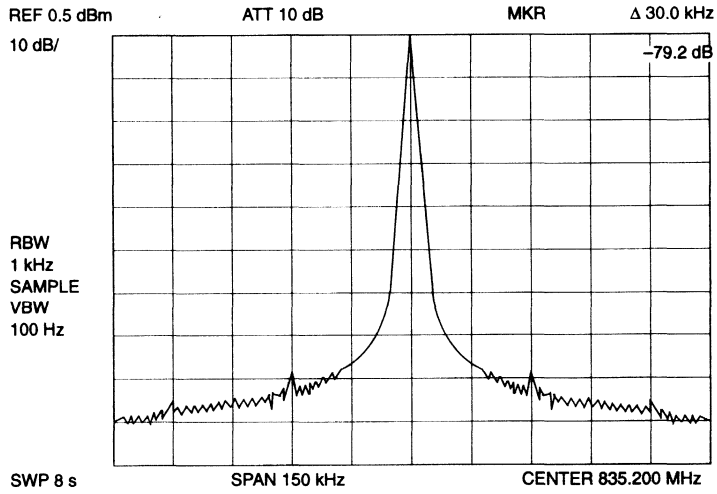
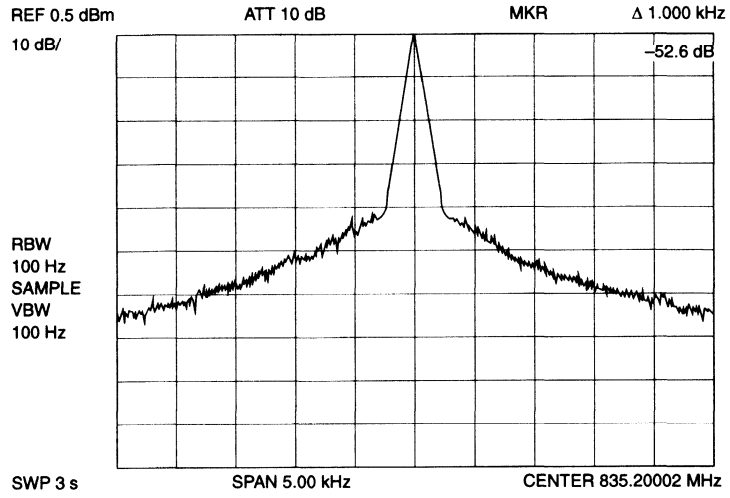
Spurious Level (Rx mode)



Phase Noise (Rx mode)



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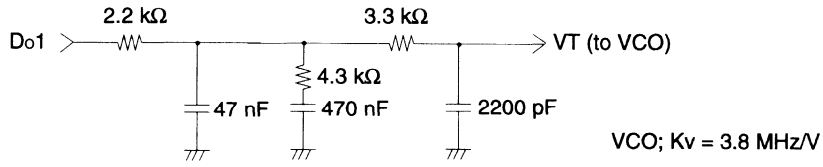
PLL Characteristics (Tx mode)

fr = 30 kHz/V_{CC} = 3.0 V, Vp = 5.0 V, V_{VCO} = 5.0 V

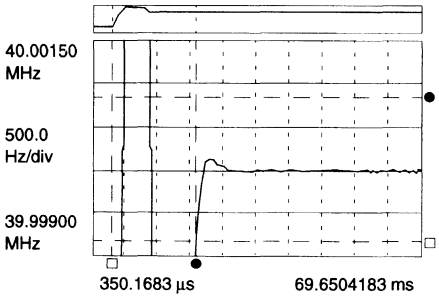
Paramater		Measured Value	Conditions
Hopping Time	Lch → Hch	17.5 mS	376.8 MHz → 385.8 MHz, Within ± 800 Hz
	Hch ← Lch	18.9 mS	385.8 MHz → 376.8 MHz, Within ± 800 Hz
Spurious Level		87 dBc	± 30 kHz Offset at 382.20 MHz
Phase Noise		81 dBc/Hz	± 1 kHz Offset at 382.20 MHz

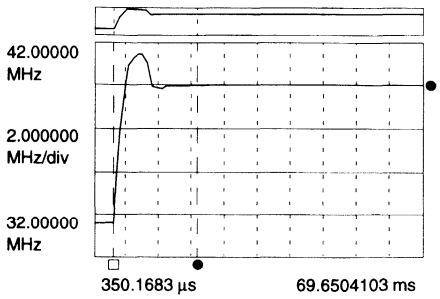
Loop Filter Schematics (Tx mode)



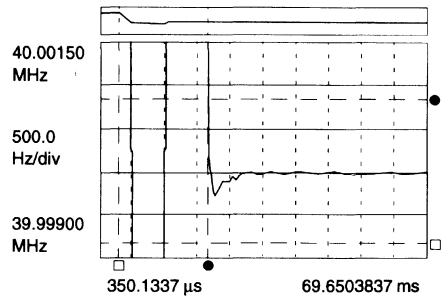
PLL Hopping Time (Tx mode)

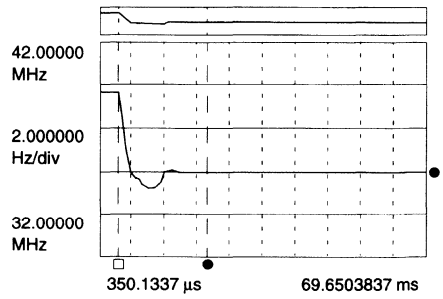
376.80 MHz → 385.80 MHz, Within ± 800 Hz
Lch → Hch 17.5 mS





385.80 MHz → 376.80 MHz, Within ± 800 Hz
Hch → Lch 18.9 mS





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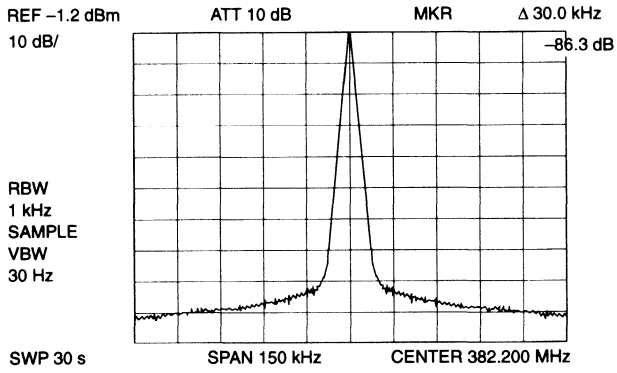
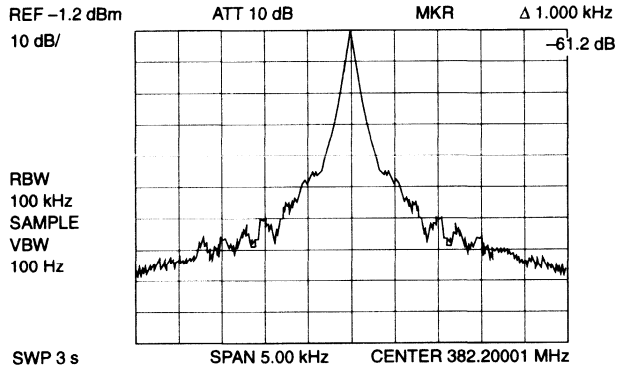
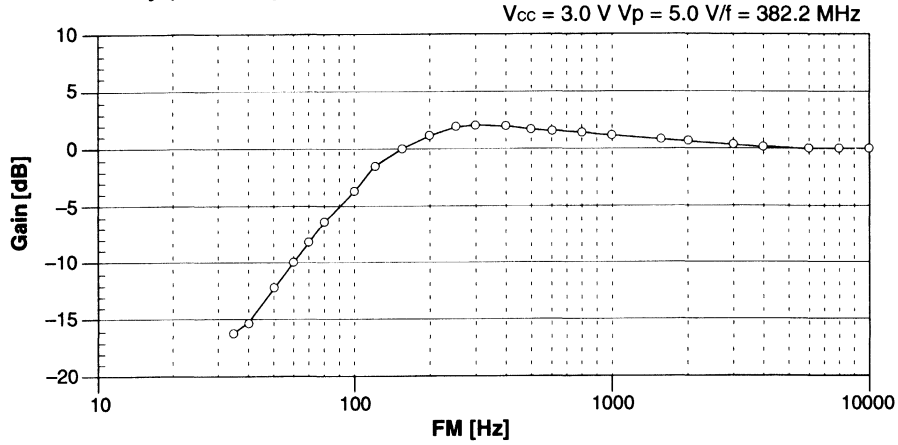
Spurious Level (Tx mode)



Phase Noise (Tx mode)



Modulation Linerity (Tx mode)



■ ORDERING INFORMATION

Part number	Package	Remarks
MB15B11PFV	20 pin, Plastic SSOP (FPT-20P-M03)	

FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-21332-1E

ASSP

1.2 GHz High-Speed Tuning PLL Frequency Synthesizer

MB15A16

■ DESCRIPTION

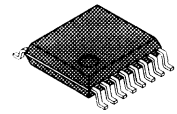
The Fujitsu MB15A16 is a serial input phase-locked loop (PLL) frequency synthesizer with a pulse-swallow function, and is suitable for the digital radio applications such as GSM. MB15A16 achieves the low noise performance as well as the high-speed lock-up which required for digital cellularphones.
The MB15A16 can operate from a single +3 V supply and has an Icc of 7.0 mA (typical).

■ FEATURES

- High operating frequency : f_{IN} = 1.2 GHz (V_{IN} = –10 dBm)
- Pulse-swallow function : High-speed dual-modules prescaler with selectable 64/65 and 128/129 divide ratios
- Low supply current : I_{CC} = 7.0 mA typ. at 3 V
- Power saving funtion : I_{PS} = 100 µA typ. (Controlled with PS pin)
- Serial input, 18-bit programmable divider consisting of:
  Binary 7-bit swallow counter : 0 to 127
  Binary 11-bit programmable counter : 5 to 2,047
- Serial input 17-bit programmable reference divider consisting of:
  Binary 14-bit programmable reference counter : 6 to 16,383
  1-bit for setting a prescaler divide ratio (SW bit)
  1-bit for switching a phase polarity (FC bit)
  1-bit for selecting LD/fout (LDS bit)
- On-chip high performance charge pump circuit and phase comparator, achieving high-speed lock-up and low phase noise
- Two types of phase comparator outputs selectable
  On-chip charge pump output
  Output for an external charge pump
- Wide operating temperature range: –40 to +85°C
- Plastic 16-pin SSOP (Shrink Small Outline Package)

■ PACKAGE

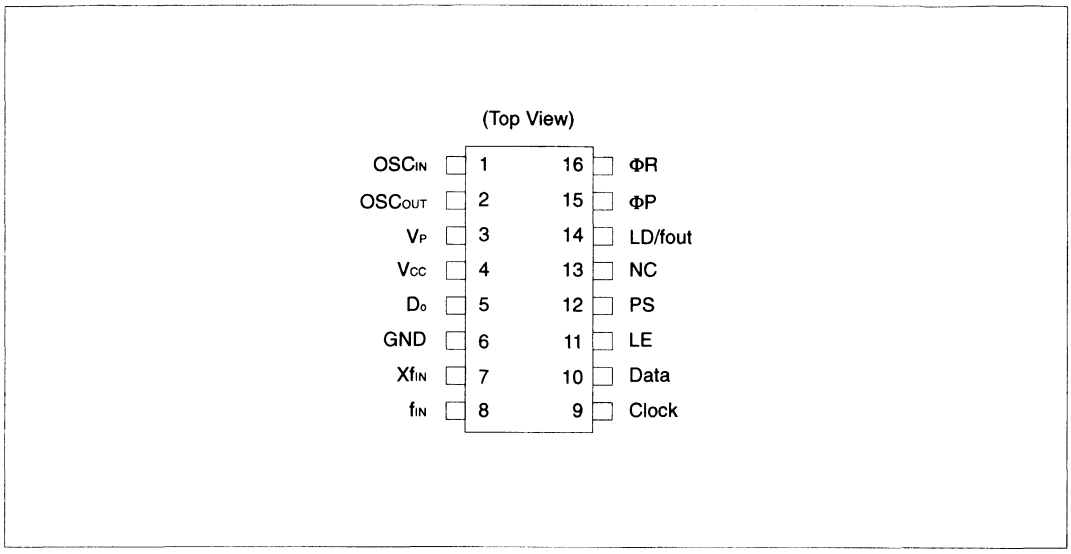
16-pin, Plastic SSOP



(FPT-16P-M05)

This device contains circuitry to protect the inputs against damage due to high static voltages or electroc fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

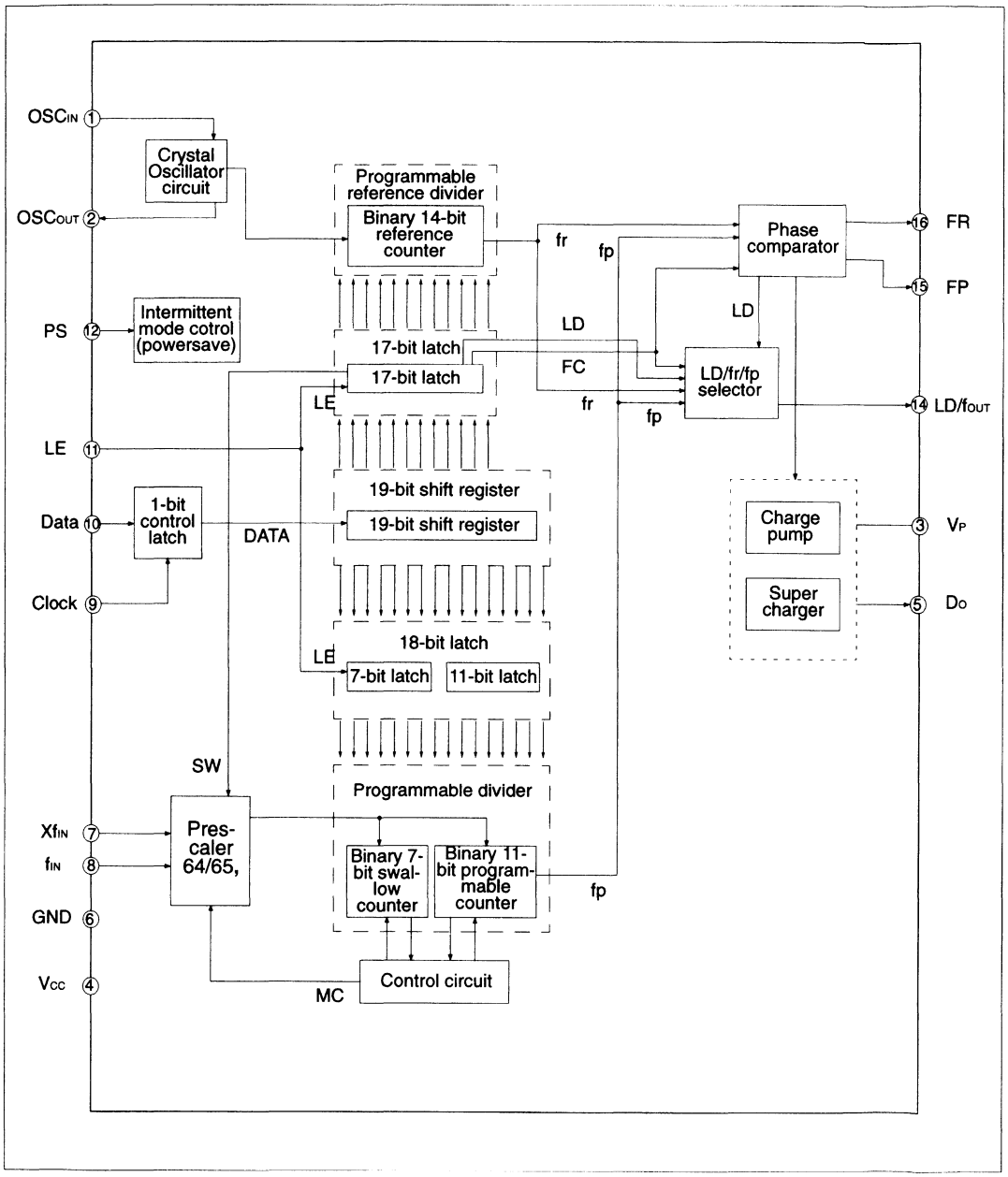
■ PIN ASSIGNMENT



■ PIN DESCRIPTION

Pin No.	Pin name	I/O	Description
1	OSC_{IN}	I	Programmable reference divider input. Oscillator input. Connection for external crystal or TCXO.
2	OSC_{OUT}	O	Oscillator output. Connection for the external crystal.
3	V_P	–	Power supply input for the charge pump.
4	V_{CC}	–	Power supply input.
5	D_O	O	Charge pump output. Phase of the charge pump can be reversed according FC input.
6	GND	–	Ground.
7	Xfin	I	Prescaler complementary input, and should be grounded via a capacitor.
8	fin	I	Prescaler input. Connection with an external VCO should be done AC coupled.
9	Clock	I	Clock input for 19-bit shift register. Data is shifted into the shift register on the rising edge of the clock. (Open is prohibited.)
10	Data	I	Serial data input using binary code. The last bit of the data is a control bit. (Open is prohibited.) Control bit = "H" ; Data is transmitted to the 17-bit latch. Control bit = "L" ; Data is transmitted to the 18-bit latch.
11	LE	I	Load enable signal input (Open is prohibited.) When LE is high, the data of the shift register are transferred to a latch, according to the control bit in the serial data.
12	PS	I	Power saving control input. This pin must be set at "L" at Power-ON. (Open is prohibited.) PS = "H" ; Normal mode PS = "L" ; Power saving mode
13	NC	–	No connection.
14	LD/f_{OUT}	O	Lock detector output(LD)/Monitor pin of the phase comparator(fout). A LDS bit in a serial data switchs LD/fout pin's output. LDS = "H" ; outputs fout LDS = "L" ; outputs LD
15	ΦP	O	Phase comparator output for an external charge pump. Phase of the output is reversed according to FC input. ΦP pin is a N-ch open drain output.
16	ΦR	O	Phase comparator output for an external charge pump. Phase of the output is reversed according to FC input. ΦR pin is a C-MOS output.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Remark
Power supply voltage	V_{CC}	−0.5 to +5.0	V	
	V_P	V_{CC} to 5.5	V	
Output voltage	V_O	−0.5 to V_{CC} +0.5	V	
Open drain voltage	V_{OOP}	−0.5 to 6.0	V	ΦP
Output current	I_O	±10	mA	
Storage temperature	Tstg	−55 to +125	°C	

Note: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Remark
		Min	Typ	Max		
Power supply voltage	V_{CC}	2.7	3.0	3.6	V	
	V_P	V_{CC}	−	5.0	V	
Input voltage	V_I	GND	−	V_{CC}	V	
Operating temperature	Ta	−40	−	+85	°C	

Notes: To protect against damage by electrostatic discharge, note the following handling precautions:

- Store and transport devices in conductive containers.
- Use properly grounded workstations, tools, and equipment.
- Turn off power before inserting or removing this device into or from a socket.
- Protect leads with conductive sheet, when transporting a board mounted device.

■ ELECTRICAL CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Value			Unit	Condition
			Min	Typ	Max		
Power supply current (Power saving current)		I_{CC} (I_{PS})	–	7 (0.1)	–	mA	With f_{IN} = 1.2 GHz, OSC_{IN} = 12 MHz, V_{CC} = 3.0 V. In locked state.
Operating frequency	f_{IN}	f_{IN}	300	–	1200	MHz	AC coupling with a 1000pF capacitor connected.
	OSC_{IN}	f_{OSC}	–	12	23	MHz	
Input sensitivity	f_{IN}	V_{IN}	–10	–	6	dBm	50Ω (refer to the test circuit.)
	OSC_{IN}	V_{OSC}	0.5	–	–	Vp-p	
High-level input voltage	Data, Clock, LE, PS	V_{IH}	V_{CC} x 0.7	–	–	V	
Low-level input voltage		V_{IL}	–	–	V_{CC} x 0.3	V	
High-level input current	Data, Clock, LE, PS	I_{IH}	–	–	1.0	mA	
Low-level input current		I_{IL}	–1.0	–	–	µA	
Input current	OSC_{IN}	I_{OSC}	–100	–	100	µA	
High-level output voltage	ΦR, LD	V_{OH}	2.1	–	–	V	Vcc = 3 V, I_{OH} = –1.0 mA
Low-level output voltage	ΦR, ΦP, LD	V_{OL}	–	–	0.4	V	Vcc = 3 V, I_{OL} = 1.0 mA
High-impedance cut off current	D_O, ΦP	I_{OFF}	–	–	0.3	µA	V_P = Vcc to 3.6 V V_{OOP} = GND to 6 V
Output current	ΦR, LD	I_{OH}	–1.0	–	–	mA	Vcc = 3 V
	ΦR, ΦP, LD	I_{OL}	–	–	1.0	mA	Vcc = 3 V
	D_O	I_{DOH}	–15	–	–5	mA	Vcc = 3 V, Vp = 5.0 V, V_{DOH} = 4.0 V
		I_{DOL}	6	–	18	mA	Vcc = 3 V, Vp = 5.0 V, V_{DOL} = 1.0 V

■ FUNCTION DESCRIPTIONS

Pulse Swallow Function

The devide ratio can be calculated using the following equation:

$f_{VCO} = [(M \times N) + A] \times f_{OSC} \div R \quad (A < N)$

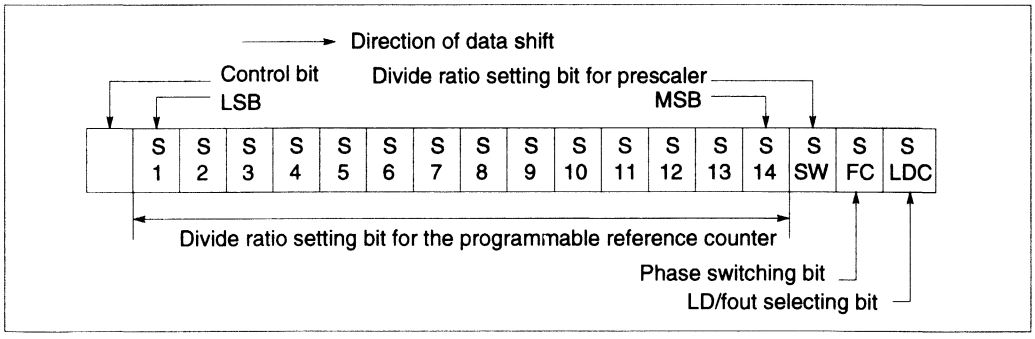
- f_{VCO} : Output frequency of external voltage controlled oscillator (VCO)
- N : Preset divide ratio of binary 11-bit programmable counter (5 to 2,047)
- A : Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$)
- f_{OSC} : Output frequency of the reference frequency oscillator
- R : Preset divide ratio of binary 14-bit programmable reference counter (6 to 16,383)
- M : Preset divide ratio of modules prescaler (64 or 128)

Serial Data Input

Serial data is processed using the Data, Clock, and LE pins. Serial data controls the 16-bit programmable reference divider and 18-bit programmable divider separately.
Binary serial data is entered via the Data pin.
One bit of data is shifted into the internal shift register on the rising edge of the clock. When the load enable pin is high or open, stored data is latched depending on the control data as follows:

Control data	Destination of serial data
H	17 bit latch
L	18 bit latch

(a) Programmable reference divider
The programmable reference divider consists of a 17-bit latch and a 14-bit reference counter. The serial 18-bit data format is shown below:



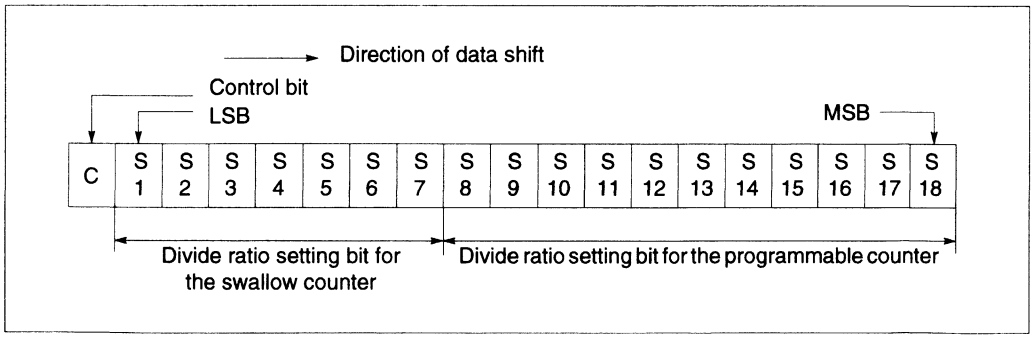
- 14-bit programmable reference counter divide ratio

Divide ratio R	S 14	S 13	S 12	S 11	S 10	S 9	S 8	S 7	S 6	S 5	S 4	S 3	S 2	S 1
6	0	0	0	0	0	0	0	0	0	0	0	1	1	0
7	0	0	0	0	0	0	0	0	0	0	0	1	1	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

(Divide ratio = 6 to 16,383)

Notes: 1. Divide ratios less than 6 are prohibited.
2. SW : This bit selects the divide ratio of the prescaler.
Low : 128 or 129
High: 64 or 65
3. LDS : This bit selects LD/fout pin output
High: outputs phase comparator monitoring signal(fout).
Low : outputs lock detecting signal(LD)
4. FC : This bit selects phase characteristics.
5. S1 to S14 : These bits select the divide ratio of the programmable reference counter (6 to 16,383).
6. C : Control bit: Set high.
7. Start data input with MSB first.

(b) Programmable divider
The programmable divider consists of a 19-bit shift register, a 18-bit latch, a 7-bit swallow counter, and a 11-bit programmable counter. The serial 19-bit data format is shown below:



- 7-bit swallow counter divide ratio

Divide ratio A	S7	S6	S5	S4	S3	S2	S1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

(Divide ratio = 0 to 127)

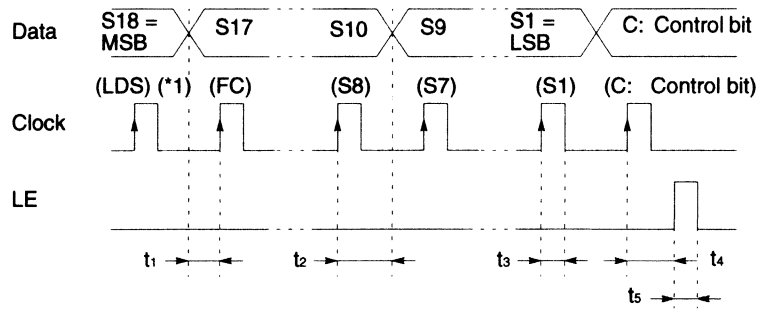
Divide ratio N	S18	S17	S16	S15	S14	S13	S12	S11	S10	S9	S8
5	0	0	0	0	0	0	0	0	1	0	1
6	0	0	0	0	0	0	0	0	1	1	0
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

(Divide ratio = 5 to 2,047)

Notes: 1. Divide ratios less than 5 are prohibited for 11-bit programmable counter.
2. S1 to S7 : These bits select the divide ratio of swallow counter (0 to 127).
3. S8 to S18 : These bits select the divide ratio of programmable counter (5 to 2,047).
4. C : Control bit: (Set low)
5. Start data input with MSB first.

Serial Data Input Timing

- t_1 (≥ 100ns) : Data setup time t_2 (≥ 1000ns) : Data hold time t_3 (≥ 300ns) : Clock pulse width
  t_4 (≥ 100ns) : LE setup time to the rising edge of last clock t_5 (≥ 790ns) : LE pulse width



*1: Bits enclosed in parentheses are used when the divide ratio of the programmable reference divider is selected.
Note: One bit of data is shifted into the shift register on the rising edge of the clock.

Power Saving Mode (Intermittent operation control circuit)

Setting PS pin to Low, MB15A16 enters into power saving mode resultantly current consumption can be limited to 100μA (typ.). Setting PS pin to High, power saving mode is released so that the device works normally.
In addition, the intermittent operation control circuit is included which helps smooth start up from stand by mode. The power consumption can be reduced by the intermittent operation that powering down or waking up parts of the PLL circuitry. If a PLL is powered up uncontrolled, the resulting phase comparator output signal is unpredictable due to an undefined phase relation between reference frequency (f_r) and comparison frequency (f_p) and may in the worst case take longer time for lock up of the loop.
To prevent this, the intermittent operation control circuit enforces a limited error signal output of the phase detector during power up, thus keeping the loop locked.

Note: PS pin must be set "L" at Power-ON

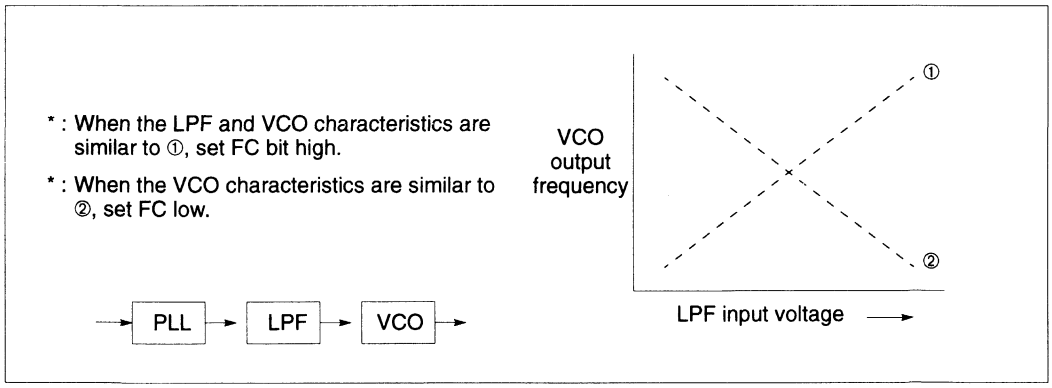
Relation Between the FC Input and Phase Characteristics

The FC bit changes the phase characteristics of the phase comparator. Both the internal charge pump output level (Do) and the phase comparator output (ΦR, ΦP) are reversed according to the FC bit. Also, the monitor pin (f_{OUT}) output is controlled by the FC bit. The relationship between the FC bit and each of Do, ΦR, and ΦP is shown below.

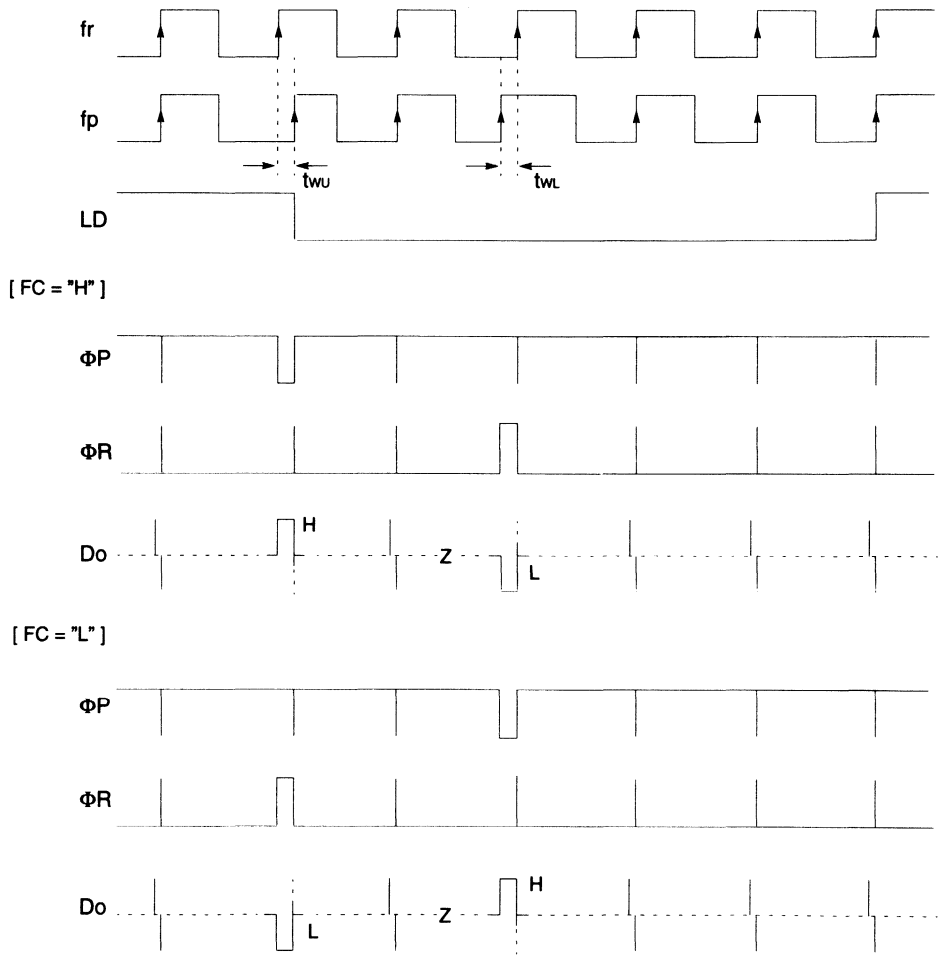
	FC = High				FC = Low			
	Do	ΦR	ΦP	fout	Do	ΦR	ΦP	fout
$f_r > f_p$	H	L	L	(fr)	L	H	Z(*1)	(fp)
$f_r < f_p$	L	H	Z(*1)	(fr)	H	L	L	(fp)
$f_r = f_p$	Z(*1)	L	Z(*1)	(fr)	Z(*1)	L	Z(*1)	(fp)

*1: High impedance

When designing a synthesizer, the FC pin setting depends on the VCO and LPF characteristics.

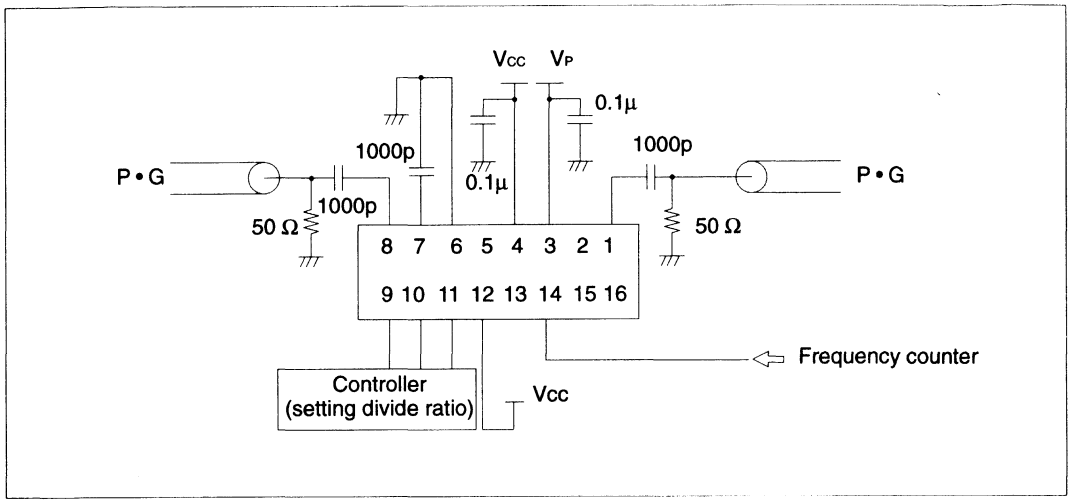


Phase Comparator Output Waveforms



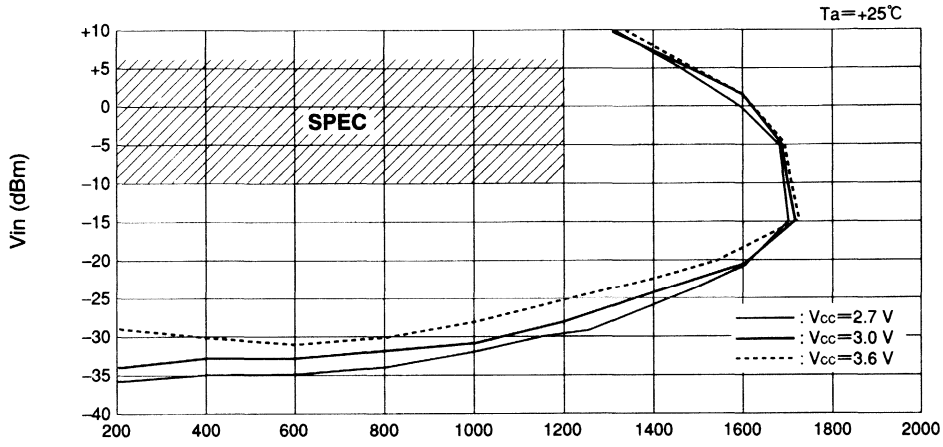
Notes: 1. Phase difference detection range: -2π to $+2\pi$
2. LD output becomes low when phase is twu or more. LD output becomes high when phase error is twL or less and continues to be so for three cycles or more.
3. twu and twL depend on OSCin input frequency.
twu ≤ 8/fosc (e. g. twu ≤ 625ns, foscin = 12.8 MHz)
twL ≥ 16/fosc (e. g. twL ≥ 1250ns, foscin = 12.8 MHz)

■ TEST CIRCUIT (for Measuring Input Sensitivity fin/OSCin)

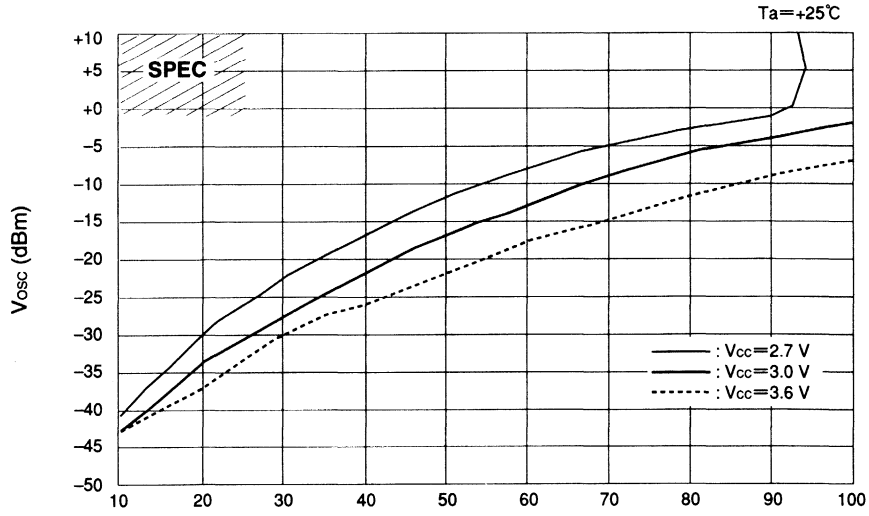


■ TYPICAL CHARACTERISTICS

Input Sensitivity (fin Pin)



Input Sensitivity (OSCin Pin)



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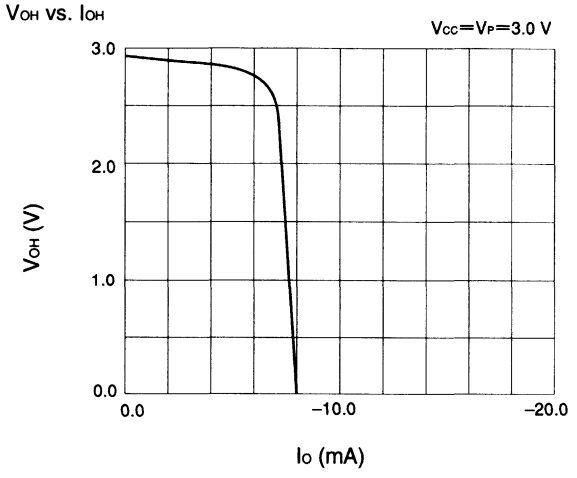
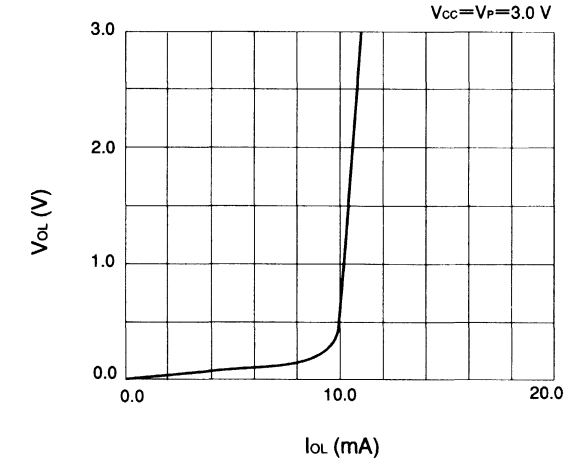
Charge Pump Current vs. Voltage (Do Pin)

V_{OH} vs. I_{OH}



V_{OL} vs. I_{OL}



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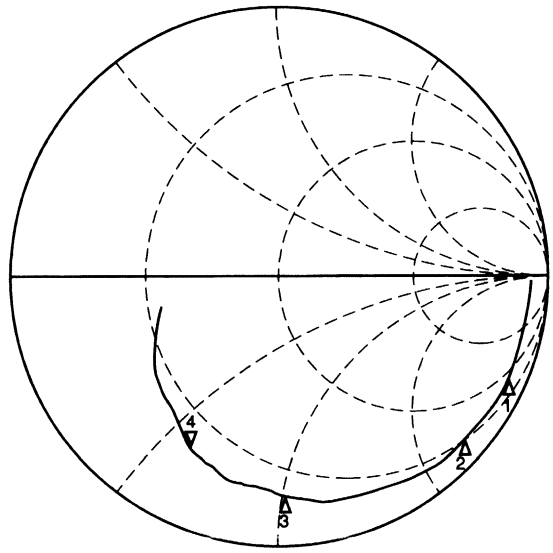
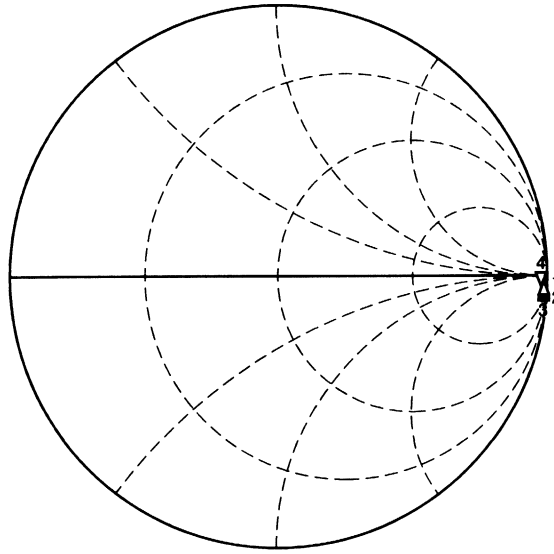
Input Impedance

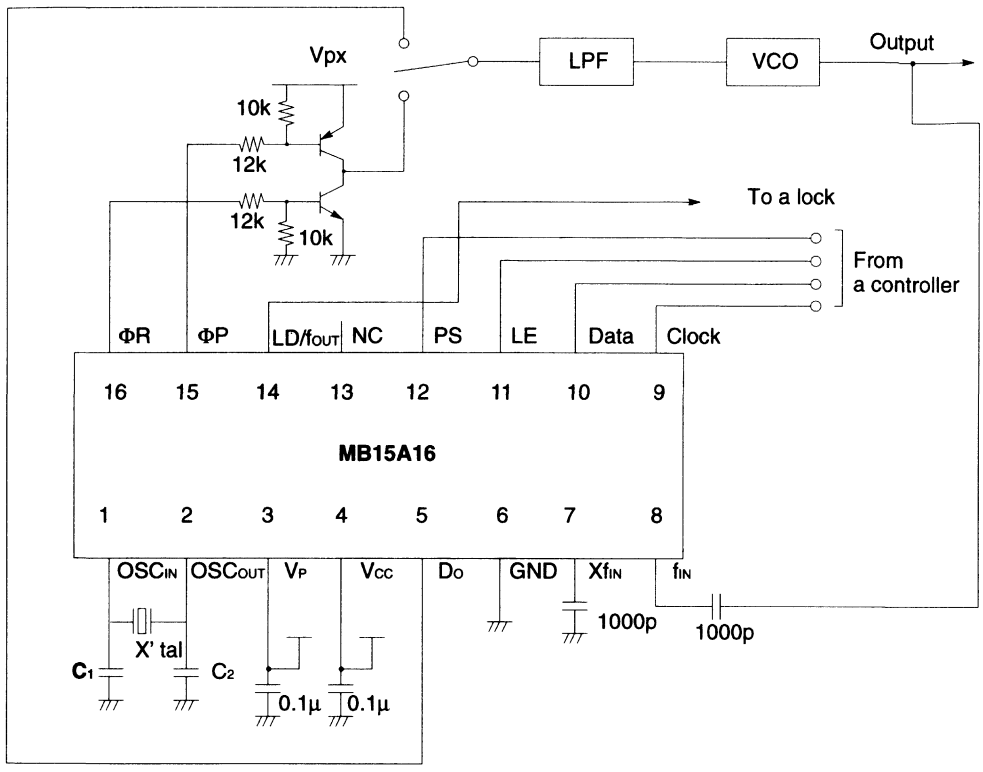
fin Pin



OSCin Pin



■ APPLICATION EXAMPLE

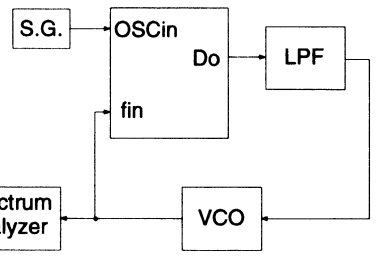


V_{PX}	:	Maximum 6 V
C_1, C_2	:	Depend on the crystal parameters
ΦP	:	N-ch open drain output
ΦR	:	C-MOS output

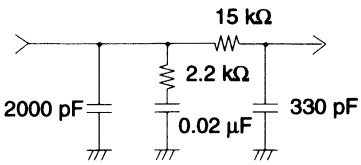
■ REFERENCE INFORMATION

Typical plots measured with the test circuit are shown below. Each plots shows lock up time, phase noise, and reference leakage.

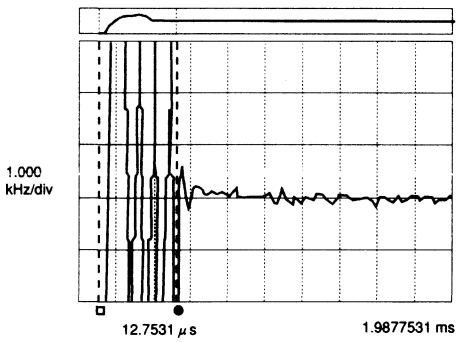
Test Circuit



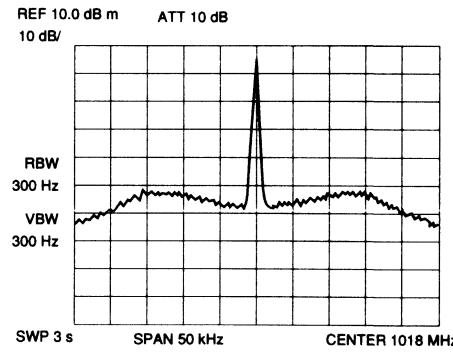
- f_{VCO} = 1018 MHz
- K_V = 20 MHz/V
- f_r = 200 kHz
- fosc = 13 MHz
- LPF



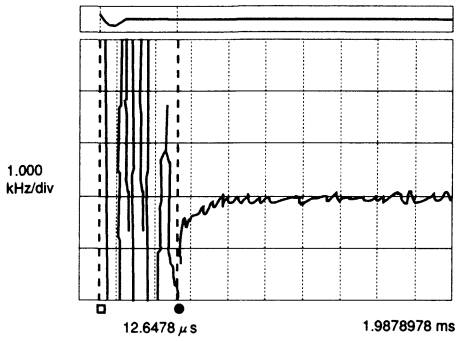
PLL Lock Up Time = 400 µs
(1,031 MHz → 1,005 MHz, within ± 1 kHz)



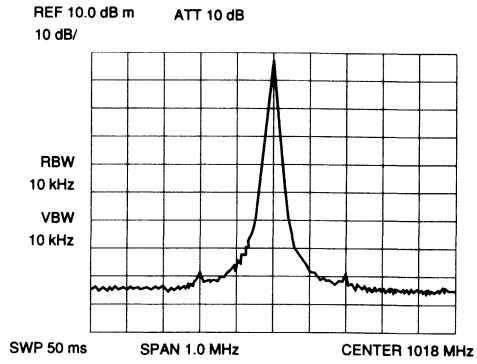
PLL Phase Noise
@Within loop band = 74 dBc/Hz



PLL Lock Up Time = 400 µs
(1,005 MHz → 1,031 MHz, within ± 1 kHz)



PLL Reference Leakage
@200 kHz offset = 75dBc



■ ORDERING INFORMATION

Part number	Package	Remarks
MB15A16 PFV	16-pin Plastic SSOP (FPT-16P-M05)	

FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-21340-1E

ASSP
Single Serial Input PLL Frequency Synthesizer
On-Chip 1.2 GHz Prescaler

MB15E03

■ DESCRIPTION

The Fujitsu MB15E03 is serial input Phase Locked Loop (PLL) frequency synthesizer with a 1.2 GHz prescaler. A 64/65 or a 128/129 can be selected for the prescaler that enables pulse swallow operation.

The latest BiCMOS process technology is used, resultantly a supply current is limited as low as 3.5 mA typ. This operates with a supply voltage of 3.0 V (typ.).

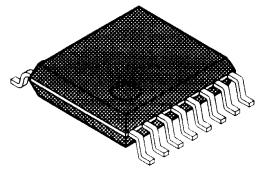
Furthermore, a super charger circuit is included to get a fast tuning as well as low noise performance. As a result of this, MB15E03 is ideally suitable for digital mobile communication such as GSM (Global System for Mobile Communications).

■ FEATURES

- High frequency operation: 1.2 GHz max
- Low power supply voltage: V_{CC} = 2.7 to 3.6 V
- Very Low power supply current : I_{CC} = 3.5 mA (at V_{CC} = 3 V)
- Power saving function : I_{PS} = 0.1 µA typ.
- Pulse swallow function: 64/65 or 128/129
- Serial input 14-bit programmable reference divider: R = 5 to 16,383
- Serial input 18-bit programmable divider consisting of:
  - Binary 7-bit swallow counter: 0 to 127
  - Binary 11-bit programmable counter: 3 to 2,047
- Wide operating temperature: Ta = −40 to 85°C
- Plastic 16-pin SSOP package (FPT-16P-M05)

■ PACKAGE

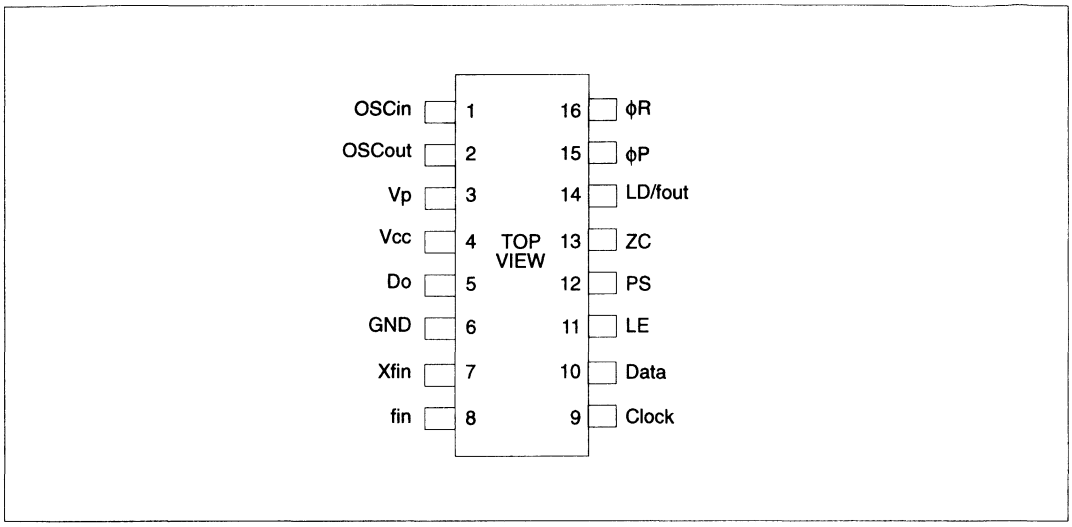
16-pin, Plastic SSOP



(FPT-16P-M05)

This device contains circuitry to protect the inputs against damage due to high static voltages or electroc fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

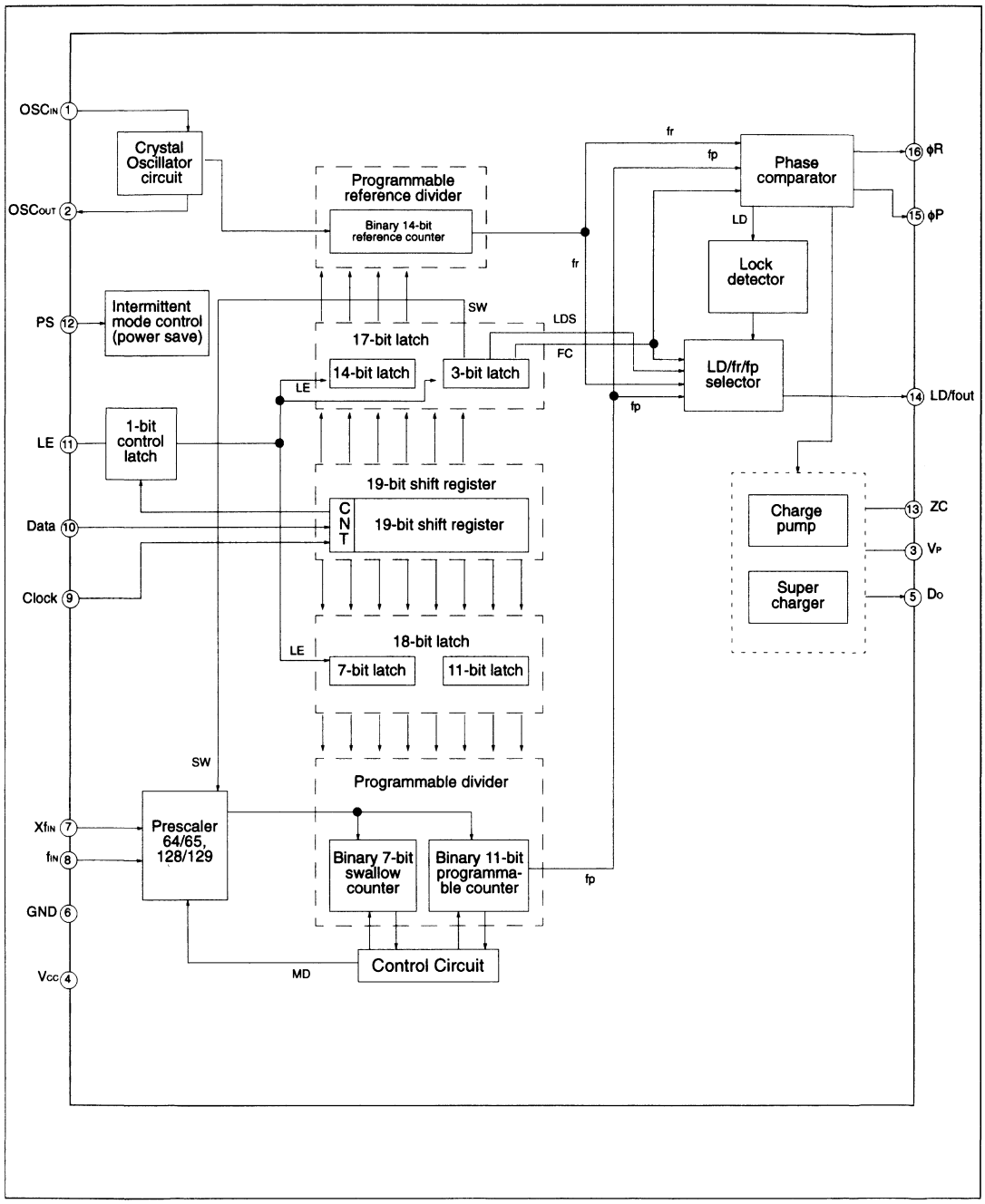
■ PIN ASSIGNMENT



■ PIN DESCRIPTIONS

Pin no.	Pin name	I/O	Descriptions
1	OSC_{IN}	I	Programmable reference divider input. Oscillator input. Connection for an crystal or a TCXO. TCXO should be connected with a coupling capacitor.
2	OSC_{OUT}	O	Oscillator output. Connection for an external crystal.
3	V_P	–	Power supply voltage input for the charge pump.
4	V_{CC}	–	Power supply voltage input.
5	D_O	O	Charge pump output. Phase of the charge pump can be reversed by FC bit.
6	GND	–	Ground.
7	Xfin	I	Prescaler complementary input, and should be grounded via a capacitor.
8	fin	I	Prescaler input. Connection with an external VCO should be done with AC coupling.
9	Clock	I	Clock input for the 19-bit shift register. Data is shifted into the shift register on the rising edge of the clock. *(Open is prohibited.)*
10	Data	I	Serial data input using binary code. The last bit of the data is a control bit. *(Open is prohibited.)* Control bit = "H" ; Data is transmitted to the programmable reference counter. Control bit = "L" ; Data is transmitted to the programmable counter.
11	LE	I	Load enable signal input *(Open is prohibited.)* When LE is high, the data in the shift register is transferred to a latch, according to the control bit in the serial data.
12	PS	I	Power saving mode control. This pin must be set at "L" at Power-ON. *(Open is prohibited.)* PS = "H" ; Normal mode PS = "L" ; Power saving mode
13	ZC	I	Forced high-impedance control for the charge pump (with internal pull up resistor.) ZC = "H" ; Normal Do output. ZC = "L" ; Do becomes high impedance.
14	LD/fout	O	Lock detect signal output(LD)/phase comparator monitoring output (fout). The output signal is selected by LDS bit in the serial data. LDS = "H" ; outputs fout (fr/fp monitoring output) LDS = "L" ; outputs LD ("H" at locking, "L" at unlocking.)
15	ϕP	O	Phase comparator output for an external charge pump. Nch open drain output.
16	ϕR	O	Phase comparator output for an external charge pump. CMOS output.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Remark
Power supply voltage	V_{CC}	−0.5 to +4.0	V	
	V_P	V_{CC} to +6.0	V	
Input voltage	V_I	−0.5 to V_{CC} +0.5	V	
Output voltage	V_O	−0.5 to V_{CC} +0.5	V	
Storage temperature	T_{stg}	−55 to +125	°C	

Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Remark
		Min.	Typ.	Max.		
Power supply voltage	V_{CC}	2.7	3.0	3.6	V	
	V_P	V_{CC}	–	6.0	V	
Input voltage	V_I	GND	–	V_{CC}	V	
Operating temperature	Ta	−40	–	+85	°C	

Notes: To protect against damage by electrostatic discharge, note the following handling precautions:
-Store and transport devices in conductive containers.
-Use properly grounded workstations, tools, and equipment.
-Turn off power before inserting or removing this device into or from a socket.
-Protect leads with conductive sheet, when transporting a board mounted device.

■ ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.7 to 3.6 V, Ta = –40 to +85°C)

Parameter		Symbol	Condition	Value			Unit
				Min.	Typ.	Max.	
Power supply current*1		I_{CC}	fin = 1200 MHz, fosc = 12 MHz	–	3.5	–	mA
Power saving current		Ips	PS = "L", ZC = "H" or open	–	0.1*2	10	µA
Operating frequency		fin		100	–	1200	MHz
Crystal oscillator operating frequency		fosc	min. 500 mVp-p	3	–	40	MHz
Input sensitivity	fin	Vfin	50 Ω system (Refer to the test circuit.)	–10	–	+2	dBm
	OSCin	V_{OSC}		500	–	V_{CC}	mVp-p
Input voltage	Data, Clock, LE, PS, ZC	V_{IH}		V_{CC} × 0.7	–	–	V
		V_{IL}		–	–	V_{CC} × 0.3	
Input current	Data, Clock, LE, PS	I_{IH}		–1.0	–	+1.0	µA
		I_{IL}		–1.0	–	+1.0	
	ZC	I_{IH}		–1.0	–	+1.0	µA
		I_{IL}	Pull up input	–100	–	0	
	OSCin	I_{IH}		0	–	+100	µA
		I_{IL}		–100	–	0	
Output voltage	φP	V_{OL}	Open drain output	–	–	0.4	V
	φR, LD/fout	V_{OH}	V_{CC} = 3 V, I_{OH} = –1 mA	V_{CC} – 0.4	–	–	V
		V_{OL}	V_{CC} = 3 V, I_{OL} = 1 mA	–	–	0.4	
	Do	V_{DOH}	V_{CC} = 3 V, I_{DOH} = –1 mA	Vp – 0.4	–	–	V
		V_{DOL}	V_{CC} = 3 V, I_{DOL} = 1 mA	–	–	0.4	
High impedance cutoff current	Do	I_{OFF}	V_{CC} = 3 V, Vp = 6 V Voop = GND to 6 V	–	–	1.1	µA
Output current	φP	I_{OL}		1.0	–	–	mA
	φR, LD/fout	I_{OH}		–	–	–1.0	mA
		I_{OL}		1.0	–	–	
	Do	I_{DOH}	V_{CC} = 3.0 V, Vp = 5 V, V_{DOH} = 4.0 V Ta = 25°C	–	–10.0	–	mA
		I_{DOL}	V_{CC} = 3.0 V, Vp = 5 V, V_{DOL} = 1.0 V Ta = 25°C	–	10.0	–	

*1: Conditions; V_{CC} = 3.0 V, Ta = 25°C, in locking state.

*2: Conditions; V_{CC} = 3.0 V, Ta = 25°C, fosc = 12 MHz (–2 dB)

■ FUNCTION DESCRIPTIONS

Pulse Swallow Function

The divide ratio can be calculated using the following equation:

$f_{VCO} = [(M \times N) + A] \times f_{OSC} + R \quad (A < N)$

- f_{VCO} : Output frequency of external voltage controlled oscillator (VCO)
- N : Preset divide ratio of binary 11-bit programmable counter (5 to 2,047)
- A : Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$)
- f_{OSC} : Output frequency of the reference frequency oscillator
- R : Preset divide ratio of binary 14-bit programmable reference counter (5 to 16,383)
- M : Preset divide ratio of modules prescaler (64 or 128)

Serial Data Input

Serial data is processed using the Data, Clock, and LE pins. Serial data controls the programmable reference divider and the programmable divider separately.
Binary serial data is entered through the Data pin.
One bit of data is shifted into the shift register on the rising edge of the clock. When the load enable pin is high, stored data is latched according to the control bit data as follows:

Table.1 Control Bit

Control bit (CNT)	Destination of serial data
H	17 bit latch (for the programmable reference divider)
L	18 bit latch (for the programmabie divider)

Shift Register Configuration

Programmable Reference Counter

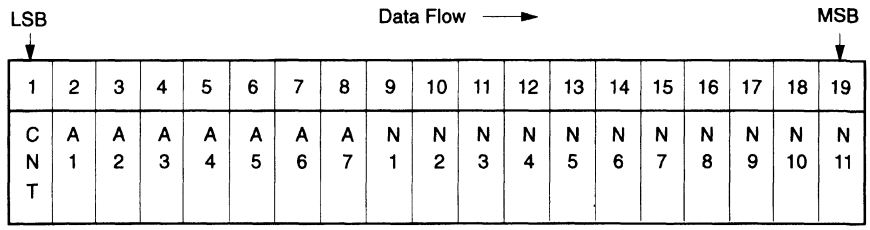
LSB ↓ Data Flow ⟶ MSB ↓

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
CNT	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	SW	FC	LDS

CNT : Control bit [Table. 1]
R1 to R14 : Divide ratio setting bit for the programmable reference counter (5 to 16,383) [Table. 2]
SW : Divide ratio setting bit for the prescaler (64/65 or 128/129) [Table. 5]
FC : Phase control bit for the phase comparator [Table. 7]
LDS : LD/fout signal select bit [Table. 6]

Note: Start data input with MSB first

Programmable Reference Counter



1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
CNT	A1	A2	A3	A4	A5	A6	A7	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11

CNT : Control bit [Table. 1]
N1 to N11 : Divide ratio setting bits for the programmable counter (5 to 2,047) [Table. 3]
A1 to A7 : Divide ratio setting bits for the swallow counter (0 to 127) [Table. 4]

Note: Start data input with MSB first

Table2. Binary 14-bit Programmable Reference Counter Data Setting

Divide ratio (R)	R 14	R 13	R 12	R 11	R 10	R 9	R 8	R 7	R 6	R 5	R 4	R 3	R 2	R 1
5	0	0	0	0	0	0	0	0	0	0	0	1	0	1
6	0	0	0	0	0	0	0	0	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: • Divide ratio less than 5 is prohibited.

Table.3 Binary 11-bit Programmable Counter Data Setting

Divide ratio (N)	N 11	N 10	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1
5	0	0	0	0	0	0	0	0	1	0	1
6	0	0	0	0	0	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.	.	.	.
2047	1	1	1	1	1	1	1	1	1	1	1

Note: • Divide ratio less than 5 is prohibited.
• Divide ratio (N) range = 5 to 2,047

Table.4 Binary 7-bit Swallow Counter Data Setting

Divide ratio (A)	A 7	A 6	A 5	A 4	A 3	A 2	A 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.
127	1	1	1	1	1	1	1

Note: • Divide ratio (A) range = 0 to 127

Table. 5 Prescaler Data Setting

SW	Prescaler Divide ratio
H	64/65
L	128/129

Table. 6 LD/fout Output Select Data Setting

LDS	LD/fout output signal
H	fout signal
L	LD signal

Relation between the FC input and phase characteristics

The FC bit changes the phase characteristics of the phase comparator. Both the internal charge pump output level (D_O) and the phase comparator output (ϕR, ϕP) are reversed according to the FC bit. Also, the monitor pin (f_{OUT}) output is controlled by the FC bit. The relationship between the FC bit and each of D_O, ϕR, and ϕP is shown below.

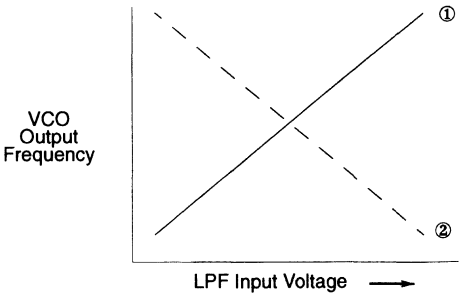
Table. 7 FC Bit Data Setting (LDS = "H")

	FC = High				FC = Low			
	Do	φR	φP	LD/fout	Do	φR	φP	LD/fout
$f_r > f_p$	H	L	L	(fr)	L	H	Z*	(fp)
$f_r < f_p$	L	H	Z*	(fr)	H	L	L	(fp)
$f_r = f_p$	Z*	L	Z*	(fr)	Z*	L	Z*	(fp)

* : High impedance

When designing a synthesizer, the FC pin setting depends on the VCO and LPF characteristics.

*: When the LPF and VCO characteristics are similar to ① , set FC bit high.
*: When the VCO characteristics are similar to ②, set FC bit low.



Power Saving Mode (Intermittent Mode Control Circuit)

Setting a PS pin to Low, the IC enters into power saving mode resultatly current sonsumption can be limited to 10μA (max.). Setting PS pin to High, power saving mode is released so that the IC works normally.
In addition, the intermittent operation control circuit is included which helps smooth start up from the power saving mode. In general, the power consumption can be saved by the intermittent operation that powering down or waking up the synthesizer. Such case, if the PLL is powered up uncontrolled, the resulting phase comparator output signal is unpredictable due to an undefined phase relation between reference frequency (f_r) and comparison frequency (f_p) and may in the worst case take longer time for lock up of the loop.
To prevent this, the intermittent operation control circuit enforces a limited error signal output of the phase detector during power up, thus keeping the loop locked.
During the power saving mode, the corresponding section except for indispensable circuit for the power saving function stops working, then current consumption is reduced to 10 μA (max.).
At that time, the Do and LD become the same state as when a loop is locking. That is, the Do becomes high impedance.
A VCO control voltage is naturally kept at the locking voltage which defined by a LPF"s time constant. As a result of this, VCO's frequency is kept at the locking frequency.

Note: • *While the power saving mode is executed, ZC pin should be set at "H" or open. If ZC is set at "L" during power saving mode, approximately 10 μA current flows.*
- *PS pin must be set "L" at Power-ON.*
- *The power saving mode can be released (PS : L → H) 1μs later after power supply remains stable.*
- *During the power saving mode, it is possible to input the serial data.*

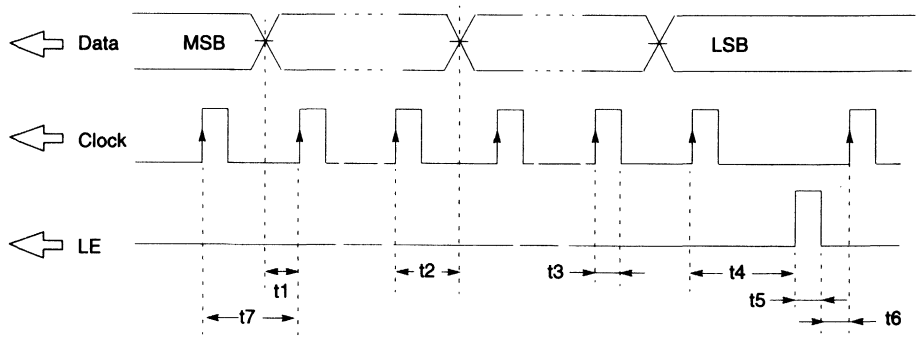
Table.8 PS Pin Setting

PS pin	Status
H	Normal mode
L	Power saving mode

Table.9 ZC Pin Setting

ZC pin	Do output
H	Normal output
L	High impedance

■ SERIAL DATA INPUT TIMING

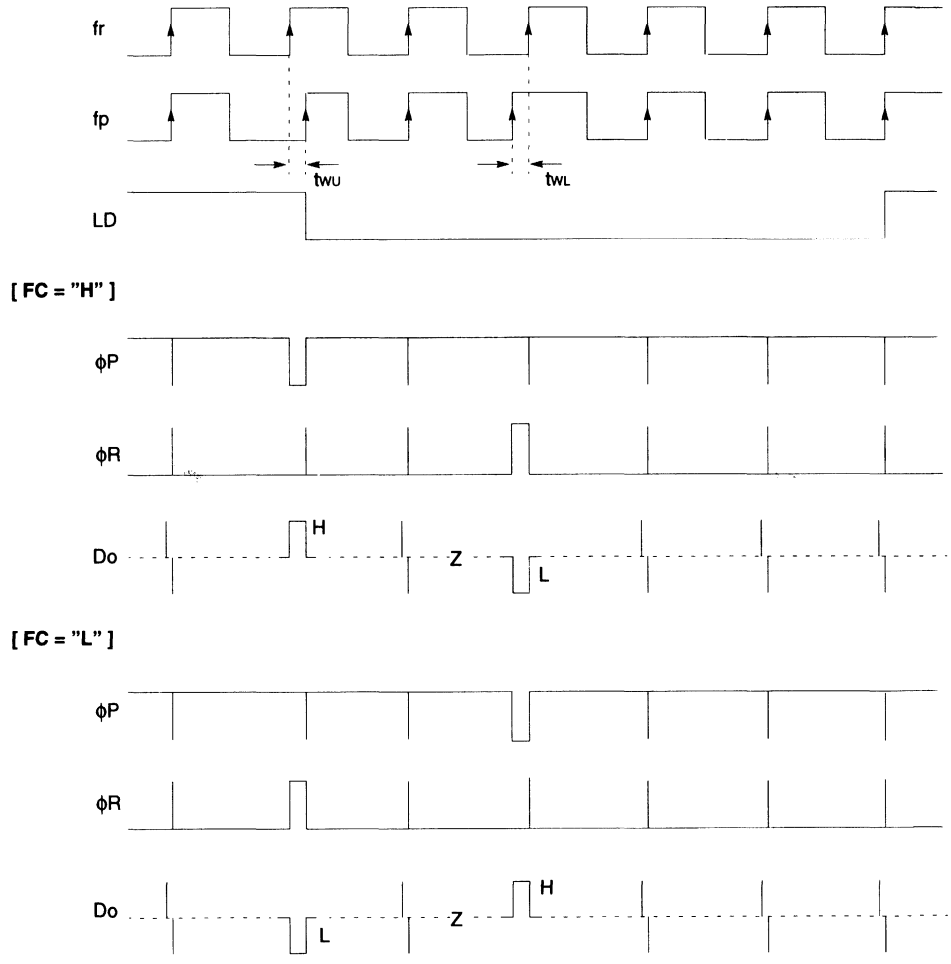


On rising edge of the clock, one bit of the data is transferred into the shift register.

Parameter	Min.	Typ.	Max.	Unit
t1	20	–	–	ns
t2	20	–	–	ns
t3	30	–	–	ns
t4	30	–	–	ns

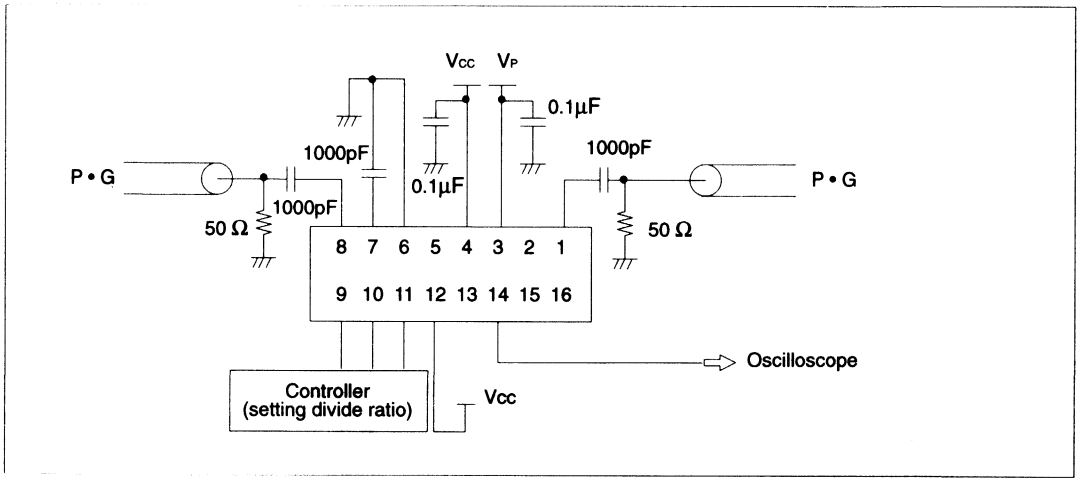
Parameter	Min.	Typ.	Max.	Unit
t5	100	–	–	ns
t6	20	–	–	ns
t7	100	–	–	ns

■ PHASE COMPARATOR OUTPUT WAVEFORM

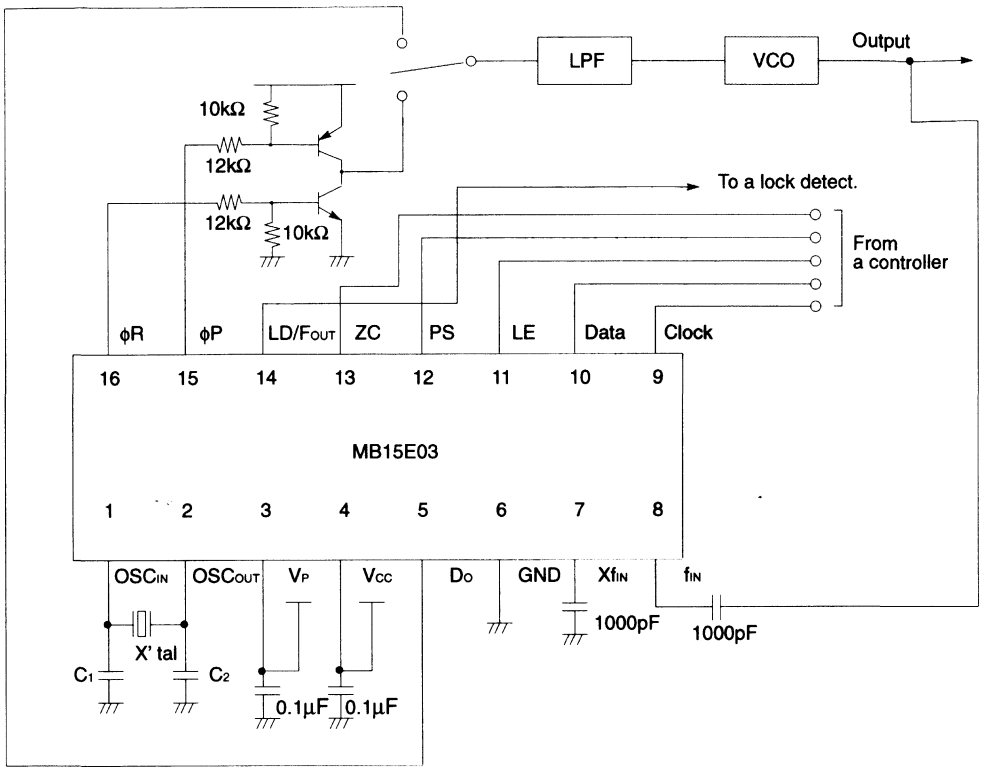


Notes:
1. Phase error detection range: -2π to $+2\pi$
2. Pulses on Do output signal during locked state are output to prevent dead zone.
3. LD output becomes low when phase is twu or more. LD output becomes high when phase error is twL or less and continues to be so for three cysles or more.
4. twu and twL depend on OSCin input frequency.
   twu ≥ 8/fosc (e. g. twu ≥ 625ns, foscin = 12.8 MHz)
   twL ≤ 16/fosc (e. g. twL ≤ 1250ns, foscin = 12.8 MHz)
5. LD becomes high during the power saving mode (PS = "L".)

■ TEST CIRCUIT (for Measuring Input Sensitivity fin/OSCin)



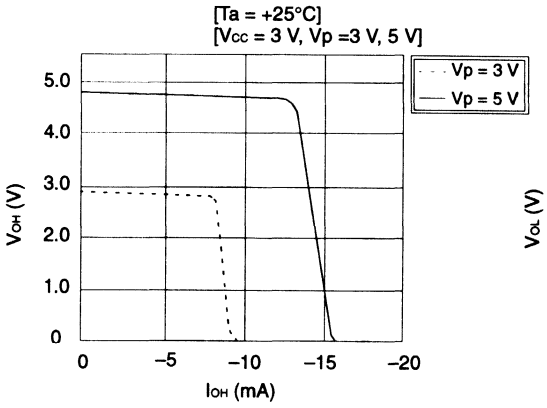
■ APPLICATION EXAMPLE

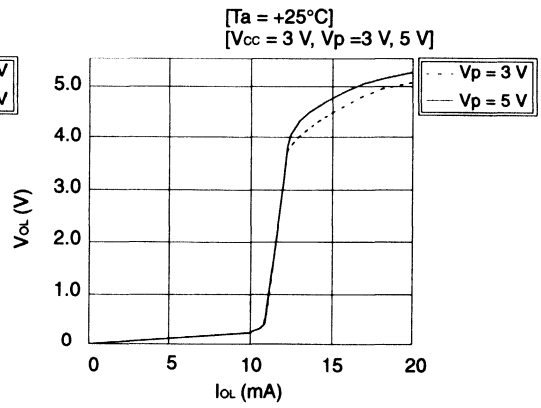


C_1, C_2 : Depend on the crystal parameters

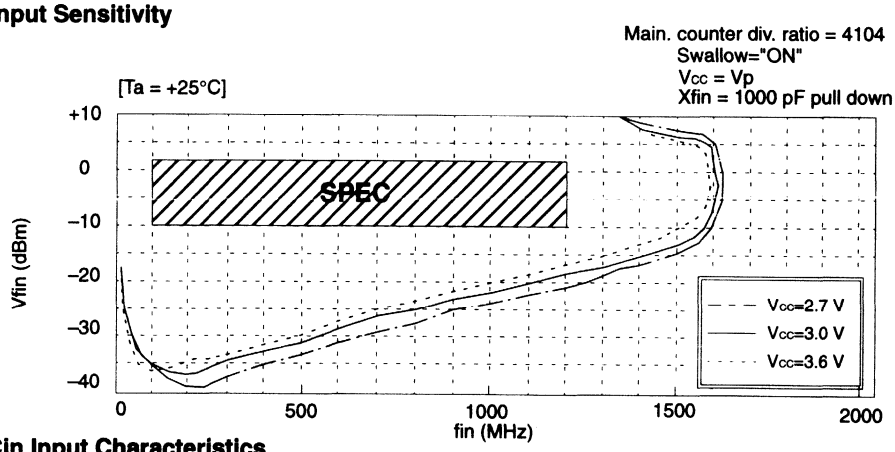
■ TYPICAL CHARACTERISTICS

Do Output Current

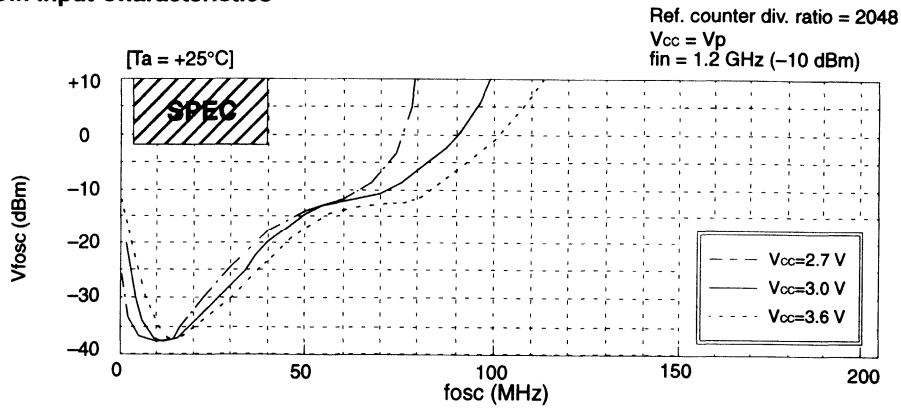




fin Input Sensitivity



OSCin Input Characteristics



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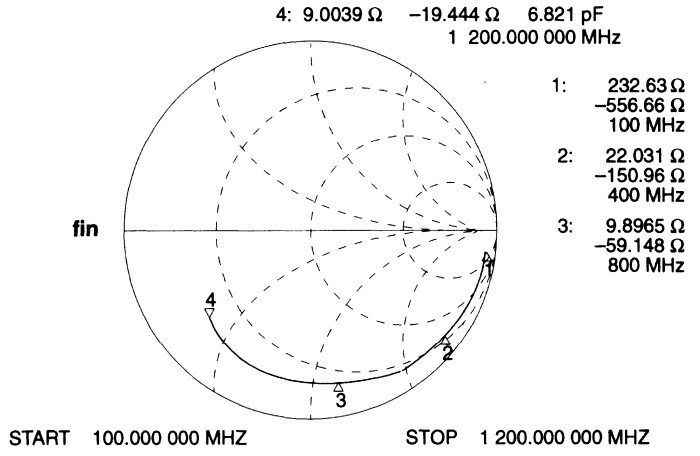
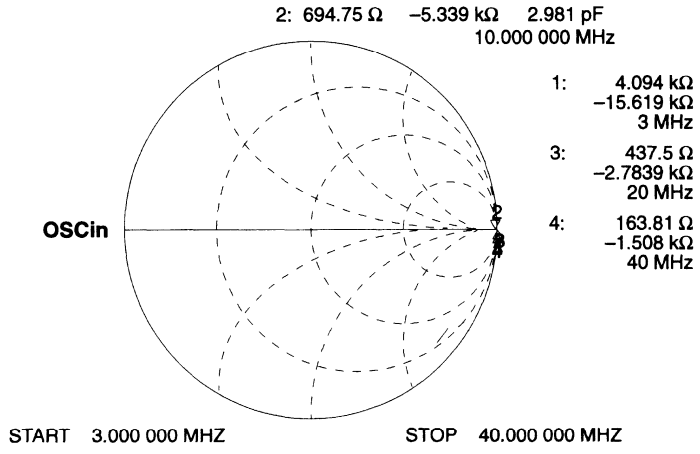
fin Input Impedance



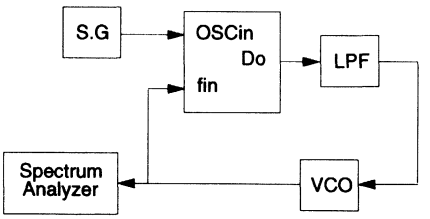
OSCin Input Impedance



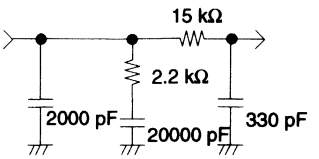
■ REFERENCE INFORMATION

Typical plots measured with the test circuit are shown below. Each plot shows lock up time, phase noise and reference leakage.

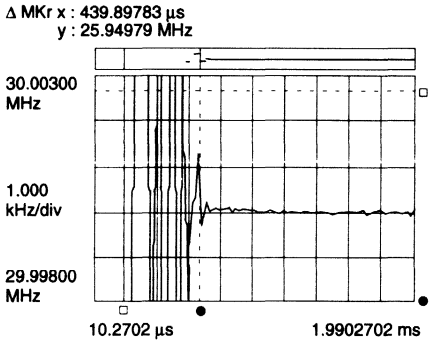
Test Circuit



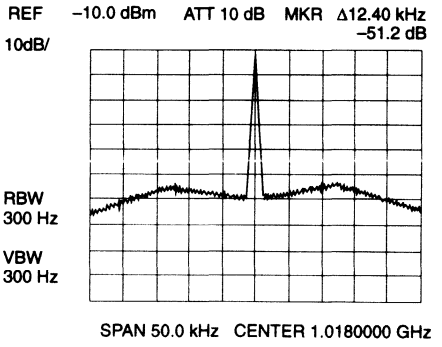
- fvco = 1018 MHz
- Kv = 20 MHz/v
- fr = 200 kHz
- fosc = 13 MHz
- LPF:



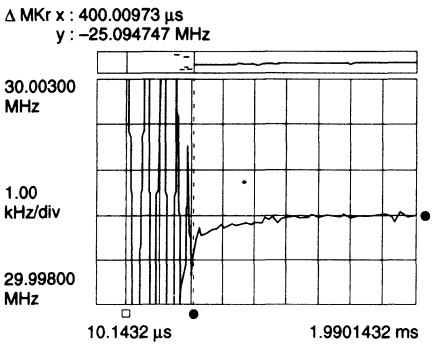
PLL Lock Up Time = 440 µs
(1005.000 MHz → 1031.000 MHz, within ± 1kHz)



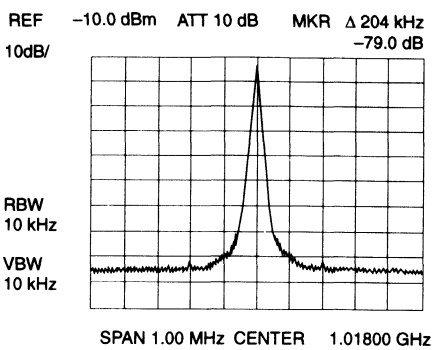
PLL Phase Noise
@ within loop band = 76.2 dBc/Hz



PLL Lock Up Time = 400 µs
(1031.000 MHz → 1005.000 MHz, within ± 1kHz)



PLL Reference Leakage
@ 200 kHz offset = 79.0 dBc



■ ORDERING INFORMATION

Part number	Package	Remarks
MB15E03PFV1	16-pin Plastic SSOP (FPT-16P-M05)	

FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-21341-1E

ASSP

Dual Serial Input PLL Frequency Synthesizer

MB15F02

■ DESCRIPTION

The Fujitsu MB15F02 is a serial input Phase Locked Loop (PLL) frequency synthesizer with a 2.0 GHz and a 500 MHz prescalers. A 64/65 or a 128/129 for the 1.2 GHz prescaler, and a 16/17 or a 32/33 for 500 MHz prescaler can be selected that enables pulse swallow operation.

The latest BiCMOS process technology is used, resultantly a supply current is limited as low as 6.0 mA typ. at a supply voltage of 3.0 V.

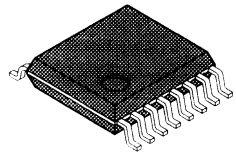
Furthermore, a super charger circuit is included to provide a fast tuning as well as low noise performance. As a result of this, MB15F02 is ideally suitable for digital mobile communications, such as GSM (Global System for Mobile Communications).

■ FEATURES

- High frequency operation RF synthesizer : 1.2 GHz max.
  IF synthesizer : 500 MHz max.
- Low power supply voltage: V_{CC} = 2.7 to 3.6V
- Very Low power supply current : I_{CC} = 6.0 mA typ. (V_{CC} = 3 V)
- Power saving function : I_{PS1} = I_{PS2} = 0.1 µA typ.
- Serial input 14–bit programmable reference divider: R = 5 to 16,383
- Serial input 18–bit programmable divider consisting of:
  - Binary 7–bit swallow counter: 0 to 127
  - Binary 11–bit programmable counter: 5 to 2,047
- On–chip high performance charge pump circuit and phase comparator, achieving high–speed lock–up and low phase noise
- Wide operating temperature: Ta = –40 to 85°C
- Plastic 16-pin SSOP package (FPT-16P-M05)

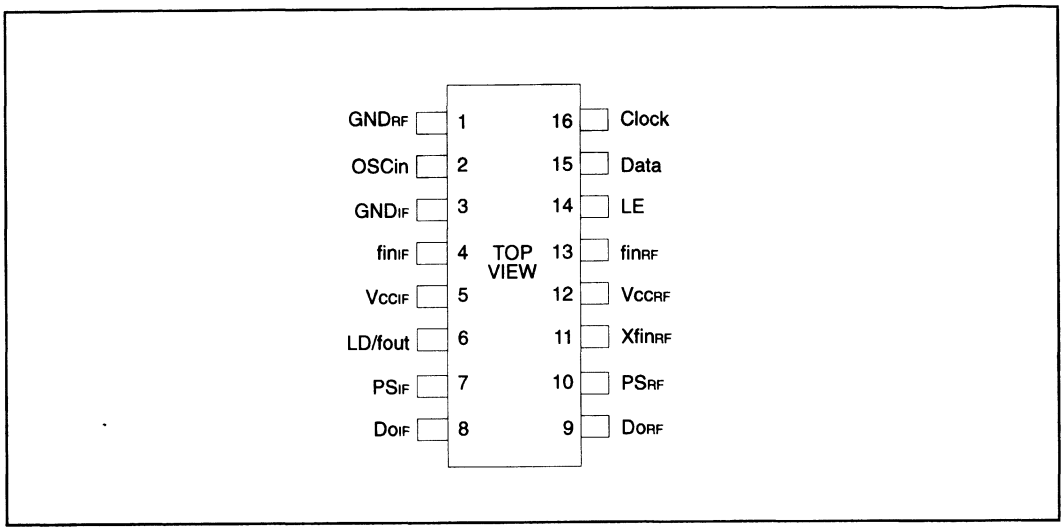
■ PACKAGE

16-pin, Plastic SSOP



(FPT-16P-M05)

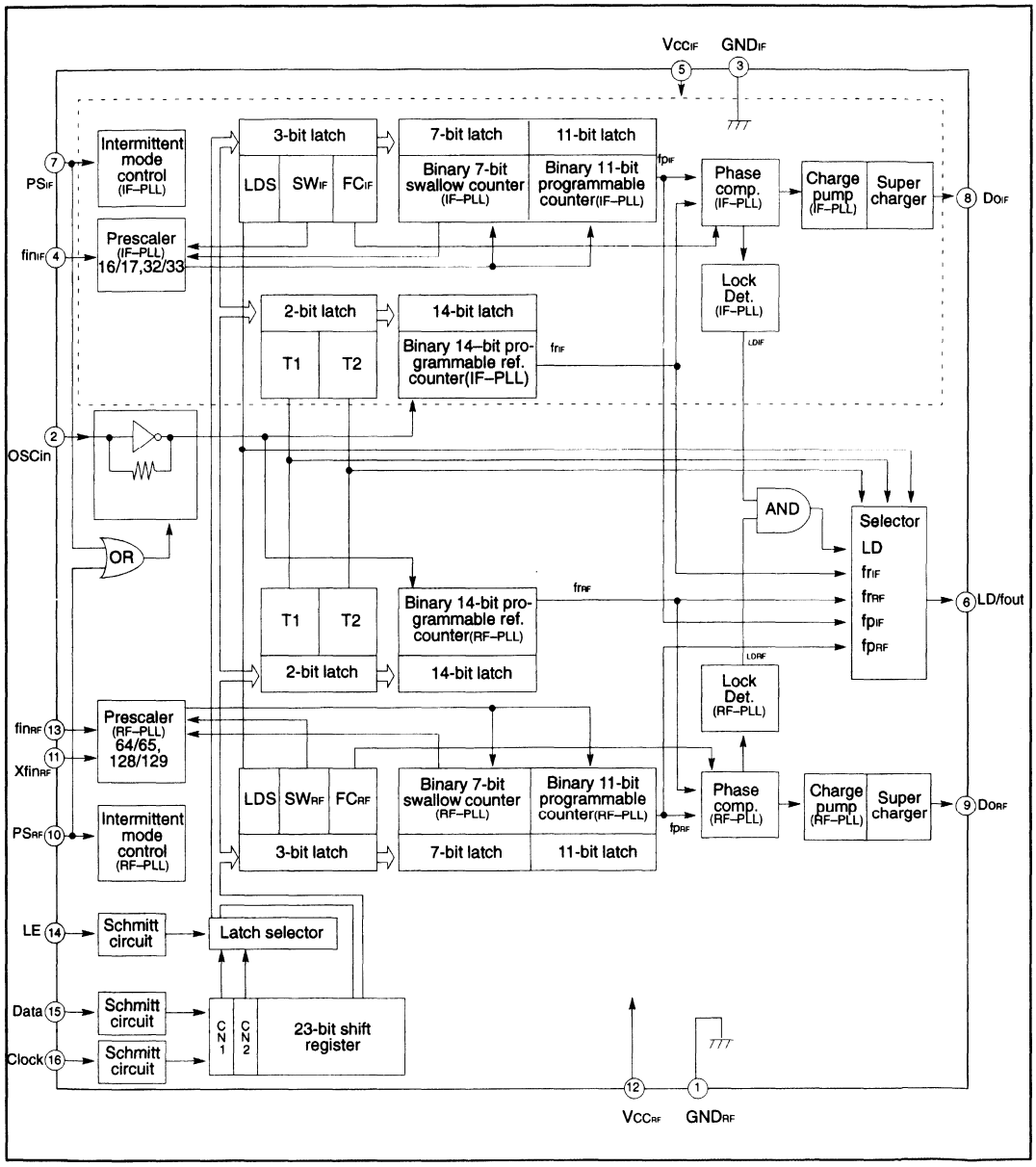
■ PIN ASSIGNMENT



■ PIN DESCRIPTIONS

Pin No.	Pin name	I/O	Descriptions
1	GND_{RF}	–	Ground for RF–PLL section.
2	OSCin	I	The programmable reference divider input. TCXO should be connected with a coupling capacitor.
3	GND_{IF}	–	Ground for the IF-PLL section.
4	fin_{IF}	I	Prescaler input pin for the IF-PLL. The connection with VCO should be AC coupling.
5	V_{CCIF}	–	Power supply voltage input pin for the IF-PLL section.
6	LD/fout	O	Lock detect signal output (LD) / phase comparator monitoring output (fout) The output signal is selected by a LDS bit in a serial data. LDS bit = "H" ; outputs fout signal LDS bit = "L" ; outputs LD signal
7	PS_{IF}	I	Power saving mode control for the IF-PLL section. This pin must be set at "L" Power-ON. (Open is prohibited.) PS_{IF} = "H" ; Normal mode PS_{IF} = "L" ; Power saving mode
8	Do_{IF}	O	Charge pump output for the IF-PLL section. Phase characteristics of the phase detector can be reversed by FC-bit.
9	Do_{RF}	O	Charge pump output for the RF-PLL section. Phase characteristics of the phase detector can be reversed by FC-bit.
10	PS_{RF}	I	Power saving mode control for the RF-PLL section. This pin must be set at "L" Power-ON. (Open is prohibited.) PS_{RF} = "H" ; Normal mode PS_{RF} = "L" ; Power saving mode
11	$Xfin_{RF}$	I	Prescaler complimentary input for the RF-PLL section. This pin should be grounded via a capacitor.
12	V_{CCRF}	–	Power supply voltage input pin for the RF-PLL section, the shift register and the oscillator input buffer.
13	fin_{RF}	I	Prescaler input pin for the RF-PLL. The connection with VCO should be AC coupling.
14	LE	I	Load enable signal input (with the schmitt trigger circuit.) When LE is "H", data in the shift register is transferred to the corresponding latch according to the control bit in a serial data.
15	Data	I	Serial data input (with the schmitt trigger circuit.) A data is transferred to the corresponding latch (IF-ref counter, IF-Prog. counter, RF-ref. counter, RF-prog. counter) according to the control bit in a serial data.
16	Clock	I	Clock input for the 23-bit shift register (with the schmitt trigger circuit.) One bit data is shifted into the shift register on a riging edge of the clock.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Remark
Power supply voltage	V_{CC}	−0.5 to +4.0	V	
Input voltage	V_I	−0.5 to V_{CC} +0.5	V	
Output voltage	V_O	−0.5 to V_{CC} +0.5	V	
Storage temperature	T_{STG}	−55 to +125	°C	

Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power supply voltage	V_{CC}	2.7	3.0	3.6	V	
Input voltage	V_I	GND	–	V_{CC}	V	
Operating temperature	Ta	−40	–	+85	°C	

Handling Precautions

- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover workbenches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

■ ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.7 to 3.6 V, Ta = −40 to +85°C)

Parameter		Symbol	Condition	Value			Unit
				Min.	Typ.	Max.	
Power supply current		I_{CCIF}*1	fin_{IF} = 500 MHz, fosc = 12 MHz	–	2.5	–	mA
		I_{CCRF}*2	fin_{RF} = 1200 MHz, fosc = 12 MHz	–	3.5	–	
Power saving current		Ips_{IF}	V_{CCIF} current at PS_{IF} ="L"	–	0.1*3	10	μA
		Ips_{RF}	V_{CCRF} current at $PS_{IF/RF}$ ="L"	–	0.1*3	10	
Operating frequency	fin_{IF}	fin_{IF}*4	IF–PLL	50	–	500	MHz
	fin_{RF}	fin_{RF}*4	RF–PLL	100	–	1200	
	OSCin	fosc		3	–	40	
Input sensitivity	fin_{IF}	$Vfin_{IF}$	IF–PLL, 50 Ω load system (Refer to the TEST CIRCUIT)	−10	–	+2	dBm
	fin_{RF}	$Vfin_{RF}$	RF–PLL, 50 Ω load system (Refer to the TEST CIRCUIT)	−10	–	+2	dBm
	OSCin	V_{OSC}		0.5	–	V_{CC}	Vp-p
Input voltage	Data, Clock, LE	V_{IH}	Schmitt trigger input	V_{CC}×0.7+0.4	–		V
		V_{IL}	Schmitt trigger input	–	–	V_{CC}×0.3–0.4	
	PS_{IF}, PS_{RF}	V_{IH}		V_{CC}×0.7	–		V
		V_{IL}		–	–	V_{CC}×0.3	
Input current	Data, Clock, LE, PS_{IF}, PS_{RF}	I_{IH}*5		−1.0		+1.0	μA
		I_{IL}*5		−1.0	–	+1.0	
	OSCin	I_{IH}		0	–	+100	μA
		I_{IL}*5		−100	–	0	
Output voltage	LD/fout	V_{OH}	Vcc = 3.0 V, I_{OH} = −1 mA	V_{CC}−0.4	–		V
		V_{OL}	Vcc = 3.0 V, I_{OL} = 1 mA	–	–	0.4	
	Do_{IF}, Do_{RF}	V_{DOH}	Vcc = 3.0 V, I_{OH} = −1 mA	V_{CC}−0.4	–		V
		V_{DOL}	Vcc = 3.0 V, I_{OL} = 1 mA	–	–	0.4	
High impedance cutoff current	Do_{IF}, Do_{RF}	I_{OFF}	Vcc = 3.0 V, V_{OFF} = GND to Vcc	–	–	1.1	μA
Output current	LD/fout	I_{OH}*5	Vcc = 3.0 V	–	–	−1.0	mA
		I_{OL}	Vcc = 3.0 V	1.0	–	–	
	Do_{IF}, Do_{RF}	I_{DOH}*5	Vcc = 3.0 V, V_{DOH} = 2.0 V, Ta = 25°C	−11	–	−6	mA
		I_{DOL}	Vcc = 3.0 V, V_{DOL} = 1.0 V, Ta = 25°C	8	–	15	

*1: Conditions ; V_{CCIF} = 3.0 V, Ta = 25°C, in locking state.

*2: Conditions; V_{CCRF} = 3.0 V, Ta = 25°C, in locking state.

*3: Conditions ; Vcc = 3.0 V, fosc = 12.8 MHz (−2 dB), Ta = 25°C

*4: AC coupling. The minimum frequency is specified with a connecting coupling capacitor of 1000 pF.

*5: The symbol "−" means direction of current flow.

■ FUNCTIONAL DESCRIPTIONS

The divide ratio can be calculated using the following equation:

$f_{VCO} = \{(M \times N) + A\} \times f_{OSC} + R \quad (A < N)$

f_{VCO}: Output frequency of external voltage controlled ocillator (VCO)
M: Preset divide ratio of dual modulus prescaler (16 or 32 for IF-PLL, 64 or 128 for RF-PLL)
N: Preset divide ratio of binary 11-bit programmable counter (5 to 2,047)
A: Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$)
f_{OSC}: Reference oscillation frequency
R: Preset divide ratio of binary 14-bit programmable reference counter (5 to 16,383)

Serial Data Input

Serial data is entered using three pins, Data pin, Clock pin, and LE pin. Programmable dividers of IF/RF–PLL sections, programmable reference dividers of IF/RF PLL sections are controlled individually.
Serial data of binary data is entered through Data pin.
On rising edge of clock, one bit of serial data is transferred into the shift register. When load enable signal is high, the data stored in the shift register is transferred to one of latch of them depending upon the control bit data setting.

Table1. Control Bit

Control bit		Destination of serial data
CN1	CN2	
L	L	The programmable reference counter for the IF-PLL.
H	L	The programmable reference counter for the RF-PLL.
L	H	The programmable counter and the swallow counter for the IF-PLL
H	H	The programmable counter and the swallow counter for the RF-PLL

Shift Register Configuration

Programmable Reference Counter

LSB ↓ Data Flow ⟶ MSB ↓

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
CN1	CN2	T1	T2	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14

CNT1, 2 : Control bit [Table. 1]
R1 to R14 : Divide ratio setting bits for the programmable reference counter (5 to 16,383) [Table. 2]
T1, 2 : Test purpose bit [Table. 3]
NOTE: Start data input with MSB first.

Programmable Counter

LSB ↓ Data Flow → MSB ↓

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
CN1	CN2	LDS	SW	FC	A1	A2	A3	A4	A5	A6	A7	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11

CNT1, 2 : Control bit [Table. 1]
N1 to N14 : Divide ratio setting bits for the programmable counter (5 to 2,047) [Table. 4]
A1 to A7 : Divide ratio setting bits for the swallow counter (0 to 127) [Table. 5]
SW : Divide ratio setting bit for the prescaler (16/17 or 32/33 for the IF-PLL, 64/65 or 128/129 for the RF-PLL) [Table. 6]
FC : Phase control bit for the phase detector [Table. 7]
LDS : LD/fout signal select bit [Table. 8]
NOTE: Start data input with MSB first.

Table2. Binary 14-bit Programmable Reference Counter Data Setting

Divide ratio (R)	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1
5	0	0	0	0	0	0	0	0	0	0	0	1	0	1
6	0	0	0	0	0	0	0	0	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: • Divide ratio less than 5 is prohibited.

Table.3 Test Purpose Bit Setting

T1	T2	LD/fout pin state
L	L	Outputs f_{RIF}
H	L	Outputs f_{RRF}
L	H	Outputs f_{PIF}
H	H	Outputs f_{PRF}

Table.4 Binary 11-bit Programmable Counter Data Setting

Divide ratio (N)	N 11	N 10	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1
5	0	0	0	0	0	0	0	0	1	0	1
6	0	0	0	0	0	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.	.	.	.
2047	1	1	1	1	1	1	1	1	1	1	1

Note: • Divide ratio less than 5 is prohibited.

Table.5 Binary 7-bit Swallow Counter Data Setting

Divide ratio (A)	A 7	A 6	A 5	A 4	A 3	A 2	A 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.
127	1	1	1	1	1	1	1

Note: • Divide ratio (A) range = 0 to 127

Table. 6 Prescaler Data Setting

		SW = "H"	SW = "L"
Prescaler divide ratio	IF-PLL	16/17	32/33
	RF-PLL	64/65	128/129

Table. 7 Phase Comparator Phase Switching Data Setting

	$FC_{IF/RF}$ = H	$FC_{IF/RF}$ = L
	$DO_{IF/RF}$	
fr > fp	H	L
fr = fp	Z	Z
fr < fp	L	H
VCO polarity	①	②

Note: • Z = High–impedance
• Depending upon the VCO and LPF polarity, FC bit should be set.

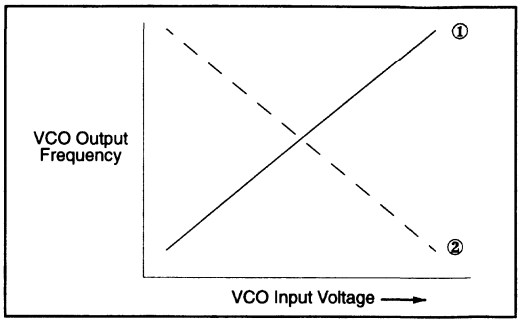
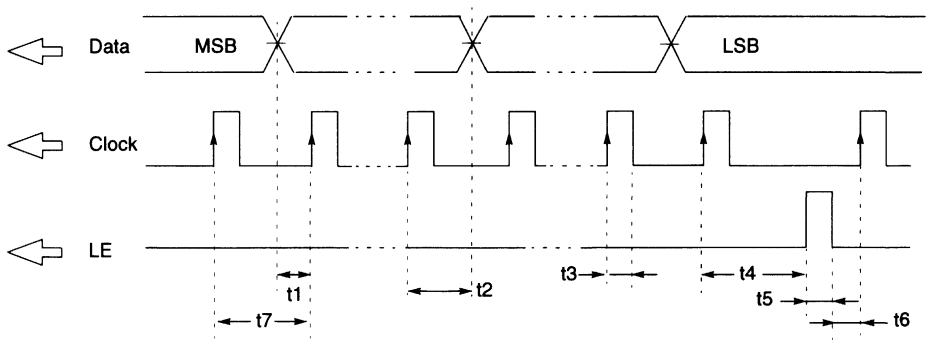


Table. 8 LD/fout Output Select Data Setting

LDS	LD/fout output signal
H	fout ($fr_{IF/RF}$, $fp_{IF/RF}$) signals
L	LD signal

Serial Data Input Timing

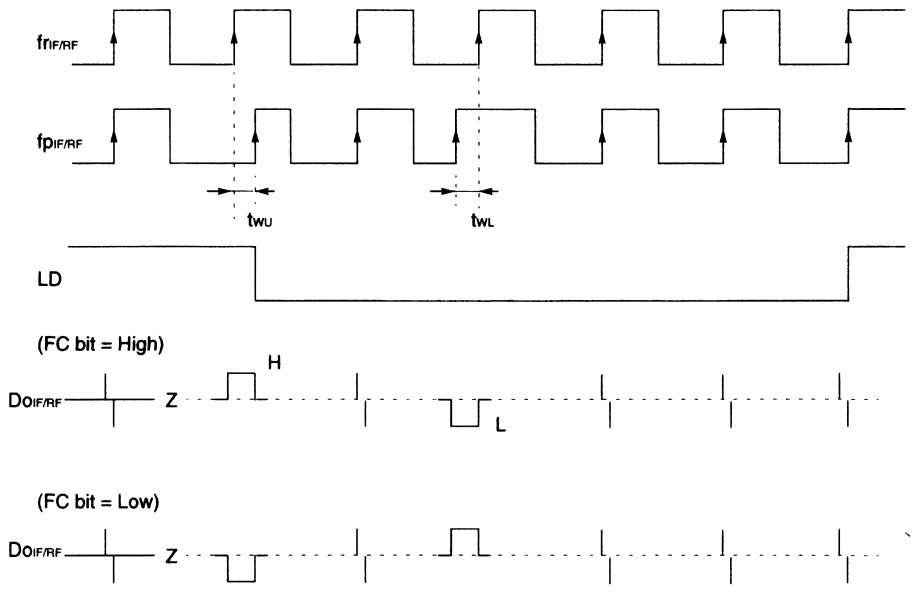


On rising edge of the clock, one bit of the data is transferred into the shift register.

Parameter	Min.	Typ.	Max.	Unit
t1	20	–	–	ns
t2	20	–	–	ns
t3	30	–	–	ns
t4	30	–	–	ns

Parameter	Min.	Typ.	Max.	Unit
t5	100	–	–	ns
t6	20	–	–	ns
t7	100	–	–	ns

■ PHASE DETECTOR OUTPUT WAVEFORM



LD Output Logic Table

IF–PLL section	RF–PLL section	LD output
Locking state / Power saving state	Locking state / Power saving state	H
Locking state / Power saving state	Unlocking state	L
Unlocking state	Locking state / Power saving state	L
Unlocking state	Unlocking state	L

Note: • Phase error detection range = -2π to $+2\pi$

- Pulses on $D_{O_{IF/RF}}$ signals are output to prevent dead zone.
- LD output becomes low when phase error is t_{WU} or more.
- LD output becomes high when phase error is t_{WL} or less and continues to be so for three cycles or more.
- t_{WU} and t_{WL} depend on OSCin input frequency as follows.
  $t_{WU} \geq 8/fosc$: i.e. $t_{WU} \geq 625ns$ when foscin = 12.8 MHz
  $t_{WL} \leq 16/fosc$: i.e. $t_{WL} \leq 1250ns$ when foscin = 12.8 MHz

■ POWER SAVING MODE (Intermittent Mode Control Circuit)

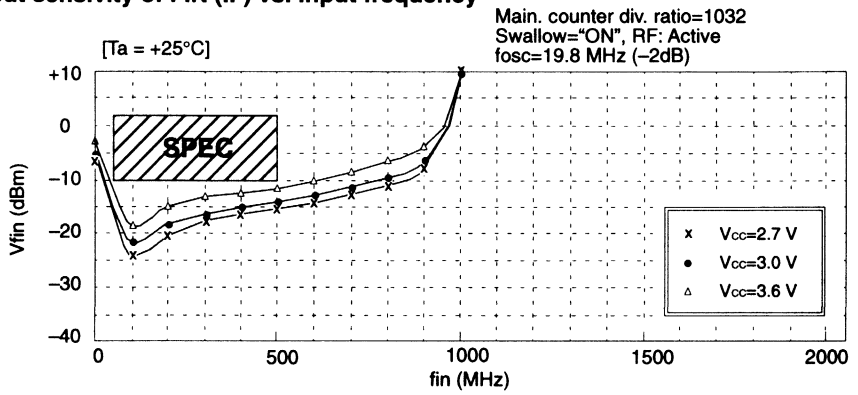
Setting a $PS_{IF(RF)}$ pin to Low, IF-PLL (RF-PLL) enters into power saving mode resultant current consumption can be limited to 10μA (typ.). Setting PS pin to High, power saving mode is released so that the device works normally. In addition, the intermittent operation control circuit is included which helps smooth start up from stand by mode. In general, the power consumption can be saved by the intermittent operation that powering down or waking up the synthesizer. Such case, if the PLL is powered up uncontrolled, the resulting phase comparator output signal is unpredictable due to an undefined phase relation between reference frequency (fr) and comparison frequency (fp) and may in the worst case take longer time for lock up of the loop.
To prevent this, the intermittent operation control circuit enforces a limited error signal output of the phase detector during power up. Thus keeping the loop locked.
Allow 1 μs after frequency stabilization on power-up for exiting the power saving mode (PS: L to H)
Serial data can be entered during the power saving mode.
During the power saving mode, the corresponding section except for indispensable circuit for the power saving function stops working, then current consumption is reduced to 10μA per one PLL section.
At that time, the Do and LD become the same state as when a loop is locking. That is, the Do becomes high impedance.
A VCO control voltage is naturally kept at the locking voltage which defined by a LPF's time constant. As a result of this, VCO's frequency is kept at the locking frequency.

Note: PS pin must be set "L" at Power-ON. The power saving mode should be released at 1 μs after the power supply becomes stable.

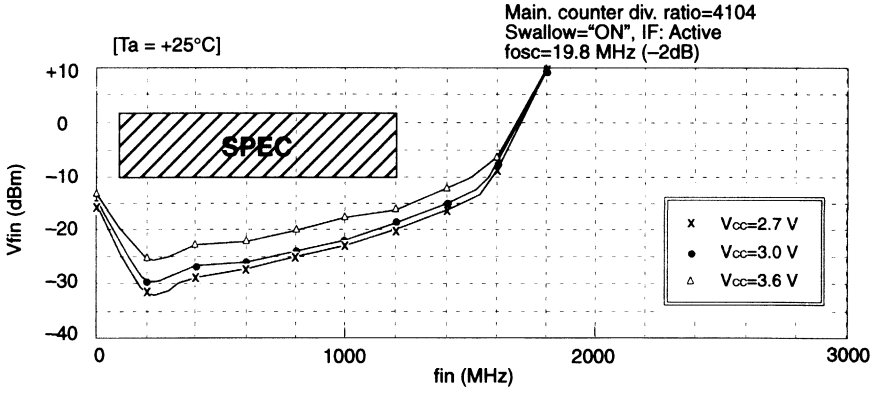
PS_{IF}	PS_{RF}	IF-PLL counters	RF-PLL counters	OSC input buffer
L	L	OFF	OFF	OFF
H	L	ON	OFF	ON
L	H	OFF	ON	ON
H	H	ON	ON	ON

■ TYPICAL CHARACTERISTICS

Input sensivity of FIN (IF) vs. Input frequency



Input sensivity of FIN (RF) vs. Input frequency



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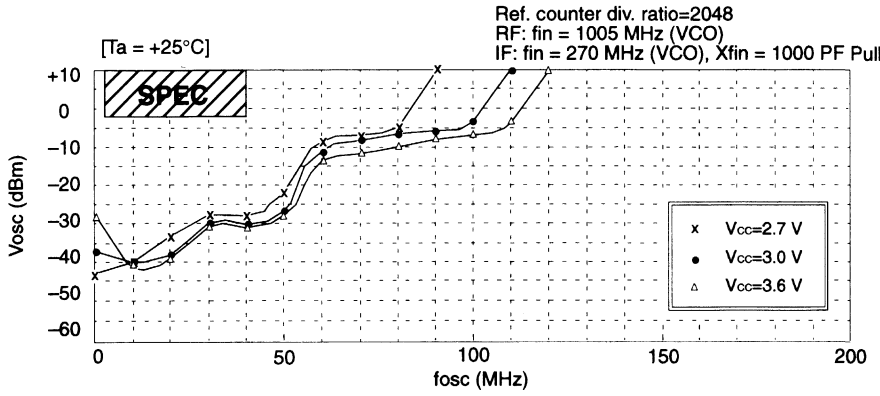
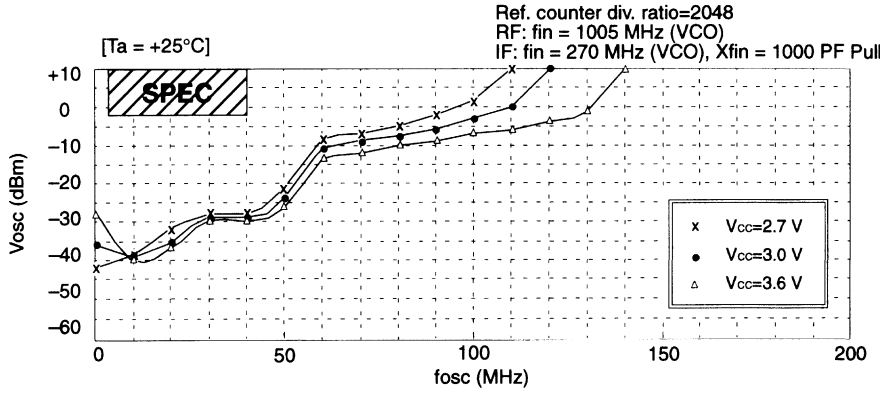
Input sensivity of OSC (IF) vs. Input frequency



Input sensivity of OSC (RF) vs. Input frequency



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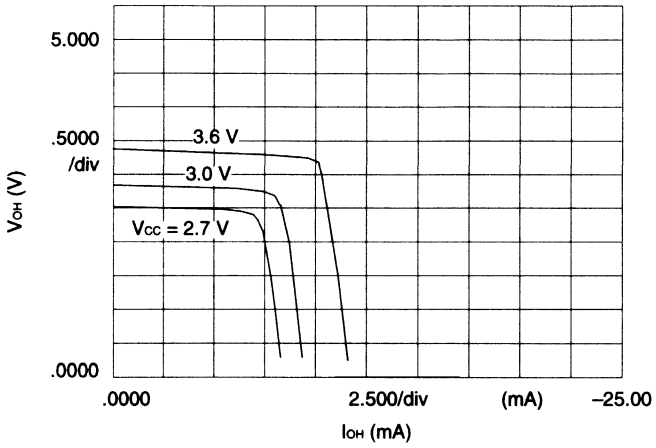
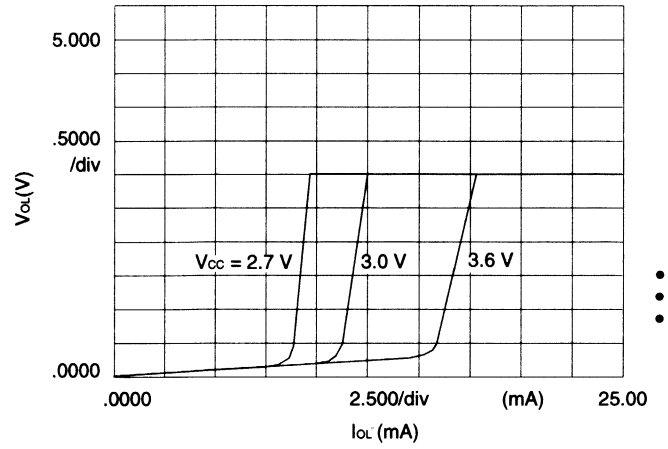
Do output Current (IF)

Conditions: Ta = +25°C
V_{CC}= 2.7, 3.0, 3.6 V



- D_O = V_{CC} = 1 V
- OSCin = 12.8 MHz (+10 dB)
- fin [IF/RF] = "H" (= V_{CC})



- D_O = 1 V
- fin [IF] = 500 MHz (–10 dB)
- OSCin, fin [RF] = "H" (= V_{CC})

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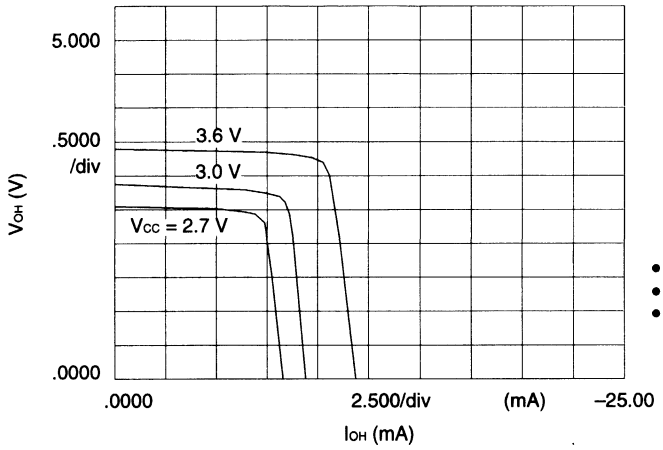
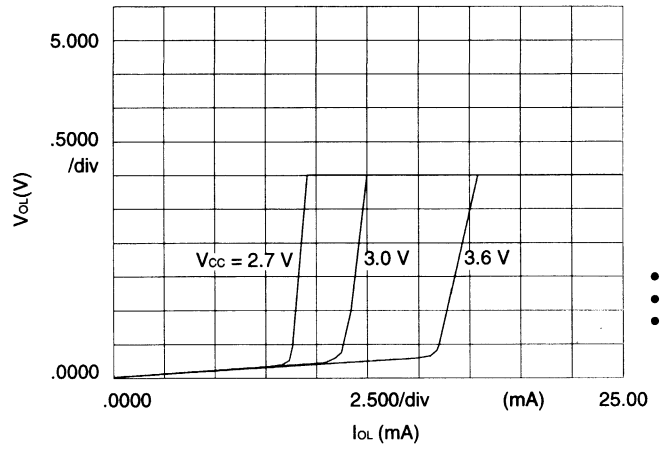
(Continued)

Do output Current (RF)

Conditions: Ta = +25°C
V_{CC}= 2.7, 3.0, 3.6 V



- D_O = V_{CC} = 1 V
- OSCin = 12.8 MHz (+10 dB)
- fin [IF/RF] = "H" (= V_{CC})

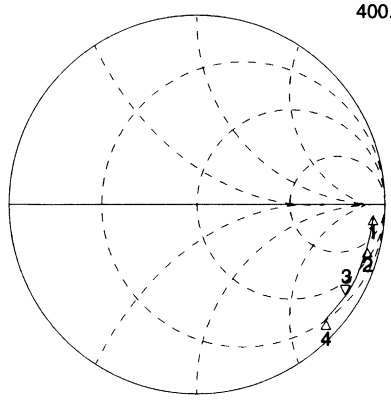


- D_O = 1 V
- fin [RF] = 1.2 GHz (–10 dB)
- OSCin, fin [IF] = "H" (= V_{CC})

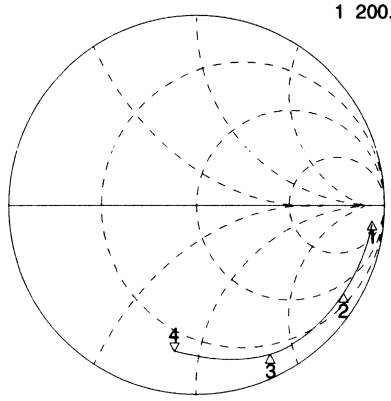
(Continued)

Input Impedance

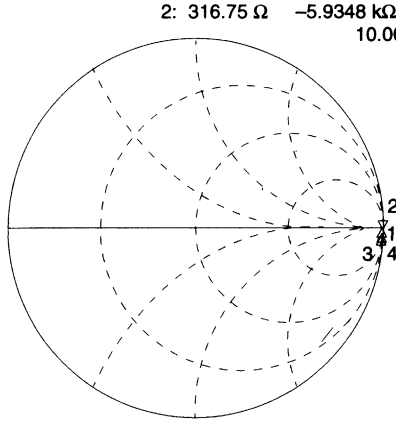
finIF Pin



finRF Pin



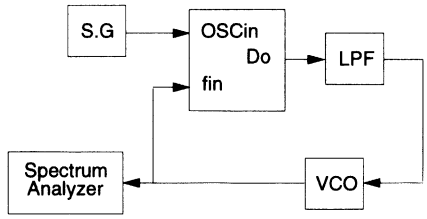
OSCin Pin



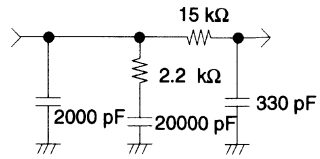
■ REFERENCE INFORMATION

Typical plots measured with the test circuit are shown below. Each plot shows lock up time, phase noise and reference leakage.

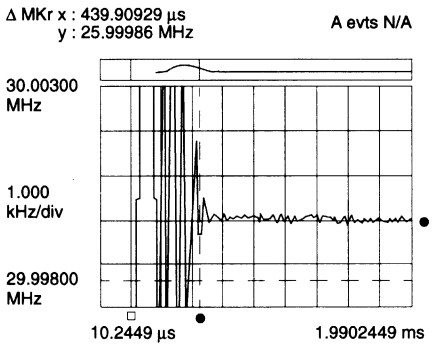
Test Circuit



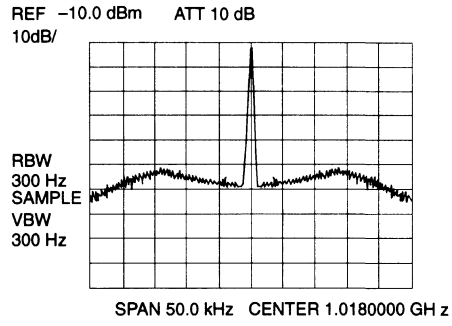
- fvco = 1018 MHz
- Kv = 20 MHz/v
- fr = 200 kHz
- fosc = 13 MHz
- LPF:



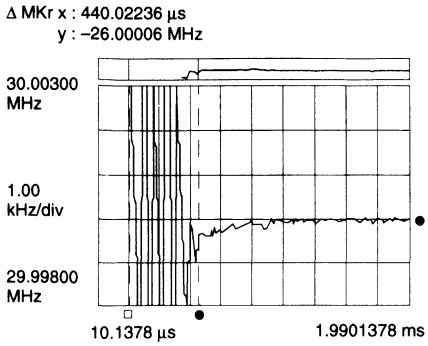
PLL Lock Up Time = 440 µs
(1005.000 MHz → 1031.000 MHz, within ± 1kHz)



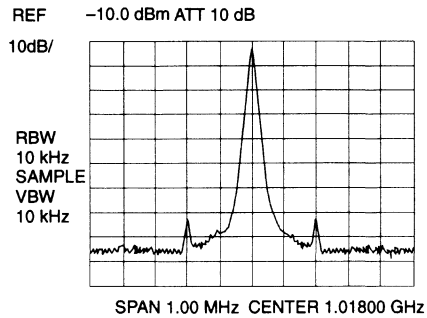
PLL Phase Noise
@ within loop band = 75.5 dBc/Hz



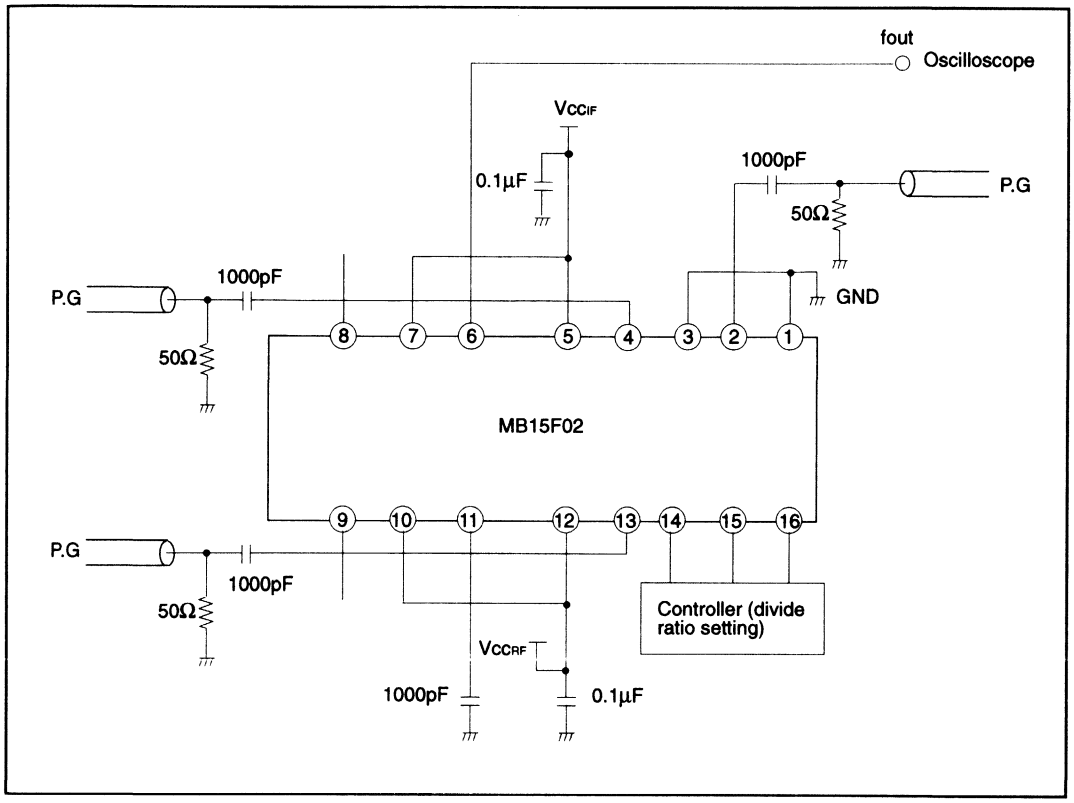
PLL Lock Up Time = 440 µs
(1031.000 MHz → 1005.000 MHz, within ± 1kHz)



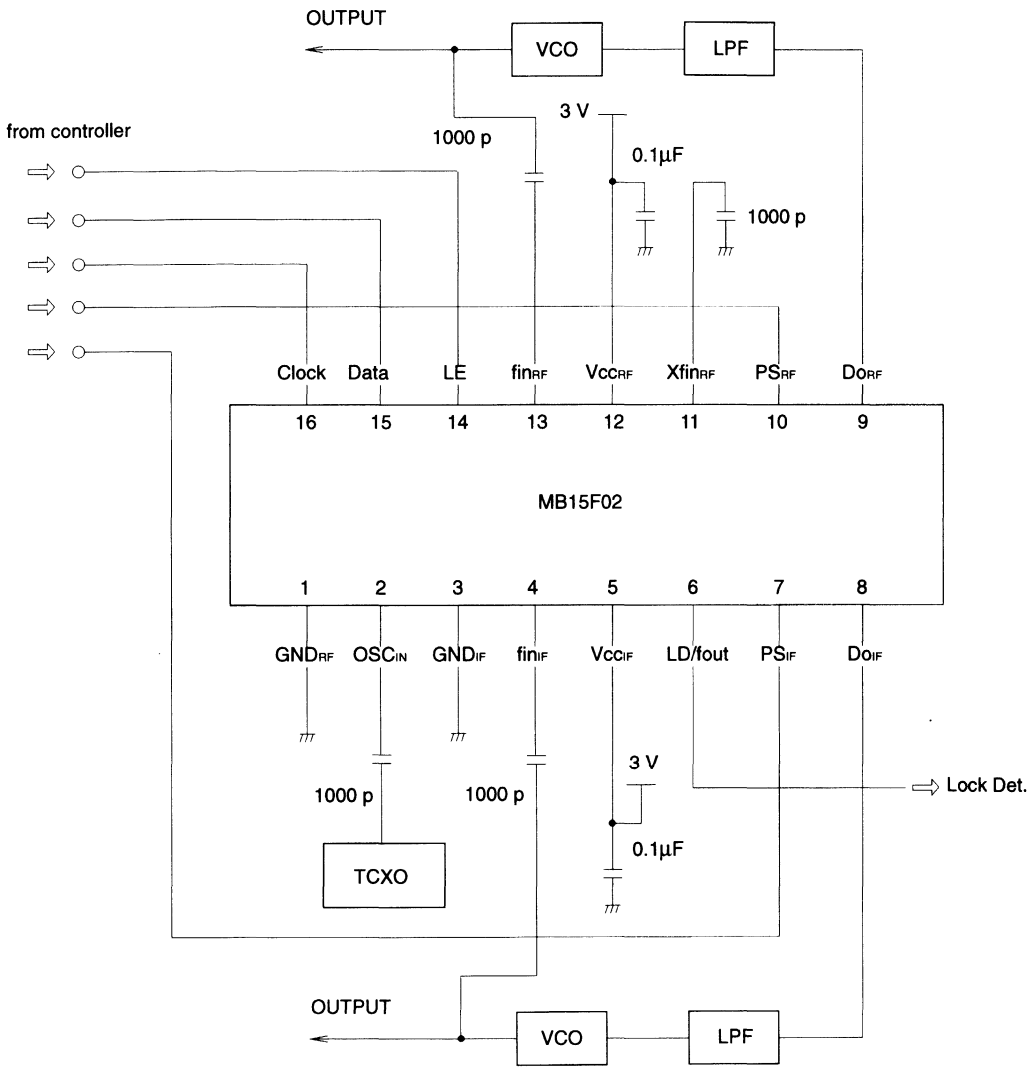
PLL Reference Leakage
@ 200 kHz offset = 71.4 dBc



■ TEST CIRCUIT (Prescaler Input/Programmable Reference Divider Input Sensitivity Test)



■ APPLICATION EXAMPLE



Clock, Data, LE: Schmitt trigger circuit is provided (insert a pull-down or pull-up resistor to prevent oscillation when open-circuited in the input).

■ ORDERING INFORMATION

Part number	Package	Remarks
MB15F02 PFV	16pin, Plastic SSOP (FPT-16P-M05)	

MEMO

FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-21333-1E

ASSP

2.0 GHz High-Speed Tuning PLL Frequency Synthesizer

MB15A17

■ DESCRIPTION

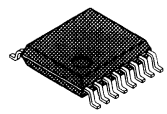
The Fujitsu MB15A17 is a serial input phase-locked loop (PLL) frequency synthesizer with a pulse-swallow function, and is suitable for the digital radio applications such as GSM. MB15A17 achieves the low noise performance as well as the high-speed lock-up which required for digital cellularphones.
The MB15A17 can operate from a single +3 V supply and has an Icc of 12 mA (typical).

■ FEATURES

- High operating frequency : f_{IN} = 2.0 GHz (V_{IN} = –10 dBm)
- Pulse-swallow function : High-speed dual-modules prescaler with selectable 64/65 and 128/129 divide ratios
- Low supply current : I_{CC} = 12 mA typ. at 3 V
- Power saving funtion : I_{PS} = 100 μA typ. (Controlled with PS pin)
- Serial input, 18-bit programmable divider consisting of:
  Binary 7-bit swallow counter : 0 to 127
  Binary 11-bit programmable counter : 5 to 2,047
- Serial input 17-bit programmable reference divider consisting of:
  Binary 14-bit programmable reference counter: 6 to 16,383
  1-bit for setting a prescaler divide ratio (SW bit)
  1-bit for switching a phase polarity (FC bit)
  1-bit for selecting LD/fout (LDS bit)
- On-chip high performance charge pump circuit and phase comparator, achieving high-speed lock-up and low phase noise
- Two types of phase comparator outputs selectable
  On-chip charge pump output
  Output for an external charge pump
- Wide operating temperature range: –40 to +85°C
- Plastic 16-pin SSOP (Shrink Small Outline Package)

■ PACKAGE

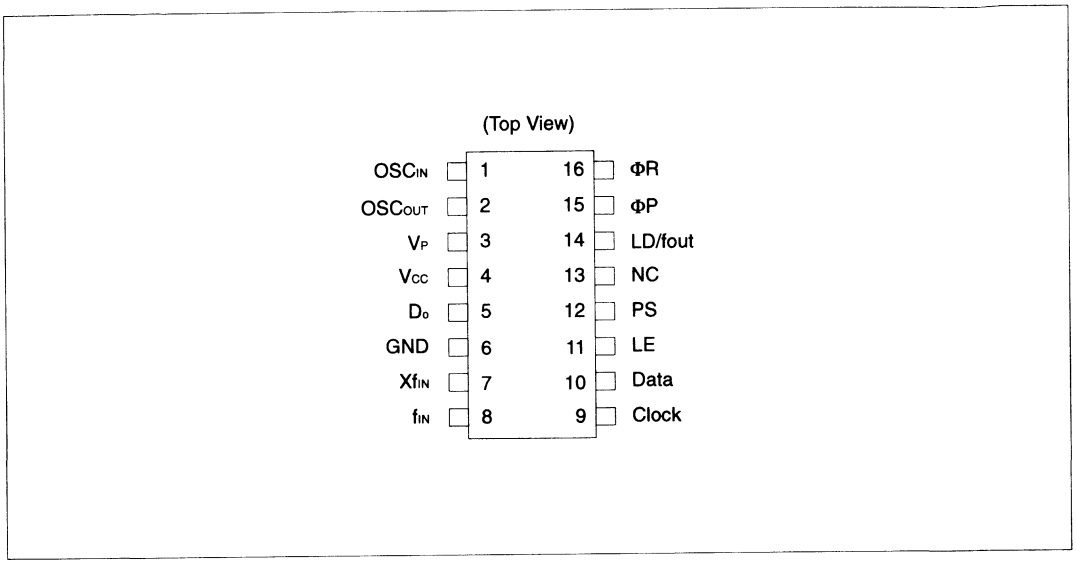
16-pin, Plastic SSOP



(FPT-16P-M05)

This device contains circuitry to protect the inputs against damage due to high static voltages or electroc fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

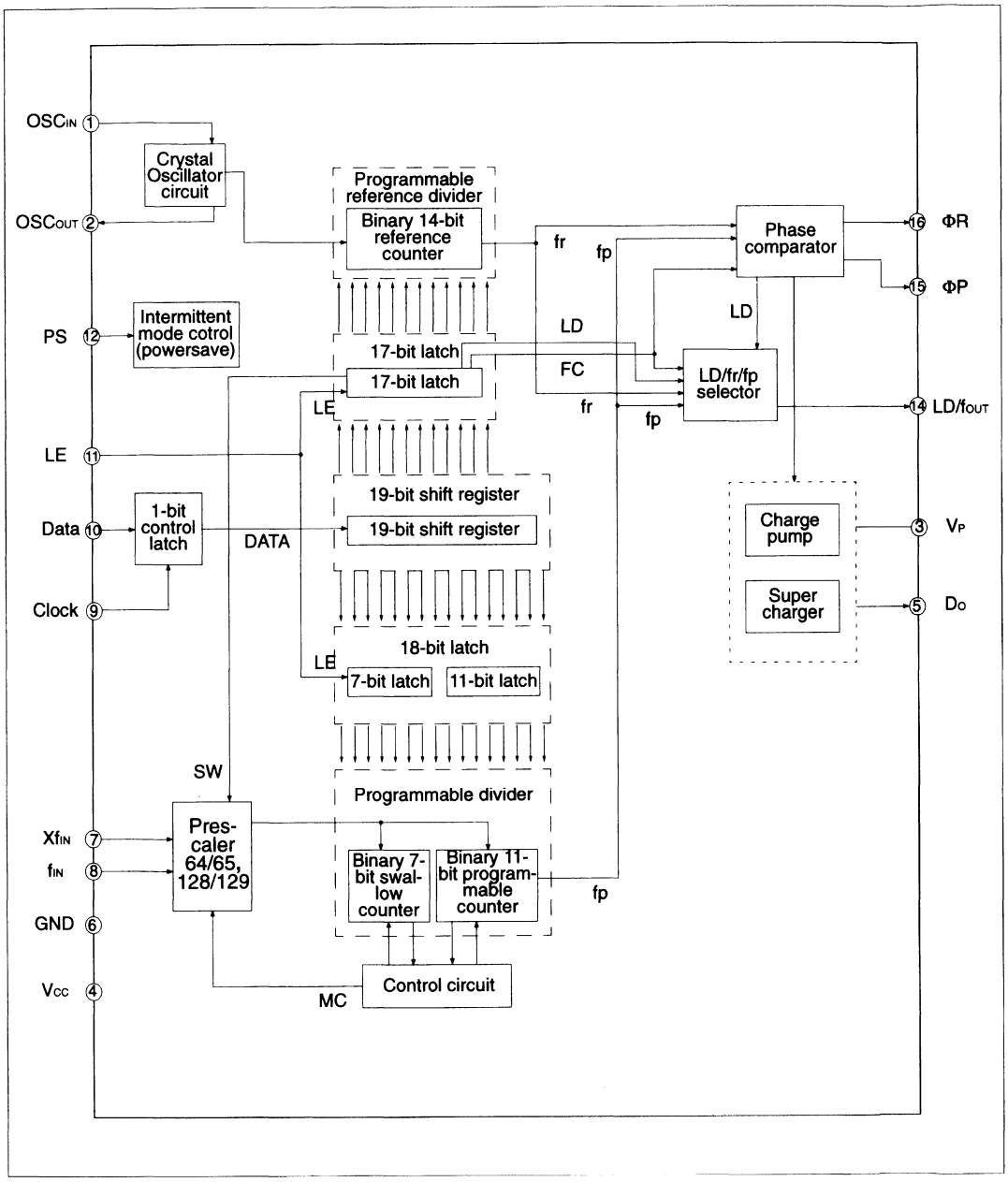
■ PIN ASSIGNMENT



■ PIN DESCRIPTION

Pin No.	Pin name	I/O	Description
1	OSC_{IN}	I	Programmable reference divider input. Oscillator input. Connection for external crystal or TCXO.
2	OSC_{OUT}	O	Oscillator output. Connection for the external crystal.
3	V_P	–	Power supply input for the charge pump.
4	V_{CC}	–	Power supply input.
5	D_O	O	Charge pump output. Phase of the charge pump can be reversed according FC input.
6	GND	–	Ground.
7	Xfin	I	Prescaler complementary input, and should be grounded via a capacitor.
8	fin	I	Prescaler input. Connection with an external VCO should be done AC coupled.
9	Clock	I	Clock input for 19-bit shift register. Data is shifted into the shift register on the rising edge of the clock. (Open is prohibited.)
10	Data	I	Serial data input using binary code. The last bit of the data is a control bit. (Open is prohibited.) Control bit = "H" ; Data is transmitted to the 17-bit latch. Control bit = "L" ; Data is transmitted to the 18-bit latch.
11	LE	I	Load enable signal input (Open is prohibited.) When LE is high, the data of the shift register are transferred to a latch, according to the control bit in the serial data.
12	PS	I	Power saving control input. This pin must be set at "L" at Power-ON. (Open is prohibited.) PS = "H" ; Normal mode PS = "L" ; Power saving mode
13	NC	–	No connection.
14	LD/f_{OUT}	O	Lock detector output(LD)/Monitor pin of the phase comparator(fout). A LDS bit in a serial data switchs LD/fout pin's output. LDS = "H" ; outputs fout LDS = "L" ; outputs LD
15	ΦP	O	Phase comparator output for an external charge pump. Phase of the output is reversed according to FC input. ΦP pin is a N-ch open drain output.
16	ΦR	O	Phase comparator output for an external charge pump. Phase of the output is reversed according to FC input. ΦR pin is a C-MOS output.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Remark
Power supply voltage	V_{CC}	−0.5 to +5.0	V	
	V_P	V_{CC} to 5.5	V	
Output voltage	V_O	−0.5 to V_{CC} +0.5	V	
Open drain voltage	V_{OOP}	−0.5 to 6.0	V	ΦP
Output current	I_O	±10	mA	
Storage temperature	Tstg	−55 to +125	°C	

Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Remark
		Min.	Typ.	Max.		
Power supply voltage	V_{CC}	2.7	3.0	3.6	V	
	V_P	V_{CC}	−	5.0	V	
Input voltage	V_{IN}	GND	−	V_{CC}	V	
Operating temperature	Ta	−40	−	+85	°C	

Handling Precautions

- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover workbenches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

■ ELECTRICAL CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Value			Unit	Condition
			Min.	Typ.	Max.		
Power supply current (Power saving current)		I_{CC} (I_{PS})	–	12 (0.1)	–	mA	With f_{IN} = 2.0 GHz, OSC_{IN} = 12 MHz, V_{CC} = 3.0 V. In locked state.
Operating frequency	f_{IN}	f_{IN}	1000	–	2000	MHz	AC coupling with a 1000 pF capacitor connected.
	OSC_{IN}	f_{OSC}	–	12	23	MHz	
Input sensitivity	f_{IN}	V_{IN}	–10	–	6	dBm	50 Ω (refer to the test circuit.)
	OSC_{IN}	V_{OSC}	0.5	–	–	Vp-p	
High-level input voltage	Data, Clock, LE, PS	V_{IH}	V_{CC} x 0.7	–	–	V	
Low-level input voltage		V_{IL}	–	–	V_{CC} x 0.3	V	
High-level input current	Data, Clock, LE, PS	I_{IH}	–	–	1.0	mA	
Low-level input current		I_{IL}	–1.0	–	–	µA	
Input current	OSC_{IN}	I_{OSC}	–100	–	100	µA	
High-level output voltage	ΦR, LD	V_{OH}	2.1	–	–	V	V_{CC} = 3 V, I_{OH} = –1.0 mA
Low-level output voltage	ΦR, ΦP, LD	V_{OL}	–	–	0.4	V	V_{CC} = 3 V, I_{OL} = 1.0 mA
High-impedance cut off current	D_O, ΦP	I_{OFF}	–	–	0.3	µA	V_P = V_{CC} to 3.6 V V_{OOP} = GND to 6 V
Output current	ΦR, LD	I_{OH}	–1.0	–	–	mA	V_{CC} = 3 V
	ΦR, ΦP, LD	I_{OL}	–	–	1.0	mA	V_{CC} = 3 V
	D_O	I_{DOH}	–15	–	–5	mA	V_{CC} = 3 V, Vp = 5.0 V, V_{DOH} = 4.0 V
		I_{DOL}	6	–	18	mA	V_{CC} = 3 V, Vp = 5.0 V, V_{DOL} = 1.0 V

■ FUNCTION DESCRIPTIONS

Pulse Swallow Function

The devide ratio can be calculated using the following equation:

$f_{VCO} = [(P \times N) + A] \times f_{OSC} + R \quad (A < N)$

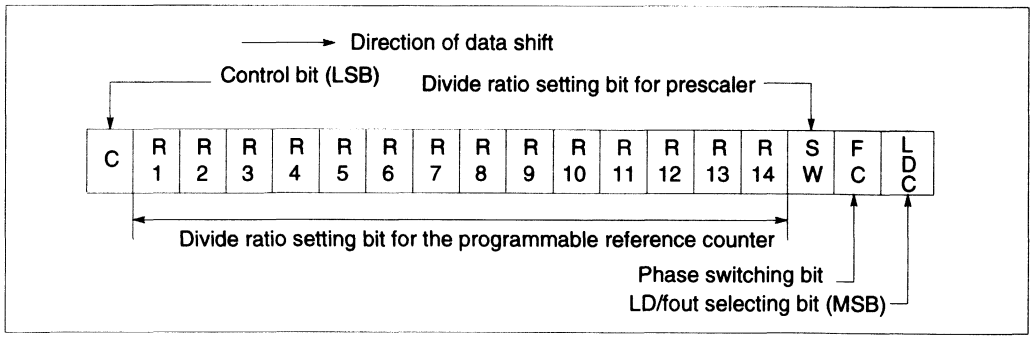
- f_{VCO} : Output frequency of external voltage controlled oscillator (VCO)
- N : Preset divide ratio of binary 11-bit programmable counter (5 to 2,047)
- A : Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$)
- f_{OSC} : Output frequency of the reference frequency oscillator
- R : Preset divide ratio of binary 14-bit programmable reference counter (6 to 16,383)
- P : Preset divide ratio of modules prescaler (64 or 128)

Serial Data Input

Serial data is processed using the Data, Clock, and LE pins. Serial data controls the 17-bit programmable reference divider and 18-bit programmable divider separately.
Binary serial data is entered via the Data pin.
One bit of data is shifted into the internal shift register on the rising edge of the clock. When the load enable pin is high or open, stored data is latched depending on the control data as follows:

Control data	Destination of serial data
H	17 bit latch
L	18 bit latch

(a) Programmable reference divider
The programmable reference divider consists of a 17-bit latch and a 14-bit reference counter. The serial 18-bit data format is shown below:



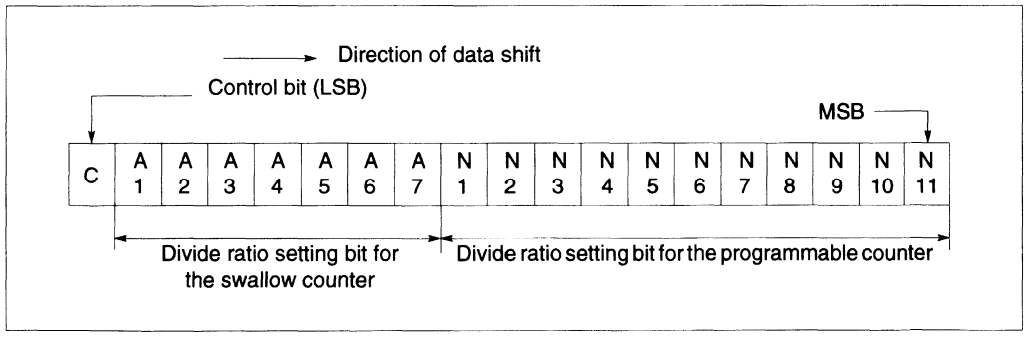
- 14-bit programmable reference counter divide ratio

Divide ratio (R)	R 14	R 13	R 12	R 11	R 10	R 9	R 8	R 7	R 6	R 5	R 4	R 3	R 2	R 1
6	0	0	0	0	0	0	0	0	0	0	0	1	1	0
7	0	0	0	0	0	0	0	0	0	0	0	1	1	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

(Divide ratio = 6 to 16,383)

Notes: 1. Divide ratios less than 6 are prohibited.
2. SW : This bit selects the divide ratio of the prescaler.
Low : 128 or 129
High: 64 or 65
3. LDS : This bit selects LD/fout pin output
High: outputs phase comparator monitoring signal(fout).
Low : outputs lock detecting signal(LD)
4. FC : This bit selects phase characteristics.
5. S1 to S14 : These bits select the divide ratio of the programmable reference counter (6 to 16,383).
6. C : Control bit: Set high.
7. Start data input with MSB first.

(b) Programmable divider
The programmable divider consists of a 19-bit shift register, a 18-bit latch, a 7-bit swallow counter, and a 11-bit programmable counter. The serial 19-bit data format is shown below:



• 7-bit swallow counter divide ratio

Divide ratio (A)	A 7	A 6	A 5	A 4	A 3	A 2	A 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

(Divide ratio = 0 to 127)

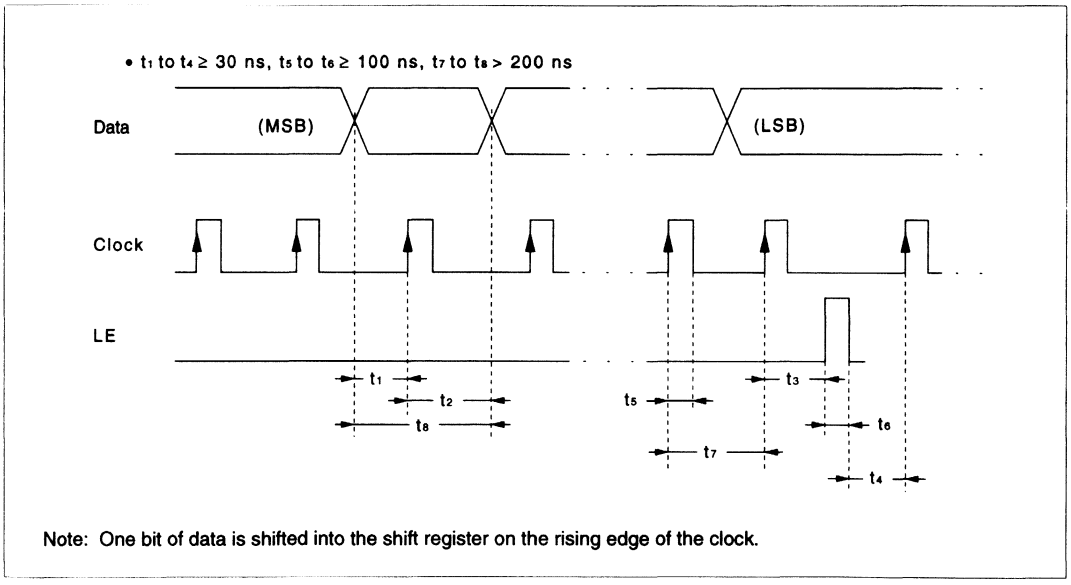
• 11-bit programmable counter divide ratio

Divide ratio (N)	N 11	N 10	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1
5	0	0	0	0	0	0	0	0	1	0	1
6	0	0	0	0	0	0	0	0	1	1	0
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

(Divide ratio = 5 to 2,047)

Notes: 1. Divide ratios less than 5 are prohibited for 11-bit programmable counter.
2. A1 to A7 : These bits select the divide ratio of swallow counter (0 to 127).
3. N1 to N11 : These bits select the divide ratio of programmable counter (5 to 2,047).
4. C : Control bit: (Set low)
5. Start data input with MSB first.

Serial Data Input Timing



Note: One bit of data is shifted into the shift register on the rising edge of the clock.

Power Saving Mode (Intermittent operation control circuit)

PS	State
H	Normal operation
L	Power saving mode

Setting PS pin to Low, MB15A17 enters into power saving mode resultantly current consumption can be limited to 100 μA (typ.). Setting PS pin to High, power saving mode is released so that the device works normally.
In addition, the intermittent operation control circuit is included which helps smooth start up from stand by mode. The power consumption can be reduced by the intermittent operation that powering down or waking up parts of the PLL circuitry. If a PLL is powered up uncontrolled, the resulting phase comparator output signal is unpredictable due to an undefined phase relation between reference frequency (f_r) and comparison frequency (f_p) and may in the worst case take longer time for lock up of the loop.
To prevent this, the intermittent operation control circuit enforces a limited error signal output of the phase detector during power up, thus keeping the loop locked.

Note: PS pin must be set "L" at Power-ON

Relation Between the FC Input and Phase Characteristics

The FC bit changes the phase characteristics of the phase comparator. Both the internal charge pump output level (Do) and the phase comparator output (ΦR, ΦP) are reversed according to the FC bit. Also, the monitor pin (f_{OUT}) output is controlled by the FC bit. The relationship between the FC bit and each of Do, ΦR, ΦP, and f_{OUT} is shown below.

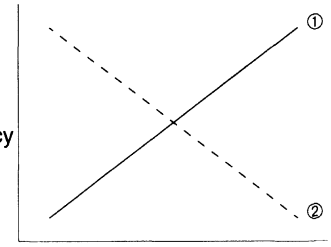
	FC = High				FC = Low			
	Do	ΦR	ΦP	fout	Do	ΦR	ΦP	fout
$f_r > f_p$	H	L	L	fr	L	H	Z(*1)	fp
$f_r < f_p$	L	H	Z(*1)	fr	H	L	L	fp
$f_r = f_p$	Z(*1)	L	Z(*1)	fr	Z(*1)	L	Z(*1)	fp

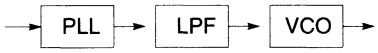
*1: High impedance

When designing a synthesizer, the FC pin setting depends on the VCO and LPF characteristics.

* : When the LPF and VCO characteristics are similar to ①, set FC bit high.

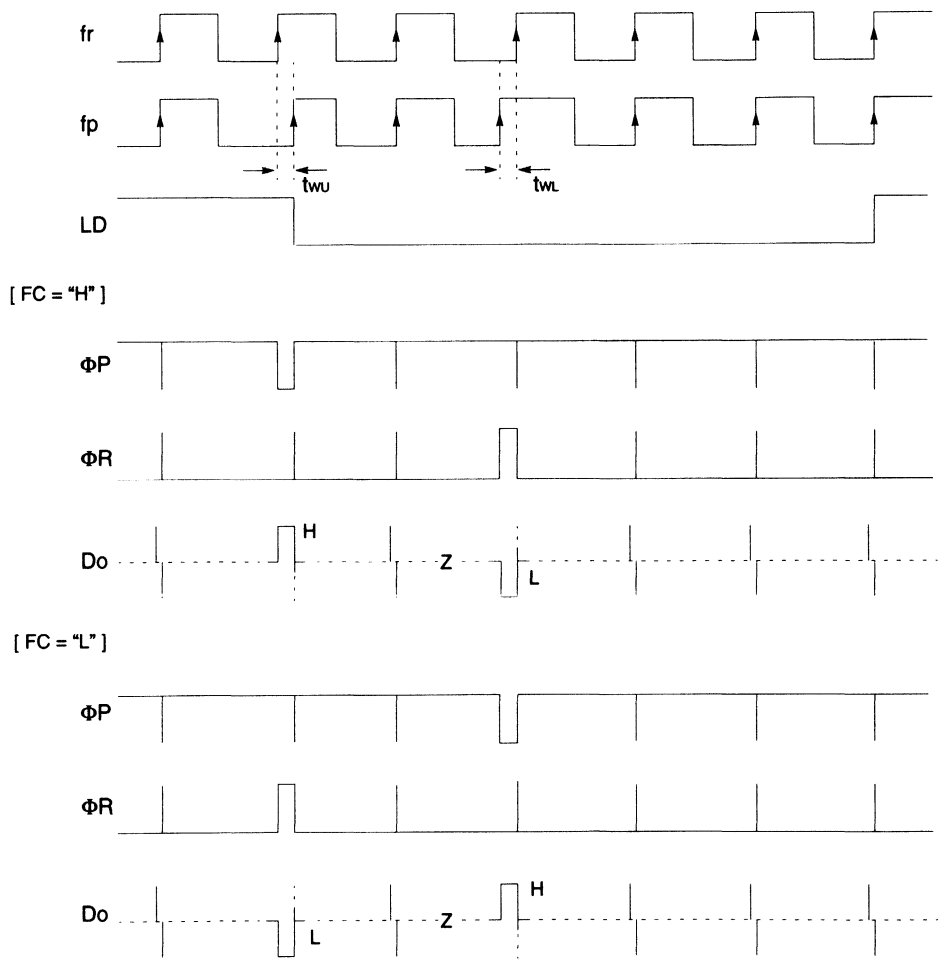
* : When the VCO characteristics are similar to ②, set FC low.





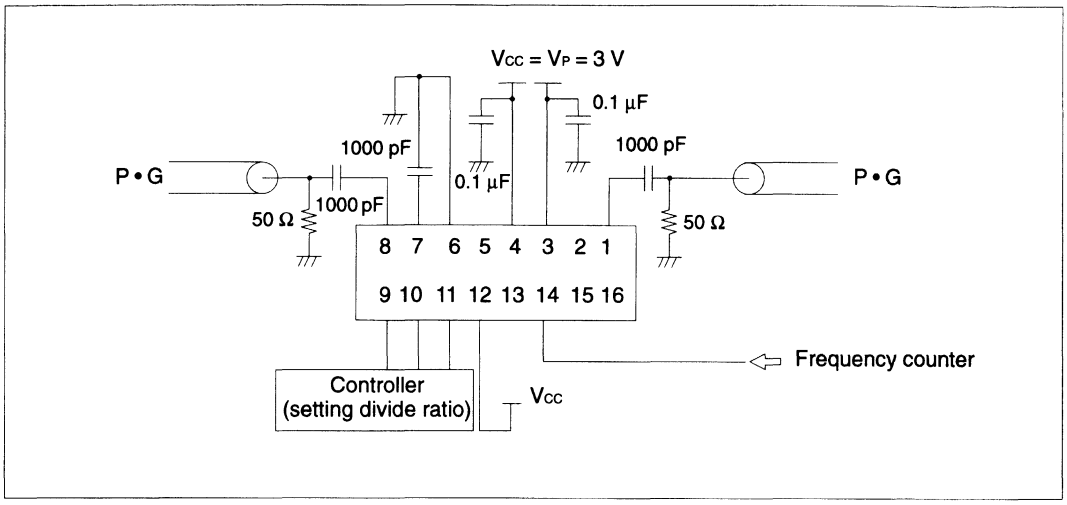
Note: When an active low pass filter is used, please be careful of the characteristics.

Phase Comparator Output Waveforms



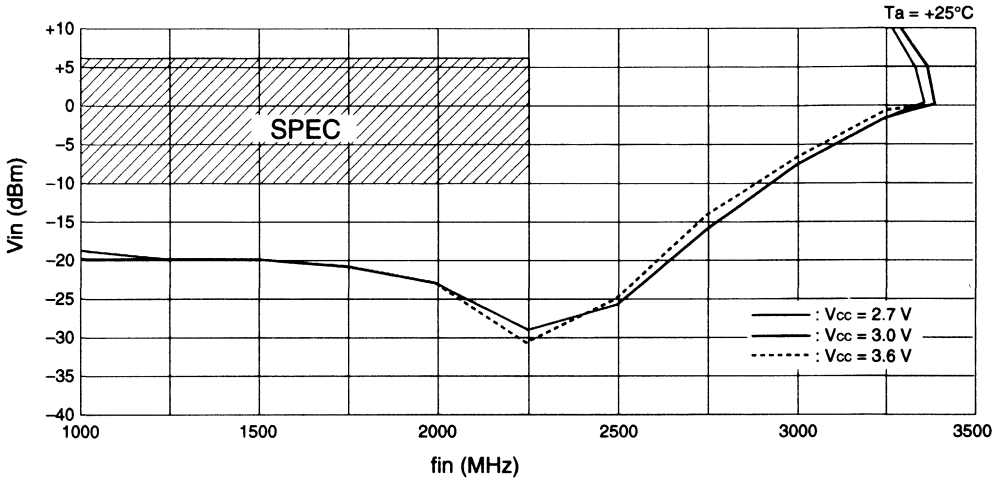
Notes: 1. Phase difference detection range: -2π to $+2\pi$
2. LD output becomes low when phase is twu or more. LD output becomes high when phase error is twL or less and continues to be so for three cycles or more.
3. twu and twL depend on OSCin input frequency.
twu ≥ 8/fosc (e. g. twu ≥ 625 ns, foscin = 12.8 MHz)
twL ≤ 16/fosc (e. g. twL ≤ 1250 ns, foscin = 12.8 MHz)

■ TEST CIRCUIT (for Measuring Input Sensitivity fin/OSCin)

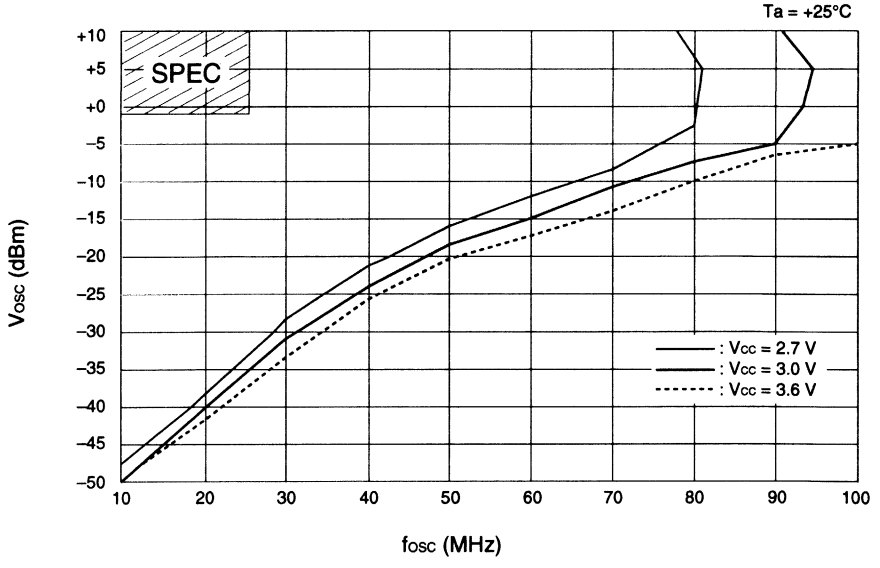


■ TYPICAL CHARACTERISTICS

Input Sensitivity (fin Pin)



Input Sensitivity (OSCin Pin)



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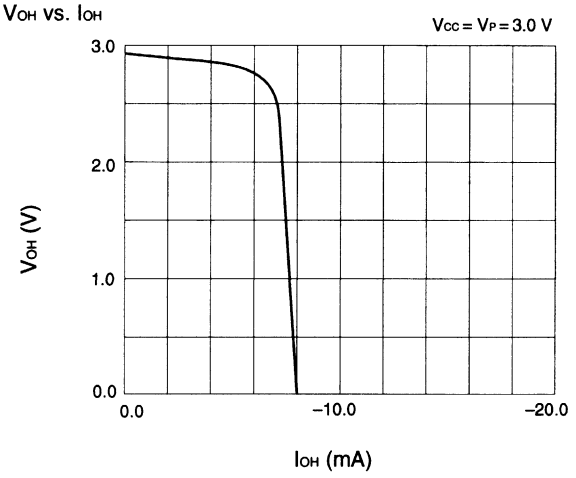
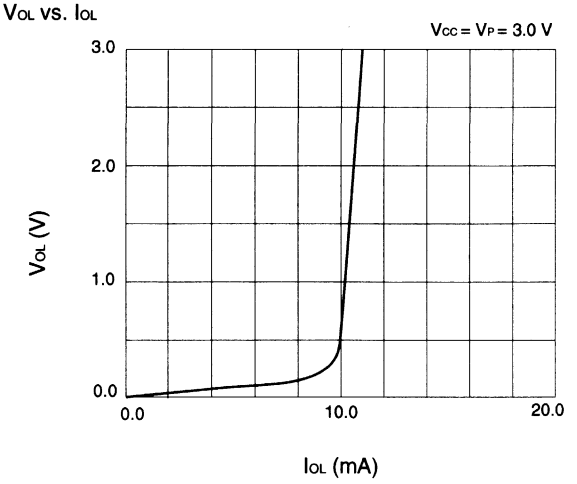
Charge Pump Current vs. Voltage (Do Pin)

V_{OH} vs. I_{OH}



V_{OL} vs. I_{OL}



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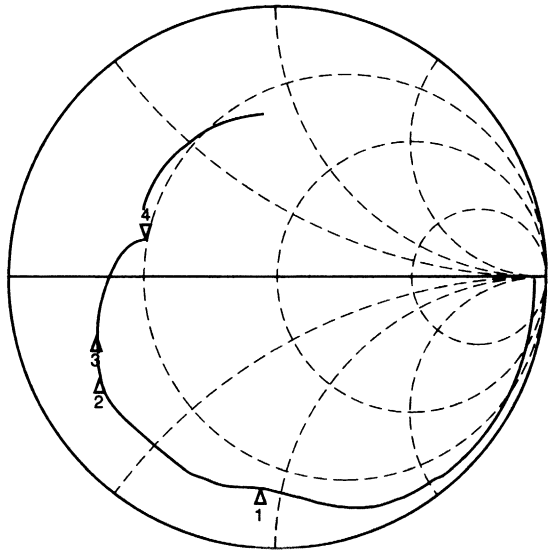
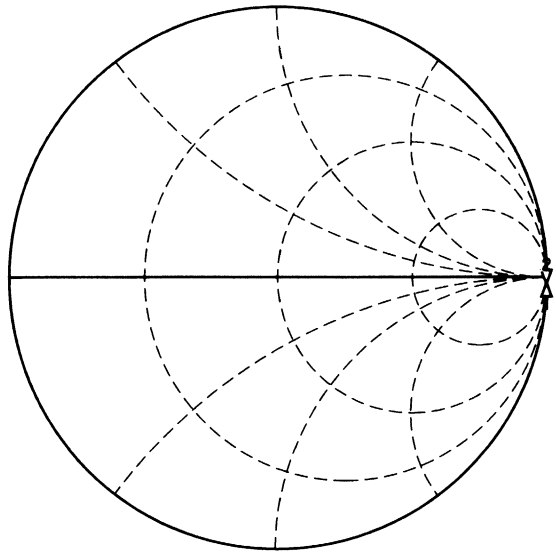
Input Impedance

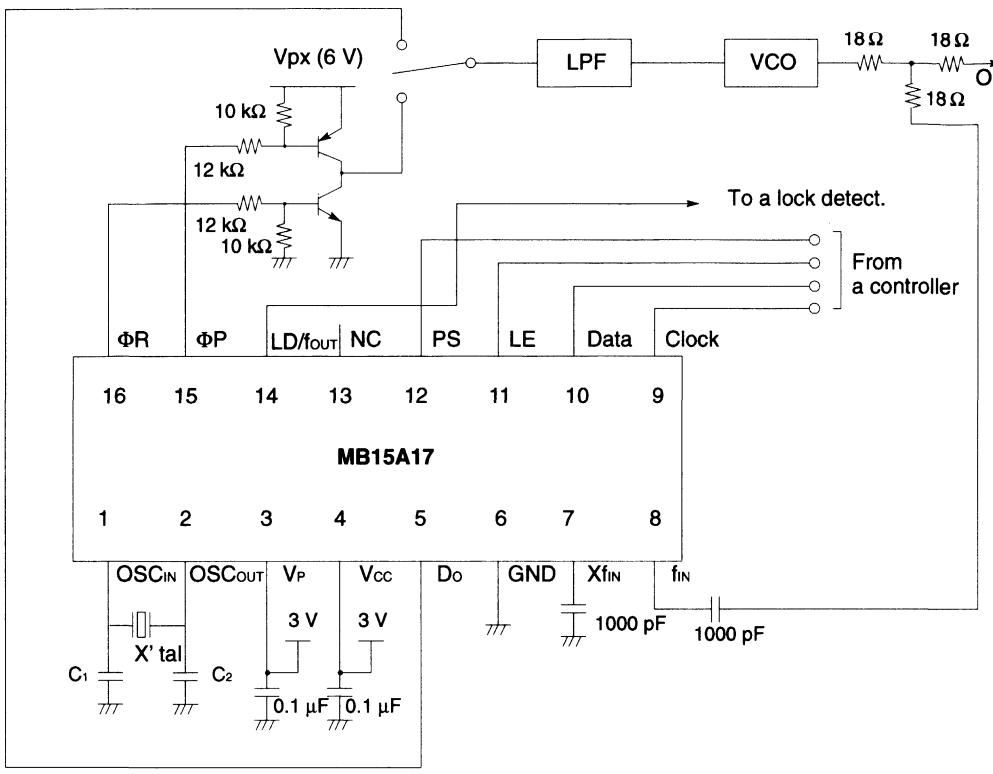
fin Pin



OSCin Pin



■ APPLICATION EXAMPLE

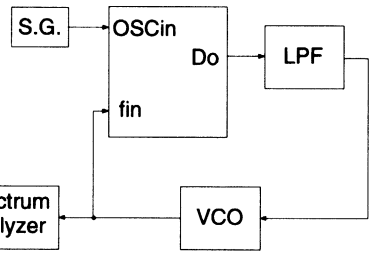


V_P	:	Maximum 5.0 V
C_1, C_2	:	Depend on the crystal parameters
ΦP	:	N-ch open drain output
ΦR	:	C-MOS output
Clock Data, LE, PS	:	When the pin is left opened, a pull down resistor must be connected.

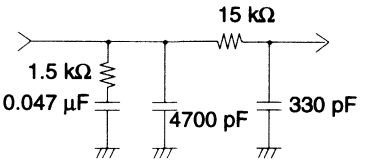
■ REFERENCE INFORMATION

Typical plots measured with the test circuit are shown below. Each plots shows lock up time, phase noise, and reference leakage.

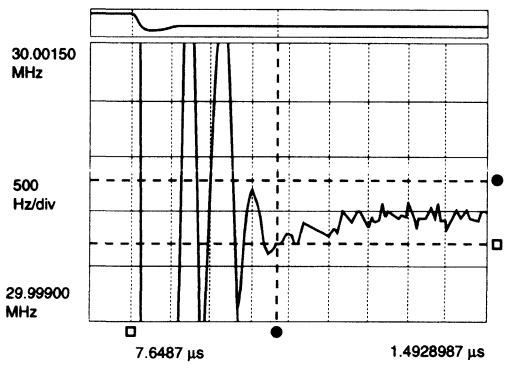
Test Circuit



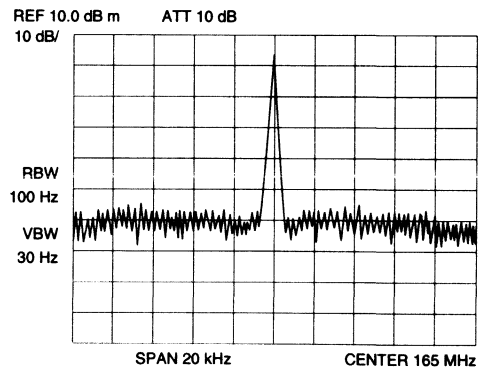
- V_{CC} = Vp = 3 V
- f_{VCO} = 1651.2 MHz
- K_V = 10 MHz/V
- f_r = 300 kHz
- f_{OSC} = 19.2 MHz
- LPF



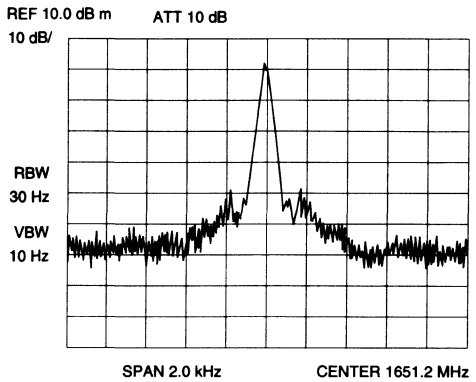
PLL Lock Up Time = 525 µs
(1651.2 MHz → 1674.0 MHz, within ± 300 Hz)



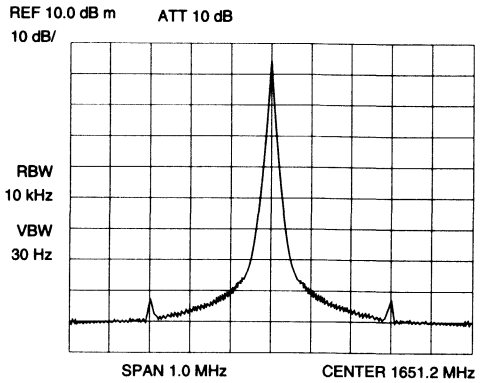
PLL Phase Noise
@10 kHz offset = 75 dBc/Hz



PLL Phase noise
@1 kHz offset = 77 dBc/Hz



PLL Reference Leakage
@300 kHz offset = 75dBc



■ ORDERING INFORMATION

Part number	Package	Remarks
MB15A17 PFV	16-pin Plastic SSOP (FPT-16P-M05)	

FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-21330-1E

ASSP
Single Serial Input PLL Frequency Synthesizer
On-Chip 2.0GHz Prescaler

MB15E05

■ DESCRIPTION

The Fujitsu MB15E05 is serial input Phase Locked Loop (PLL) frequency synthesizers with a 2.0 GHz prescaler. A 64/65 or a 128/129 can be selected for the prescaler that enables pulse swallow operation.

The latest BiCMOS process technology is used, resultantly a supply current is limited as low as 6mA typ. This operates with a supply voltage of 3.0V (typ.).

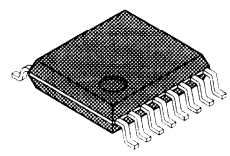
Furthermore, a super charger circuit is included to get a fast tuning as well as low noise performance. As a result of this, MB15E05 is ideally suitable for digital mobile communications, such as PCN (Personal Communication Network), PCS (Personal Communication Service), etc.

■ FEATURES

- High frequency operation: 2.0 GHz max
- Low power supply voltage: V_{CC} = 2.7 to 3.6V
- Very Low power supply current : I_{CC} = 6.0 mA typ. (V_{CC} = 3V)
- Power saving function : I_{PS} = 10 µA max.
- Pulse swallow function: 64/65 or 128/129
- Serial input 14-bit programmable reference divider: R = 5 to 16,383
- Serial input 18-bit programmable divider consisting of:
  - Binary 7-bit swallow counter: 0 to 127
  - Binary 11-bit programmable counter: 5 to 2,047
- Wide operating temperature: Ta = −40 to 85°C
- Plastic 16-pin SSOP package (FPT-16P-M05)

■ PACKAGE

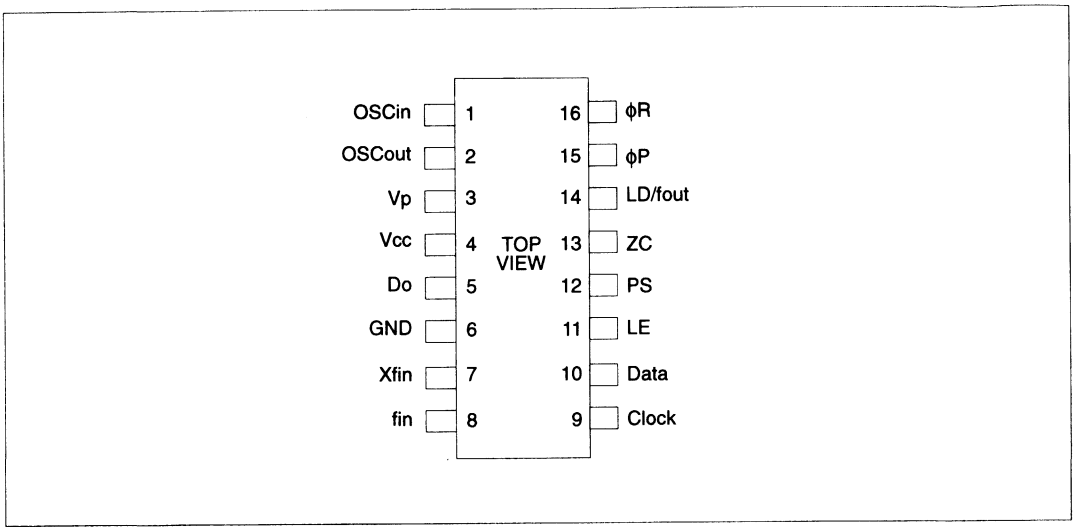
16-pin, Plastic SSOP



(FPT-16P-M05)

This device contains circuitry to protect the inputs against damage due to high static voltages or electroc fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

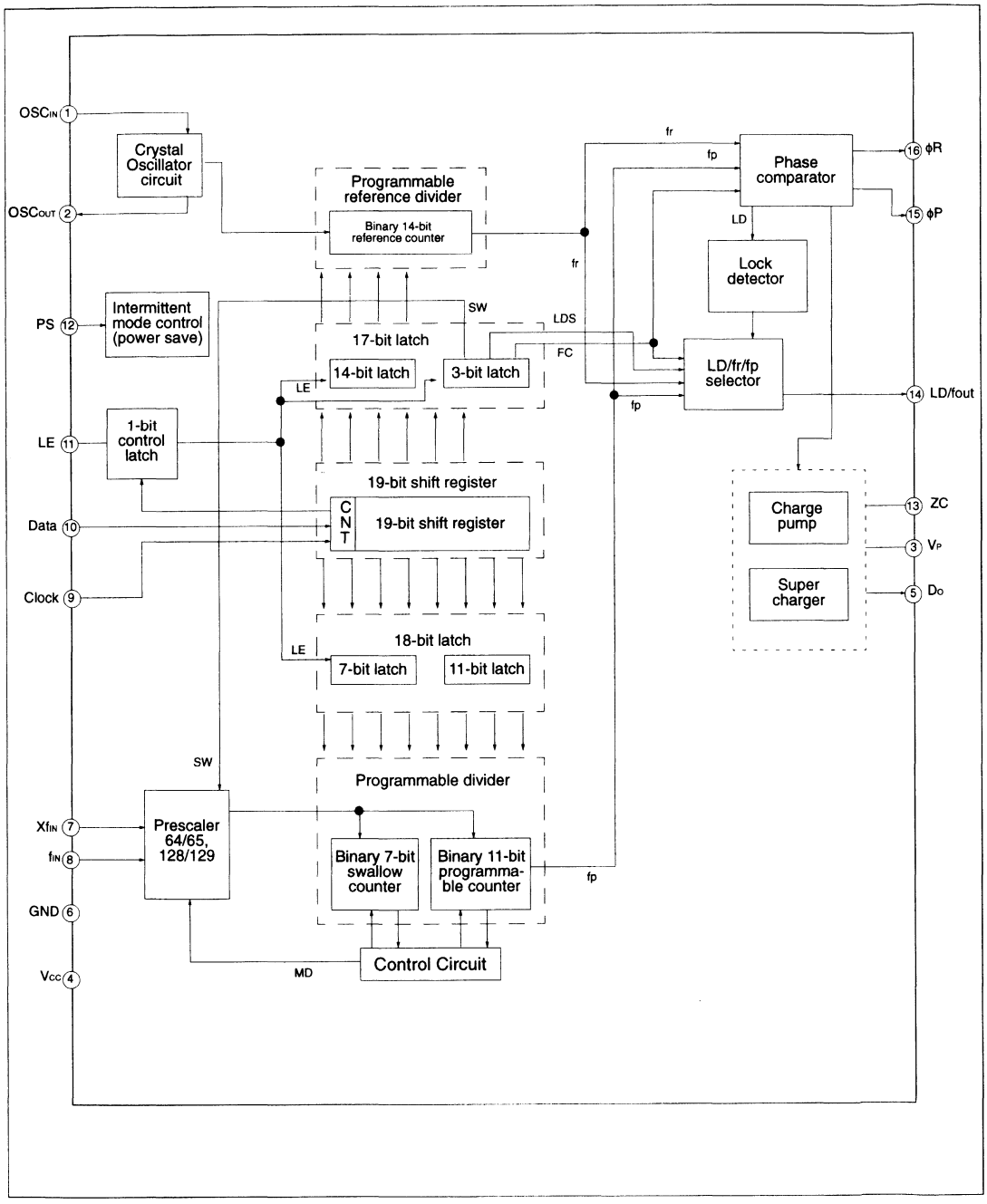
■ PIN ASSIGNMENT



■ PIN DESCRIPTIONS

Pin No.	Pin Name	I/O	Descriptions
1	OSC_{IN}	I	Programmable reference divider input. Oscillator input. Connection for an crystal or a TCXO. TCXO should be connected with a coupling capacitor.
2	OSC_{OUT}	O	Oscillator output. Connection for an external crystal.
3	V_P	–	Power supply voltage input for the charge pump.
4	V_{CC}	–	Power supply voltage input.
5	D_O	O	Charge pump output. Phase of the charge pump can be reversed by FC input.
6	GND	–	Ground.
7	Xfin	I	Prescaler complementary input, and should be grounded via a capacitor.
8	fin	I	Prescaler input. Connection with an external VCO should be done with AC coupling.
9	Clock	I	Clock input for the 19-bit shift register. Data is shifted into the shift register on the rising edge of the clock. *(Open is prohibited.)*
10	Data	I	Serial data input using binary code. The last bit of the data is a control bit. *(Open is prohibited.)* Control bit = "H" ; Data is transmitted to the programmable reference counter. Control bit = "L" ; Data is transmitted to the programmable counter.
11	LE	I	Load enable signal input *(Open is prohibited.)* When LE is high, the data in the shift register is transferred to a latch, according to the control bit in the serial data.
12	PS	I	Power saving control input. This pin should be set at "L" at Power-ON. *(Open is prohibited.)* PS = "H" ; Normal mode PS = "L" ; Power saving mode
13	ZC	I	Forced high-impedance control for the charge pump (with internal pull up resistor.) ZC = "H" ; Normal Do output. ZC = "L" ; Do becomes high impedance.
14	LD/fout	O	Lock detect signal output(LD)/ phase comparator monitoring output (fout). The output signal is selected by LDS bit in the serial data. LDS = "H" ; outputs fout (fr/fp monitoring output) LDS = "L" ; outputs LD ("H" at locking, "L" at unlocking.)
15	ϕP	O	Phase comparator output for an external charge pump.
16	ϕR	O	Phase comparator output for an external charge pump.

■ BLOCK DIAGRAM 1



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Remark
Power supply voltage	V_{CC}	−0.5 to +4.0	V	
	V_P	V_{CC} to +6.0	V	
Input voltage	V_I	−0.5 to V_{CC} +0.5	V	
Output voltage	V_O	−0.5 to V_{CC} +0.5	V	
Storage temperature	T_{stg}	−55 to +125	°C	

Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Remark
		Min	Typ	Max		
Power supply voltage	V_{CC}	2.7	3.0	3.6	V	
	V_P	V_{CC}	–	6.0	V	
Input voltage	V_I	GND	–	V_{CC}	V	
Operating temperature	Ta	−40	–	+85	°C	

Notes: To protect against damage by electrostatic discharge, note the following handling precautions:
-Store and transport devices in conductive containers.
-Use properly grounded workstations, tools, and equipment.
-Turn off power before inserting or removing this device into or from a socket.
-Protect leads with conductive sheet, when transporting a board mounted device.

■ ELECTRICAL CHARACTERISTICS

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Power supply current*1		I_{CC}	fin_{IF} = 2000MHz, fosc = 12MHz	–	6.0	–	mA
Power saving current*2		Ips	Vcc current at PS ="L" and ZC = "H"	–	–	10	µA
Operating frequency		fin		100	–	2000	MHz
Crystal oscillator operating frequency		fosc	min. 500mVp-p	3	–	40	MHz
Input sensitivity	fin	$Vfin_{IF}$	50Ω termination (Refer to the test circuit.)	–10	–	+2	dBm
	OSCin	V_{OSC}		500	–	V_{CC}	mVp–p
Input voltage	Data, Clock, LE, PS, ZC	V_{IH}		Vccx0.7	–	–	V
		V_{IL}		–	–	Vccx0.3	
Input current	Data, Clock, LE, PS	I_{IH}		–1.0	–	+1.0	µA
		I_{IL}		–1.0	–	+1.0	
	ZC	I_{IH}		–1.0	–	+1.0	µA
		I_{IL}	Pull up input	–100	–	0	
	OSCin	I_{IH}		0	–	+100	µA
		I_{IL}		–100	–	0	
Output voltage	φP	V_{OL}	Open drain output	–	–	0.4	V
	φR, LD/fout	V_{OH}		Vcc-0.4	–	–	V
		V_{OL}		–	–	0.4	
	Do	V_{DOH}		Vcc-0.4	–	–	V
		V_{DOL}		–	–	0.4	
High impedance cutoff current	Do	I_{OFF}		–	–	1.1	µA
Output current	φP	I_{OL}	Open drain output	1.0	–	–	mA
	φR, LD/fou	I_{OH}		–	–	–1.0	mA
		I_{OL}		1.0	–	–	
	Do	I_{DOH}	Vcc = 3.0V, Vp = 5V, V_{DOH} = 4.0V	–	–10.0*2	–	mA
		I_{DOL}	Vcc = 3.0V, Vp = 5V, V_{DOL} = 1.0V	–	10.0*2	–	

*1: Conditions ; Vcc = 3.0V, Ta = 25°C, in locking state.

*2: Conditions ; Ta = 25°C

■ FUNCTION DESCRIPTIONS

Pulse Swallow Function

The divide ratio can be calculated using the following equation:

$f_{VCO} = [(M \times N) + A] \times f_{OSC} \div R \quad (A < N)$

- f_{VCO} : Output frequency of external voltage controlled oscillator (VCO)
- N : Preset divide ratio of binary 11-bit programmable counter (5 to 2,047)
- A : Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$)
- f_{OSC} : Output frequency of the reference frequency oscillator
- R : Preset divide ratio of binary 14-bit programmable reference counter (5 to 16,383)
- M : Preset divide ratio of modules prescaler (64 or 128)

Serial Data Input

Serial data is processed using the Data, Clock, and LE pins. Serial data controls the programmable reference divider and the programmable divider separately.
Binary serial data is entered through the Data pin.
One bit of data is shifted into the shift register on the rising edge of the clock. When the load enable pin is high, stored data is latched according to the control bit data as follows:

Table.1 Control Bit

Control bit (CNT)	Destination of serial data
H	17 bit latch (for the programmable reference divider)
L	18 bit latch (for the programmable divider)

Shift Register Configuration

Programmable Reference Counter

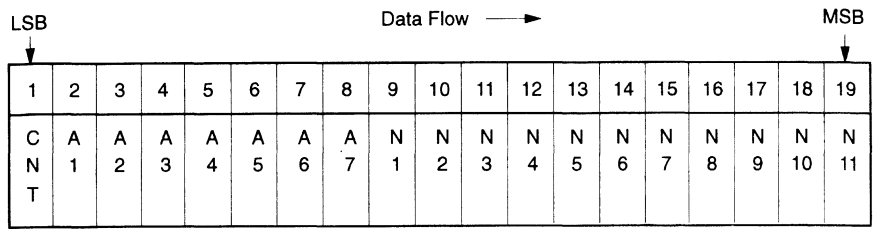
LSB ↓ Data Flow ⟶ MSB ↓

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
CNT	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	SW	FC	LDS

CNT : Control bit [Table. 1]
R1 to R14 : Divide ratio setting bit for the programmable reference counter (5 to 16,383) [Table. 2]
SW : Divide ratio setting bit for the prescaler (64/65 or 128/129) [Table. 5]
FC : Phase control bit for the phase comparator [Table. 7]
LDS : LD/fout signal select bit [Table. 6]

Note: Start data input with MSB first

Programmable Reference Counter



CNT : Control bit [Table. 1]
N1 to N11 : Divide ratio setting bits for the programmable counter (5 to 2,047) [Table. 3]
A1 to A7 : Divide ratio setting bits for the swallow counter (0 to 127) [Table. 4]

Note: Start data input with MSB first

Table2. Binary 14-bit Programmable Reference Counter Data Setting

Divide ratio (R)	R 14	R 13	R 12	R 11	R 10	R 9	R 8	R 7	R 6	R 5	R 4	R 3	R 2	R 1
5	0	0	0	0	0	0	0	0	0	0	0	1	0	1
6	0	0	0	0	0	0	0	0	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: • Divide ratio less than 5 is prohibited.

Table.3 Binary 11-bit Programmable Counter Data Setting

Divide ratio (N)	N 11	N 10	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1
5	0	0	0	0	0	0	0	0	1	0	1
6	0	0	0	0	0	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.	.	.	.
2047	1	1	1	1	1	1	1	1	1	1	1

Note: • Divide ratio less than 5 is prohibited.
• Divide ratio (N) range = 5 to 2,047

Table.4 Binary 7-bit Swallow Counter Data Setting

Divide ratio (A)	A 7	A 6	A 5	A 4	A 3	A 2	A 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.
127	1	1	1	1	1	1	1

Note: • Divide ratio (A) range = 0 to 127

Table. 5 Prescaler Data Setting

SW	Prescaler Divide ratio
H	64/65
L	128/129

Table. 6 LD/fout Output Select Data Setting

LDS	LD/fout output signal
H	fout signal
L	LD signal

Relation between the FC input and phase characteristics

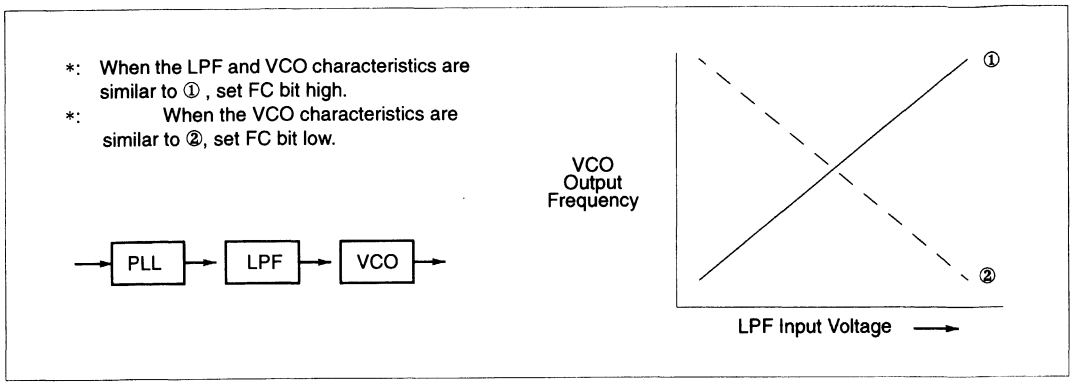
The FC bit changes the phase characteristics of the phase comparator. Both the internal charge pump output level (D_O) and the phase comparator output (ϕR, ϕP) are reversed according to the FC bit. Also, the monitor pin (f_{OUT}) output is controlled by the FC bit. The relationship between the FC bit and each of D_O, ϕR, and ϕP is shown below.

Table. 7 FC Bit Data Setting (LDS = "H")

	FC = High				FC = Low			
	Do	φR	φP	LD/fout	Do	φR	φP	LD/fout
$f_r > f_p$	H	L	L	(fr)	L	H	Z*	(fp)
$f_r < f_p$	L	H	Z*	(fr)	H	L	L	(fp)
$f_r = f_p$	Z*	L	Z*	(fr)	Z*	L	Z*	(fp)

* : High impedance

When designing a synthesizer, the FC pin setting depends on the VCO and LPF characteristics.



Power Saving Mode (Intermittent Mode Control Circuit)

Setting a PS pin to Low, the IC enters into power saving mode resultatly current sonsumption can be limited to 10μA (max.). Setting PS pin to High, power saving mode is released so that the IC works normally.
In addition, the intermittent operation control circuit is included which helps smooth start up from the power saving mode. In general, the power consumption can be saved by the intermittent operation that powering down or waking up the synthesizer. Such case, if the PLL is powered up uncontrolled, the resulting phase comparator output signal is unpredictable due to an undefined phase relation between reference frequency (f_r) and comparison frequency (f_p) and may in the worst case take longer time for lock up of the loop.
To prevent this, the intermittent operation control circuit enforces a limited error signal output of the phase detector during power up, thus keeping the loop locked.
During the power saving mode, the corresponding section except for indispensable circuit for the power saving function stops working, then current consumption is reduced to 10μA per one PLL section.
At that time, the Do and LD become the same state as when a loop is locking. That is, the Do becomes high impedance.
A VCO control voltage is naturally kept at the locking voltage which defined by a LPF"s time constant. As a result of this, VCO's frequency is kept at the locking frequency.

Note: • *While the power saving mode is executed, ZC pin should be set at "H" or open. If ZC is set at "L" during power saving mode, approximately 10 μA current flows.*
- *PS pin must be set "L" at Power-ON.*
- *The power saving mode can be released (PS : L → H) 1μs later after power supply remains stable.*
- *During the power saving mode, it is possible to input the serial data.*

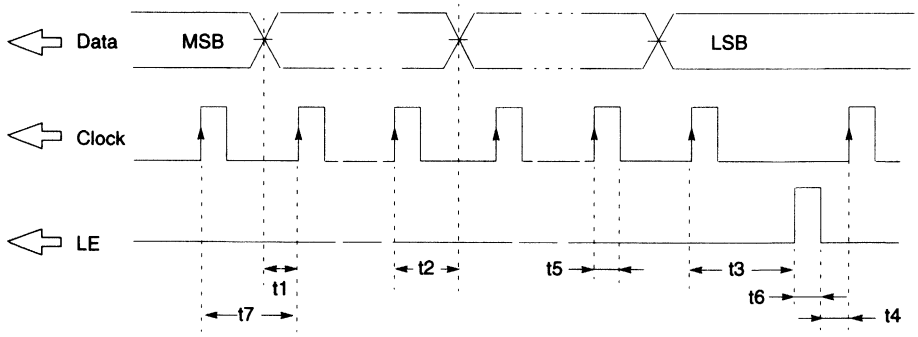
Table.8 PS Pin Setting

PS pin	Status
H	Normal mode
L	Power saving mode

Table.9 ZC Pin Setting

ZC pin	Do output
H	Normal output
L	High impedance

■ SERIAL DATA INPUT TIMING

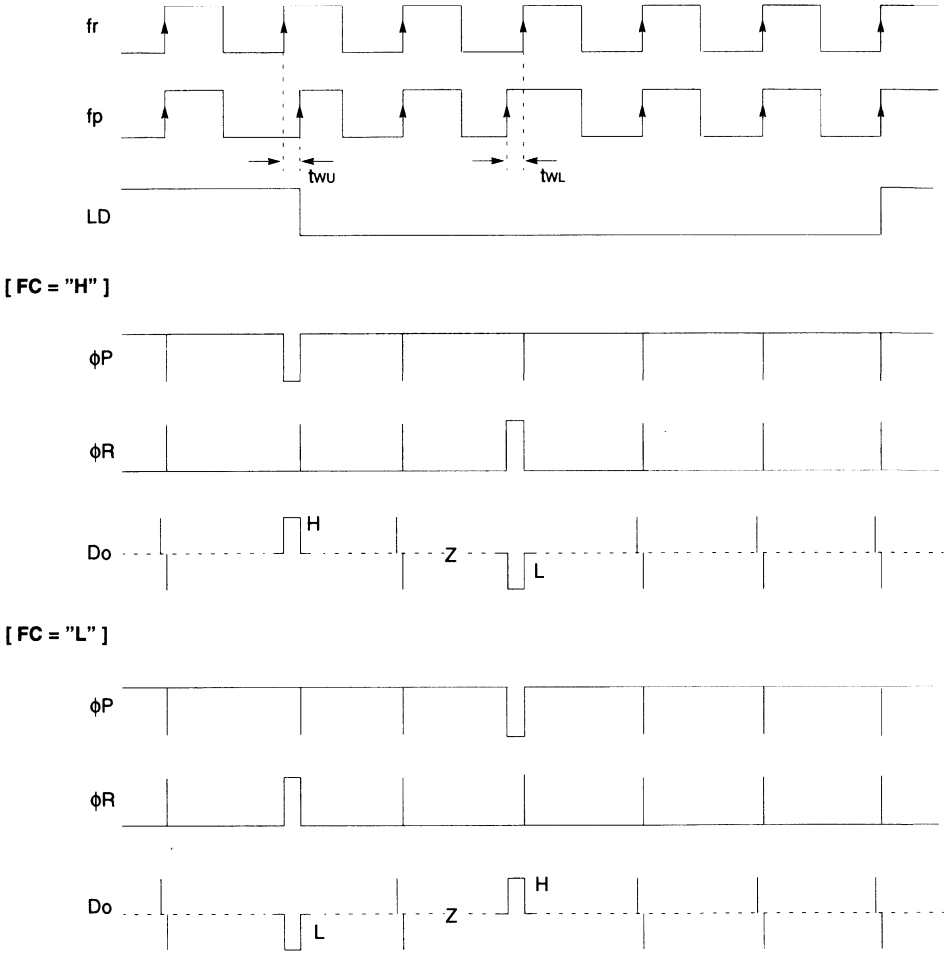


On rising edge of the clock, one bit of the data is transferred into the shift register.

Parameter	Min.	Typ.	Max.	Unit
t1	20	–	–	ns
t2	20	–	–	ns
t3	30	–	–	ns
t4	20	–	–	ns

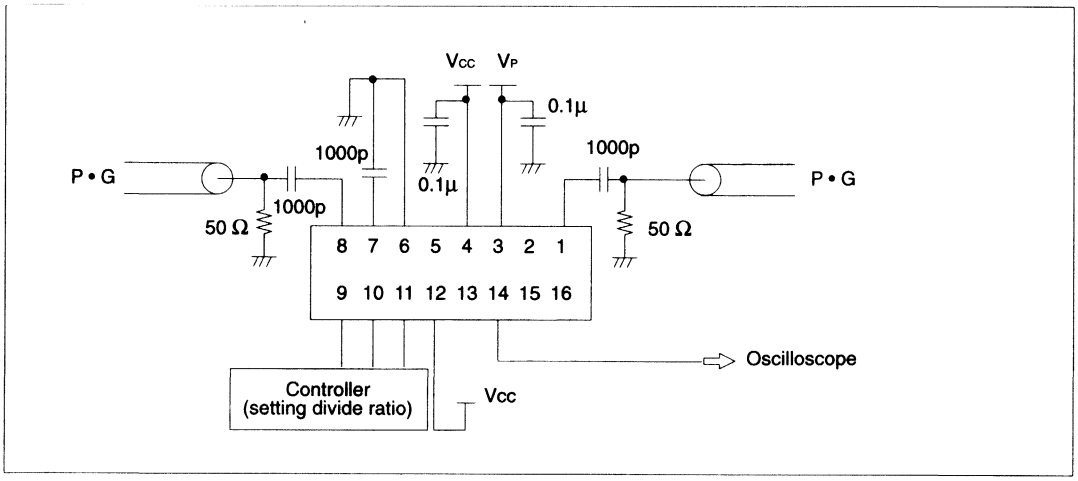
Parameter	Min.	Typ.	Max.	Unit
t5	30	–	–	ns
t6	100	–	–	ns
t7	100	–	–	ns

■ PHASE COMPARATOR OUTPUT WAVEFORM

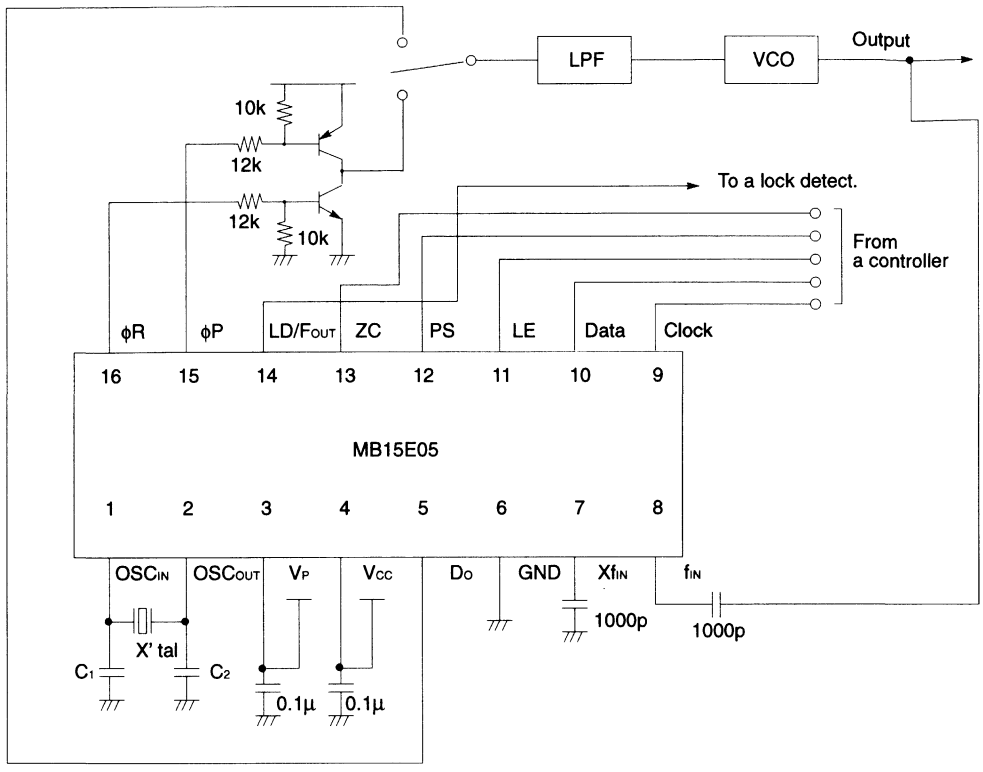


Notes:
1. Phase error detection range: -2π to $+2\pi$
2. Pulses on Do output signal during locked state are output to prevent dead zone.
3. LD output becomes low when phase is twu or more. LD output becomes high when phase error is twL or less and continues to be so for three cysles or more.
4. twu and twL depend on OSCin input frequency.
   twu ≥ 8/fosc (e. g. twu ≥ 625ns, foscin = 12.8 MHz)
   twL ≤ 16/fosc (e. g. twL ≤ 1250ns, foscin = 12.8 MHz)
5. LD becomes high during the power saving mode (PS = "L".)

■ TEST CIRCUIT (for Measuring Input Sensitivity fin/OSCin)



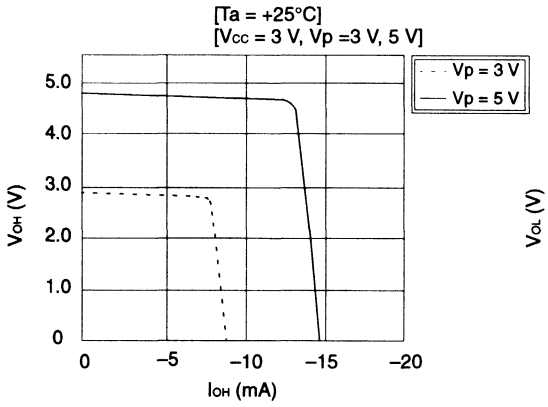
■ APPLICATION EXAMPLE

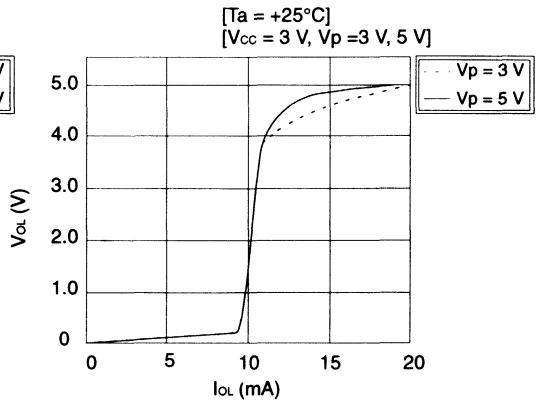


C_1, C_2 : Depend on the crystal parameters

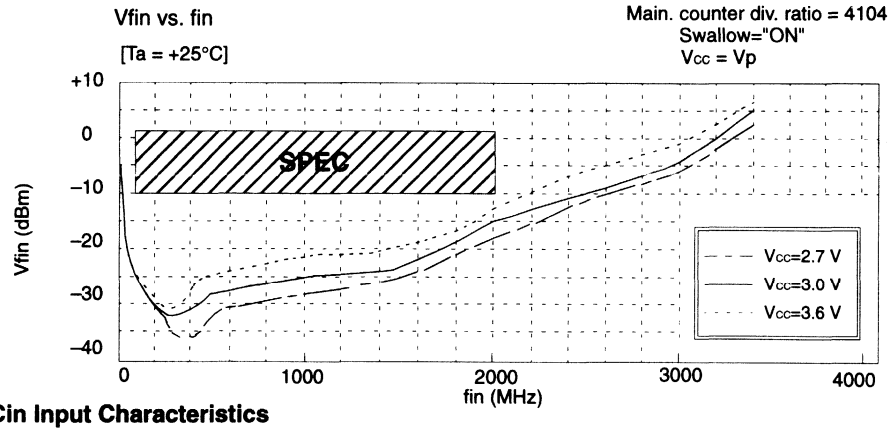
■ TYPICAL CHARACTERISTICS

Do Output Current

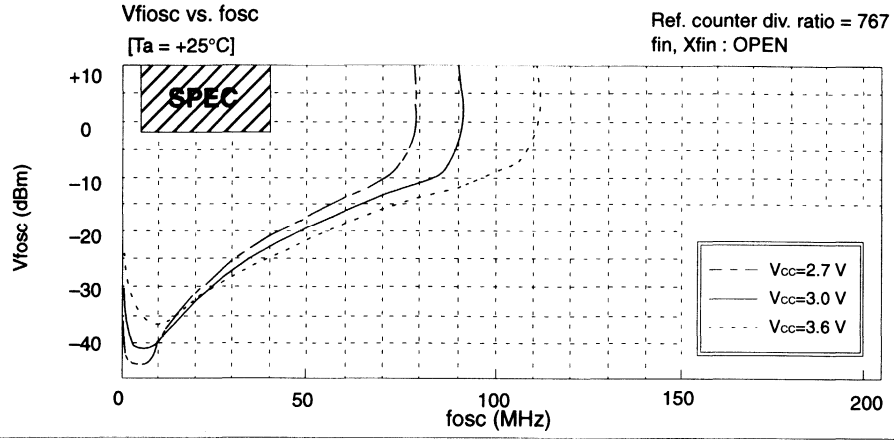




fin Input Sensitivity



OSCin Input Characteristics



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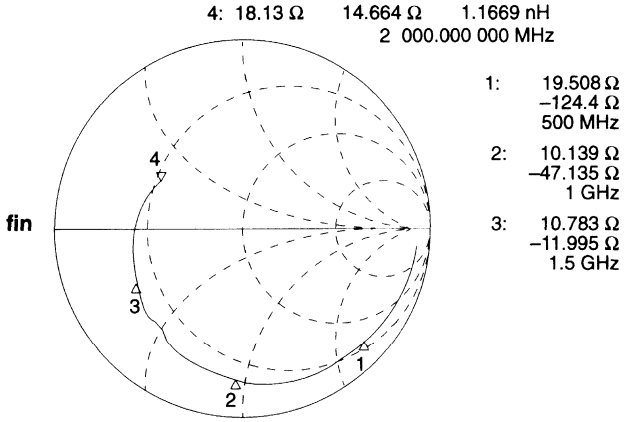
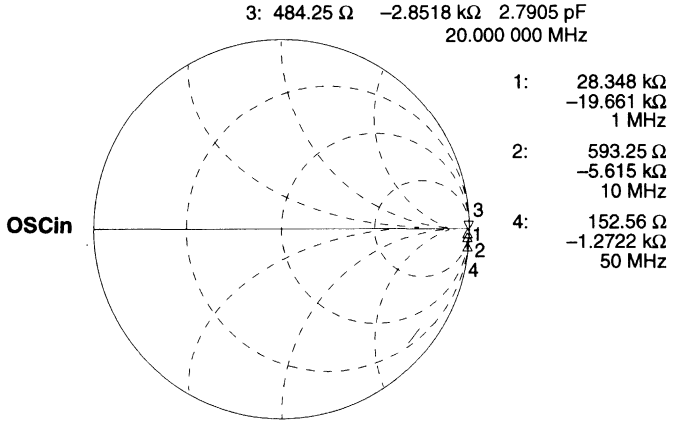
fin Input Impedance



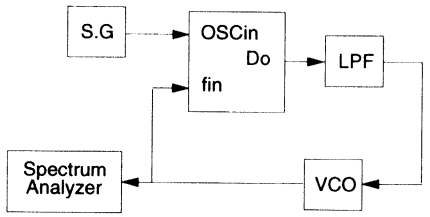
OSCin Input Impedance



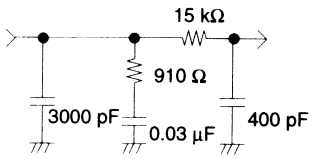
■ REFERENCE INFORMATION

Typical plots measured with the test circuit are shown below. Each plot shows lock up time, phase noise and reference leakage.

Test Circuit

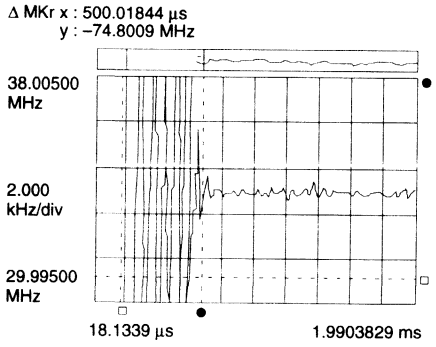


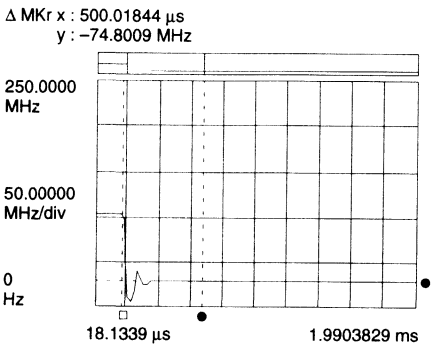
- fvco = 1835 MHz
- Kv = 87 MHz/v
- fr = 200 kHz
- fosc = 13 MHz
- LPF:



PLL Lock Up Time = 500 µs

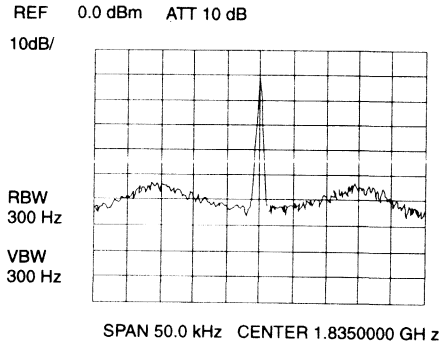
(1797.6 MHz → 1872.4 MHz, within ± 1kHz)





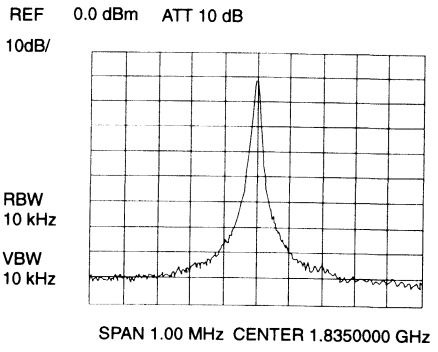
PLL Phase Noise

@ within loop band = 69.4 dBc/Hz



PLL Reference Leakage

@ 200 kHz offset = 74.6 dBc



■ ORDERING INFORMATION

Part number	Package	Remarks
MB15E05PFV1	16-pin Plastic SSOP (FPT-16P-M05)	

FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-21334-1E

ASSP

Dual Serial Input PLL Frequency Synthesizer

MB15F03

■ DESCRIPTION

The Fujitsu MB15F03 is a serial input Phase Locked Loop (PLL) frequency synthesizer with a 2.0GHz and a 500MHz prescalers. A 64/65 or a 128/129 for the 2.0GHz prescaler, and a 16/17 or a 32/33 for 500MHz prescaler can be selected that enables pulse swallow operation.

The latest BiCMOS process technology is used, resultantly a supply current is limited as low as 9.0mA typ. at a supply voltage of 3.0V.

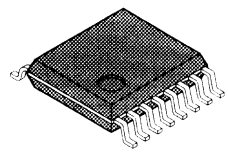
Furthermore, a super charger circuit is included to provide a fast tuning as well as low noise performance. As a result of this, MB15F03 is ideally suitable for digital mobile communications, such as PHS(Personal Handy Phone System), PCN (Personal Communication Network) and PCS(Personal Communication Service).

■ FEATURES

- High frequency operation RF synthesizer : 2.0GHz max.
  IF synthesizer : 500MHz max.
- Low power supply voltage: V_{CC} = 2.7 to 3.6V
- Very Low power supply current : I_{CC} = 9.0 mA typ. (V_{CC} = 3V)
- Power saving function : I_{PS1} = I_{PS2} = 10 µA max.
- Serial input 14–bit programmable reference divider: R = 5 to 16,383
- Serial input 18–bit programmable divider consisting of:
  - Binary 7–bit swallow counter: 0 to 127
  - Binary 11–bit programmable counter: 5 to 2,047
- On–chip high performance charge pump circuit and phase comparator, achieving high–speed lock–up and low phase noise
- Wide operating temperature: T_a = –40 to 85°C
- Plastic 16-pin SSOP package (FPT-16P-M05)

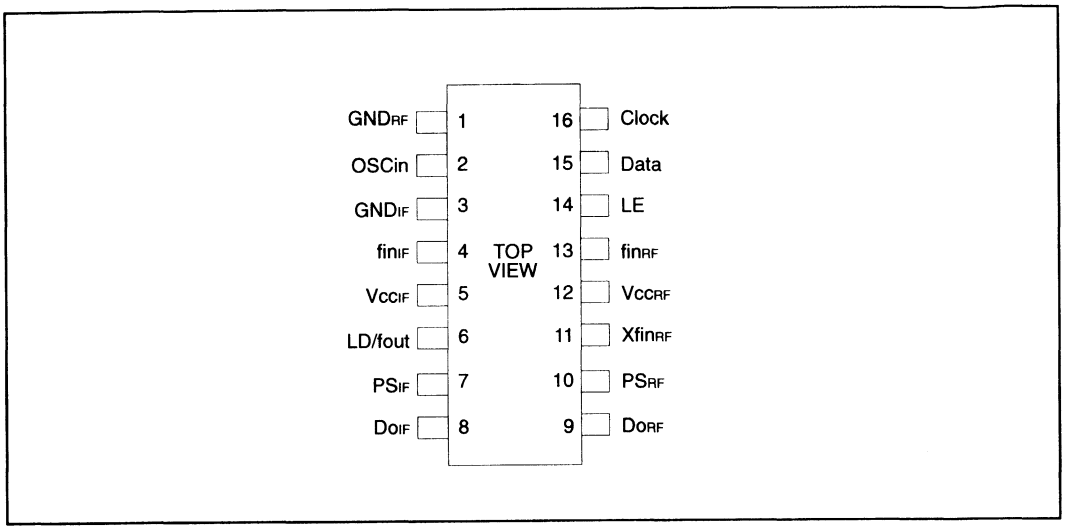
■ PACKAGE

16-pin, Plastic SSOP



(FPT-16P-M05)

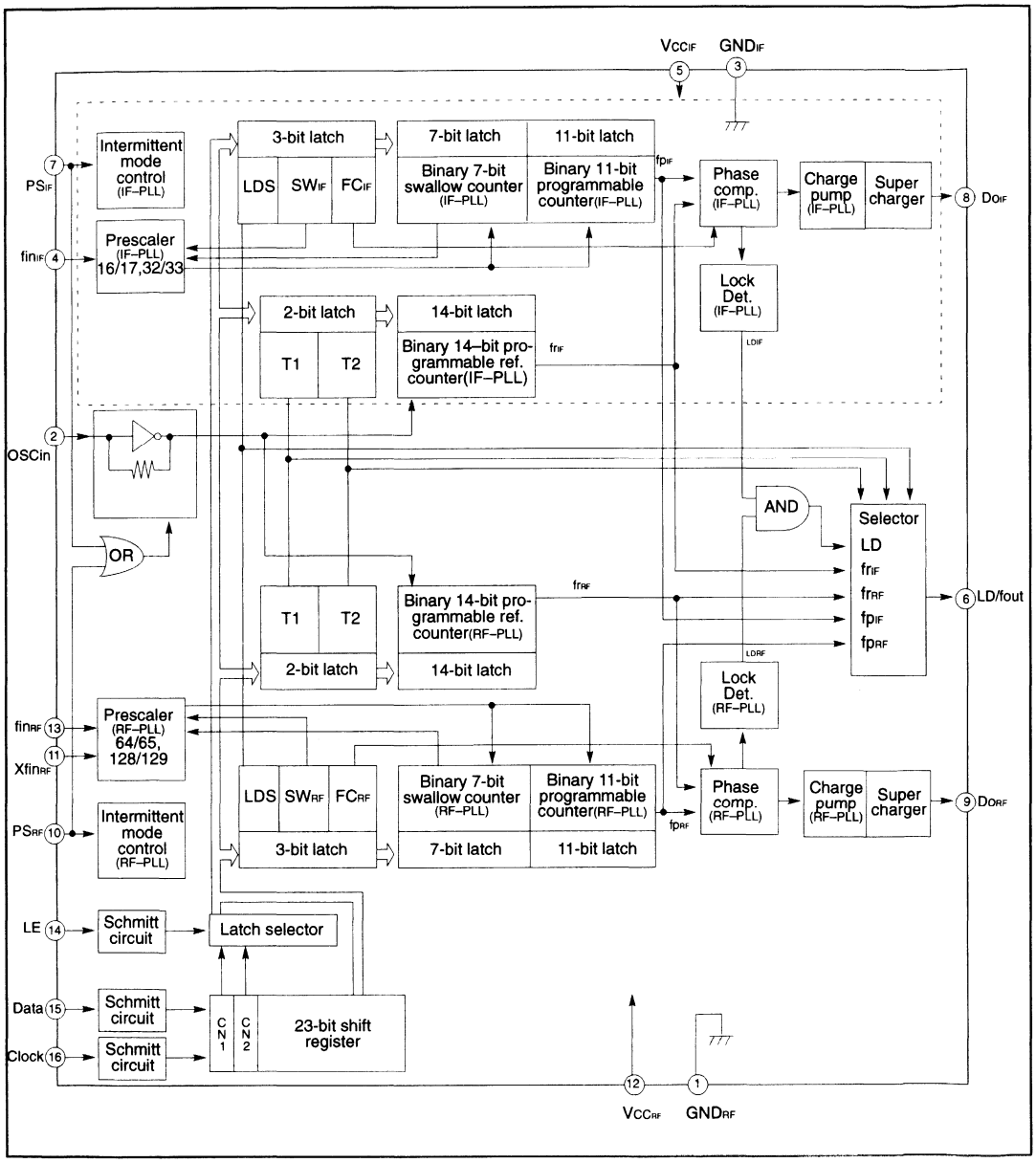
■ PIN ASSIGNMENT



■ PIN DESCRIPTIONS

Pin No.	Pin name	I/O	Descriptions
1	GND_{RF}	–	Ground for RF–PLL section.
2	OSCin	I	The programmable reference divider input. TCXO should be connected with a coupling capacitor.
3	GND_{IF}	–	Ground for the IF-PLL section.
4	fin_{IF}	I	Prescaler input pin for the IF-PLL. The connection with VCO should be AC coupling.
5	V_{CCIF}	–	Power supply voltage input pin for the IF-PLL section. When power is OFF, latched data of IF-PLL is cancelled.
6	LD/fout	O	Lock detect signal output (LD) / phase comparator monitoring output (fout) The output signal is selected by a LDS bit in a serial data. LDS bit = "H" ; outputs fout signal LDS bit = "L" ; outputs LD signal
7	PS_{IF}	I	Power saving mode control for the IF-PLL section. This pin must be set at "L" Power-ON. (Open is prohibited.) PS_{IF} = "H" ; Normal mode PS_{IF} = "L" ; Power saving mode
8	DO_{IF}	O	Charge pump output for the IF-PLL section. Phase characteristics of the phase detector can be reversed by FC-bit.
9	DO_{RF}	O	Charge pump output for the RF-PLL section. Phase characteristics of the phase detector can be reversed by FC-bit.
10	PS_{RF}	I	Power saving mode control for the RF-PLL section. This pin must be set at "L" Power-ON. (Open is prohibited.) PS_{RF} = "H" ; Normal mode PS_{RF} = "L" ; Power saving mode
11	$Xfin_{RF}$	I	Prescaler complimentary input for the RF-PLL section. This pin should be grounded via a capacitor.
12	V_{CCRF}	–	Power supply voltage input pin for the RF-PLL section, the shift register and the oscillator input buffer. When power is OFF, latched data of RF-PLL is cancelled.
13	fin_{RF}	I	Prescaler input pin for the RF-PLL. The connection with VCO should be AC coupling.
14	LE	I	Load enable signal input (with the schmitt trigger circuit.) When LE is "H", data in the shift register is transferred to the corresponding latch according to the control bit in a serial data.
15	Data	I	Serial data input (with the schmitt trigger circuit.) A data is transferred to the corresponding latch (IF-ref counter, IF-Prog. counter, RF-ref. counter, RF-prog. counter) according to the control bit in a serial data.
16	Clock	I	Clock input for the 23-bit shift register (with the schmitt trigger circuit.) One bit data is shifted into the shift register on a riging edge of the clock.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Remark
Power supply voltage	V_{CC}	−0.5 to +4.0	V	
Input voltage	V_I	−0.5 to V_{CC} +0.5	V	
Output voltage	V_O	−0.5 to V_{CC} +0.5	V	
Storage temperature	T_{STG}	−55 to +125	°C	

Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Note
		Min	Typ	Max		
Power supply voltage	V_{CC}	2.7	3.0	3.6	V	$V_{CCIF} = V_{CCRF}$
Input voltage	V_I	GND	–	V_{CC}	V	
Operating temperature	Ta	−40	–	+85	°C	

Handling Precautions

- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover workbenches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

■ ELECTRICAL CHARACTERISTICS

Parameter		Symbol	Condition	Value			Unit
				Min.	Typ.	Max.	
Power supply current*1		I_{CCIF}	f_{inIF} = 500MHz, fosc = 12MHz	–	3.0	–	mA
		I_{CCRF}	f_{inRF} = 2000MHz, fosc = 12MHz	–	6.0	–	
Power saving current		I_{psIF}	V_{CCIF} current at PS_{IF} ="L"	–	–	10	µA
		I_{psRF}	V_{CCRF} current at $PS_{IF/RF}$ ="L"	–	–	10	
Operating frequency	f_{inIF}	f_{inIF}	IF–PLL	50	–	500	MHz
	f_{inRF}	f_{inRF}	RF–PLL	100	–	2000	
	OSCin	f_{OSC}	min. 500mVp-p	3	–	40	
Input sensitivity	f_{inIF}	V_{finIF}	IF–PLL, 50Ω termination	–10	–	+2	dBm
	f_{inRF}	V_{finRF}	RF–PLL, 50Ω termination	–10	–	+2	dBm
	OSCin	V_{OSC}		500	–	V_{CC}	mVp-p
Input voltage	Data, Clock, LE	V_{IH}	Schmitt trigger input	V_{CC}x0.7+0.4	–		V
		V_{IL}	Schmitt trigger input	–	–	V_{CC}x0.3–0.4	
	PS_{IF}, PS_{RF}	V_{IH}		V_{CC}x0.7	–		V
		V_{IL}		–	–	V_{CC}x0.3	
Input current	Data, Clock, LE, PS_{IF}, PS_{RF}	I_{IH}		–1.0		+1.0	µA
		I_{IL}		–1.0	–	+1.0	
	OSCin	I_{IH}		0	–	+100	µA
		I_{IL}		–100	–	0	
Output voltage	LD/fout	V_{OH}		V_{CC}–0.4	–		V
		V_{OL}		–	–	0.4	
	DO_{IF}, DO_{RF}	V_{DOH}		V_{CC}–0.4	–		V
		V_{DOL}		–	–	0.4	
High impedance cutoff current	DO_{IF}, DO_{RF}	I_{OFF}		–	–	1.1	µA
Output current	LD/fout	I_{OH}	Vcc = 3.0V	–	–	–1.0	mA
		I_{OL}	Vcc = 3.0V	1.0	–	–	
	DO_{IF}, DO_{RF}	I_{DOH}	Vcc = 3.0V, V_{DOH} = 2.0V	–	–6.0*2	–	mA
		I_{DOL}	Vcc = 3.0V, V_{DOL} = 1.0V	–	–10.0*2	–	

*1: Conditions ; $V_{CCIF/RF}$ = 3V, Ta = 25°C, in locking state.

*2: Conditions ; Ta = 25°C

■ FUNCTIONAL DESCRIPTIONS

The divide ratio can be calculated using the following equation:

$f_{VCO} = \{(P \times N) + A\} \times f_{OSC} \div R \quad (A < N)$

f_{VCO}: Output frequency of external voltage controlled ocillator (VCO)
P: Preset divide ratio of dual modulus prescaler (16 or 32 for IF-PLL, 64 or 128 for RF-PLL)
N: Preset divide ratio of binary 11-bit programmable counter (5 to 2,047)
A: Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$)
f_{OSC}: Reference oscillation frequency
R: Preset divide ratio of binary 14-bit programmable reference counter (5 to 16,383)

Serial Data Input

Serial data is entered using three pins, Data pin, Clock pin, and LE pin. Programmable dividers of IF/RF–PLL sections, programmable reference dividers of IF/RF PLL sections are controlled individually.
Serial data of binary data is entered through Data pin.
On rising edge of clock, one bit of serial data is transferred into the shift register. When load enable signal is high, the data stored in the shift register is transferred to one of latch of them depending upon the control bit data setting.

Table1. Control Bit

Control bit		Destination of serial data
CN1	CN2	
L	L	The programmable reference counter for the IF-PLL.
H	L	The programmable reference counter for the RF-PLL.
L	H	The programmable counter and the swallow counter for the IF-PLL
H	H	The programmable counter and the swallow counter for the RF-PLL

Shift Register Configuration

Programmable Reference Counter

LSB ↓ Data Flow ⟶ MSB ↓

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
CN1	CN2	T1	T2	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14

CNT1, 2 : Control bit [Table. 1]
R1 to R14 : Divide ratio setting bits for the programmable reference counter (5 to 16,383) [Table. 2]
T1, 2 : Test purpose bit [Table. 3]
NOTE: Data input with MSB first.

Programmable Counter

LSB ↓ Data Flow ⟶ MSB ↓

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
CN1	CN2	LDS	SW	FC	A1	A2	A3	A4	A5	A6	A7	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11

CNT1, 2 : Control bit [Table. 1]
N1 to N14 : Divide ratio setting bits for the programmable counter (5 to 2,047) [Table. 4]
A1 to A7 : Divide ratio setting bits for the swallow counter (0 to 127) [Table. 5]
SW : Divide ratio setting bit for the prescaler (16/17 or 32/33 for the IF-PLL, 64/65 OR 128/129 for the RF-PLL) [Table. 6]
FC : Phase control bit for the phase detector [Table. 7]
LDS : LD/fout signal select bit [Table. 8]
NOTE: Data input with MSB first.

Table2. Binary 14-bit Programmable Reference Counter Data Setting

Divide ratio (R)	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1
5	0	0	0	0	0	0	0	0	0	0	0	1	0	1
6	0	0	0	0	0	0	0	0	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: • Divide ratio less than 5 is prohibited.

Table.3 Test Purpose Bit Setting

T1	T2	LD/fout pin state
L	L	Outputs f_{RIF}
H	L	Outputs f_{RRF}
L	H	Outputs f_{PIF}
H	H	Outputs f_{PRF}

Table.4 Binary 11-bit Programmable Counter Data Setting

Divide ratio (N)	N 11	N 10	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1
5	0	0	0	0	0	0	0	0	1	0	1
6	0	0	0	0	0	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.	.	.	.
2047	1	1	1	1	1	1	1	1	1	1	1

Note: • Divide ratio less than 5 is prohibited.

Table.5 Binary 7-bit Swallow Counter Data Setting

Divide ratio (N)	A 7	A 6	A 5	A 4	A 3	A 2	A 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.
127	1	1	1	1	1	1	1

Note: • Divide ratio (A) range = 0 to 127

Table. 6 Prescaler Data Setting

		SW = "H"	SW = "L"
Prescaler divide ratio	IF-PLL	16/17	32/33
	RF-PLL	64/65	128/129

Table. 7 Phase Comparator Phase Switching Data Setting

	FC = H	FC = L
fr > fp	H	L
fr = fp	Z	Z
fr < fp	L	H
VCO polarity	①	②

Note: • Z = High–impedance
• Depending upon the VCO and LPF polarity, FC bit should be set.

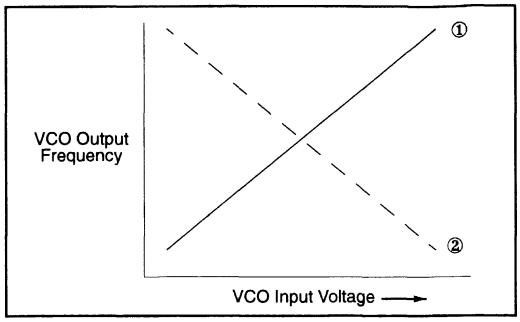
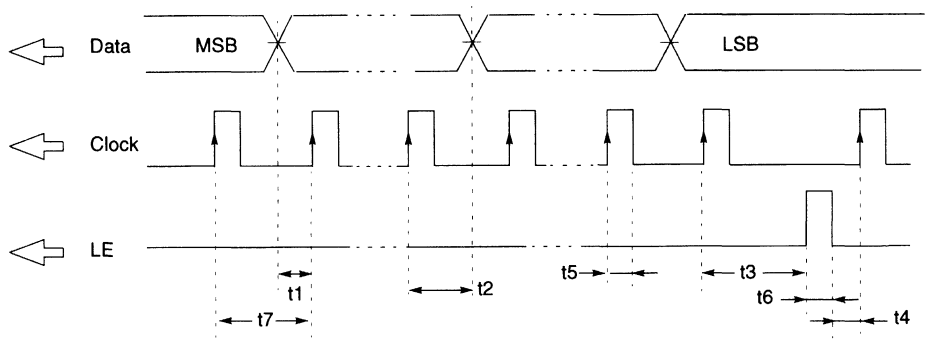


Table. 8 LD/fout Output Select Data Setting

LDS	LD/fout output signal
H	fout ($f_{IF/RF}$, $fp_{IF/RF}$) signals
L	LD signal

Serial Data Input Timing

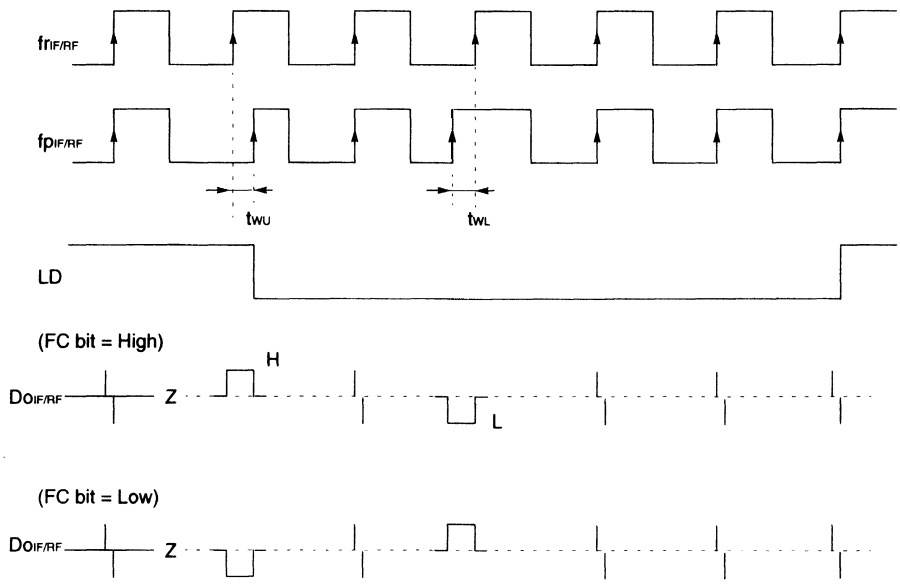


On rising edge of the clock, one bit of the data is transferred into the shift register.

Parameter	Min	Typ	Max	Unit
t1	20	–	–	ns
t2	20	–	–	ns
t3	30	–	–	ns
t4	20	–	–	ns

Parameter	Min	Typ	Max	Unit
t5	30	–	–	ns
t6	100	–	–	ns
t7	100	–	–	ns

■ PHASE DETECTOR OUTPUT WAVEFORM



LD Output Logic Table

IF–PLL section	RF–PLL section	LD output
Locking state / Power saving state	Locking state / Power saving state	H
Locking state / Power saving state	Unlocking state	L
Unlocking state	Locking state / Power saving state	L
Unlocking state	Unlocking state	L

Note: • Phase error detection range = -2π to $+2\pi$

- Pulses on $D_{O_{IF/RF}}$ signals are output to prevent dead zone.
- LD output becomes low when phase error is t_{WU} or more.
- LD output becomes high when phase error is t_{WL} or less and continues to be so for three cycles or more.
- t_{WU} and t_{WL} depend on OSCin input frequency as follows.
  $t_{WU} \geq 8/fosc$: i.e. $t_{WU} \geq 625ns$ when foscin = 12.8 MHz
  $t_{WL} \leq 16/fosc$: i.e. $t_{WL} \leq 1250ns$ when foscin = 12.8 MHz

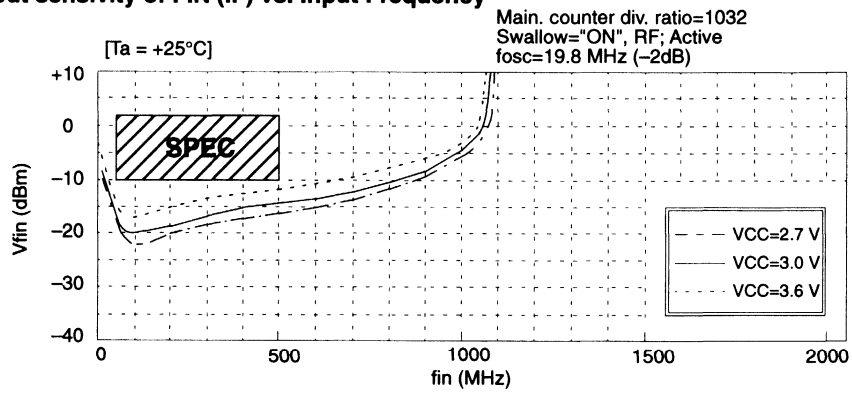
■ POWER SAVING MODE (Intermittent Mode Control Circuit)

Setting a $PS_{IF(RF)}$ pin to Low, IF-PLL (RF-PLL) enters into power saving mode resultant current consumption can be limited to 10μA (typ.). Setting PS pin to High, power saving mode is released so that the device works normally. In addition, the intermittent operation control circuit is included which helps smooth start up from stand by mode. In general, the power consumption can be saved by the intermittent operation that powering down or waking up the synthesizer. Such case, if the PLL is powered up uncontrolled, the resulting phase comparator output signal is unpredictable due to an undefined phase relation between reference frequency (fr) and comparison frequency (fp) and may in the worst case take longer time for lock up of the loop.
To prevent this, the intermittent operation control circuit enforces a limited error signal output of the phase detector during power up. Thus keeping the loop locked.
PS pin must be set "L" at Power-ON.
Allow 1 μs after frequency stabilization on power-up for exiting the power saving mode (PS: L to H)
Serial data can be entered during the power saving mode.
During the power saving mode, the corresponding section except for indispensable circuit for the power saving function stops working, then current consumption is reduced to 10μA per one PLL section.
At that time, the Do and LD become the same state as when a loop is locking. That is, the Do becomes high impedance.
A VCO control voltage is naturally kept at the locking voltage which defined by a LPF's time constant. As a result of this, VCO's frequency is kept at the locking frequency.

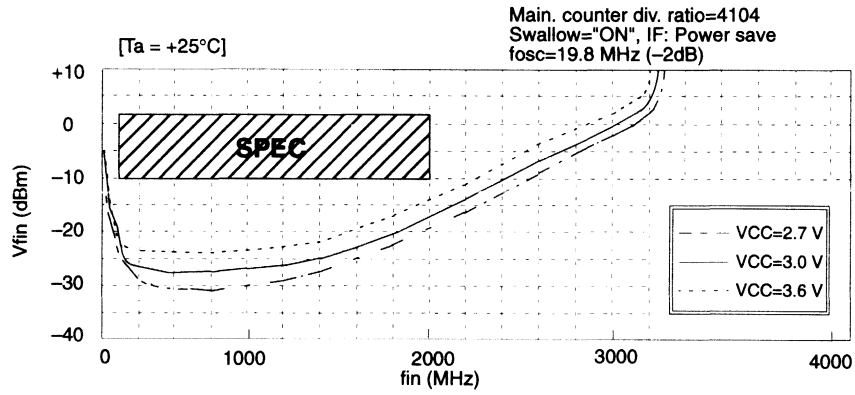
PS_{IF}	PS_{RF}	IF-PLL counters	RF-PLL counters	OSC input buffer
L	L	OFF	OFF	OFF
H	L	ON	OFF	ON
L	H	OFF	ON	ON
H	H	ON	ON	ON

■ TYPICAL CHARACTERISTICS

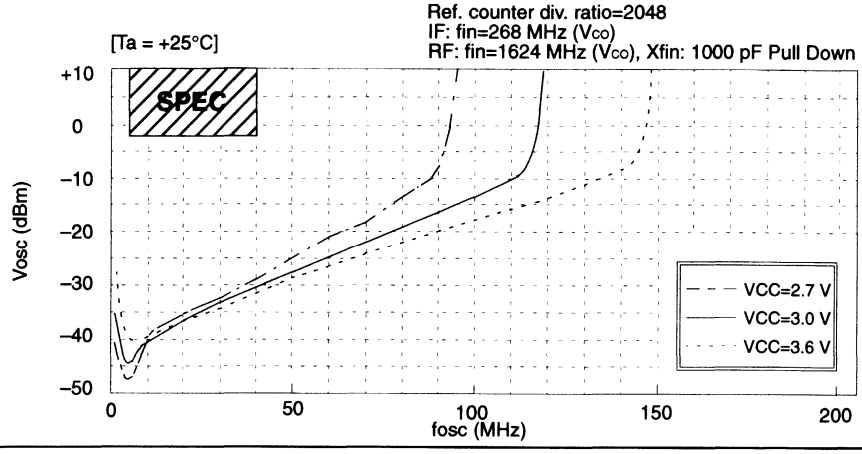
Input sensivity of FIN (IF) vs. Input Frequency



Input sensivity of FIN (RF) vs. Input Frequency



Input sensivity of OSC vs. Input Frequency

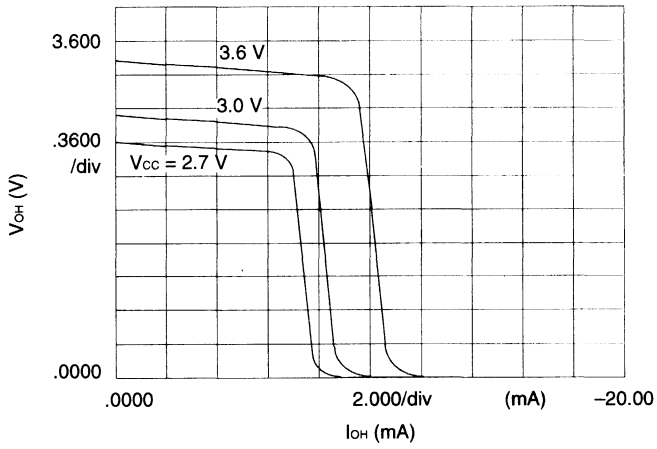


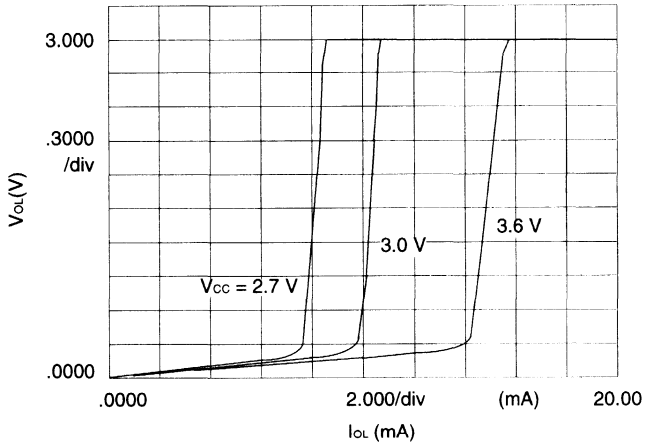
(Continued)

(Continued)

Do output Current

Conditions: Ta = +25°C
V_{CC}= 2.7, 3.0, 3.6 V





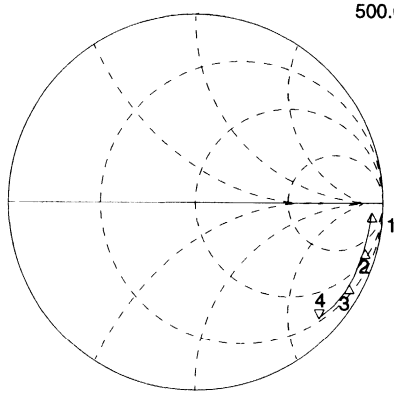
(Continued)

(Continued)

Input Impedance

finIF Pin

4: 19.672 Ω −135.77 Ω 2.3446 pF
500.000 000 MHz



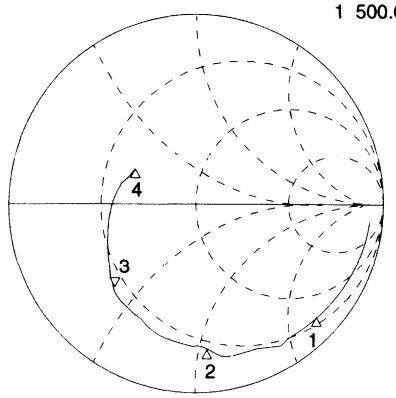
1: 735 Ω
−743.59 Ω
50 MHz

2: 92.609 Ω
−344.72 Ω
200 MHz

3: 34.313 Ω
−200.26 Ω
350 MHz

finRF Pin

3: 14.528 Ω −16.763 Ω 6.3297 pF
1 500.000 000 MHz



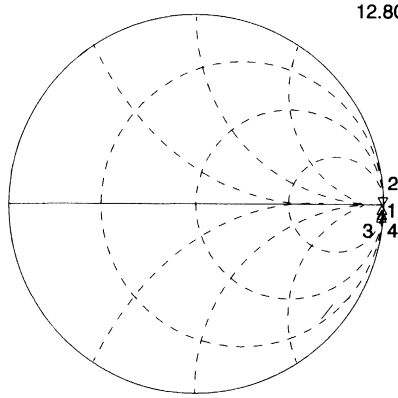
1: 21.984 Ω
−134.74 Ω
500 MHz

2: 12.24 Ω
−52.355 Ω
1 GHz

4: 21.283 Ω
7.4053 Ω
2 GHz

OSCin Pin

2: 052.75 Ω −4.903 kΩ 2.536 pF
12.800 000 MHz



1: 37.324 kΩ
−5.214 kΩ
1 MHz

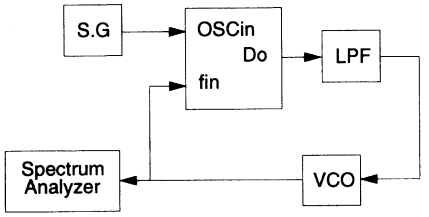
3: 084.5 Ω
−2.5811 kΩ
23 MHz

4: 082.69 Ω
−1.2345 kΩ
50 MHz

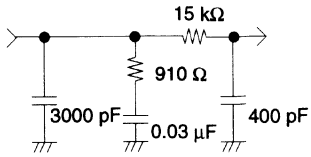
■ REFERENCE INFORMATION

Typical plots measured with the test circuit are shown below. Each plot shows lock up time, phase noise and reference leakage.

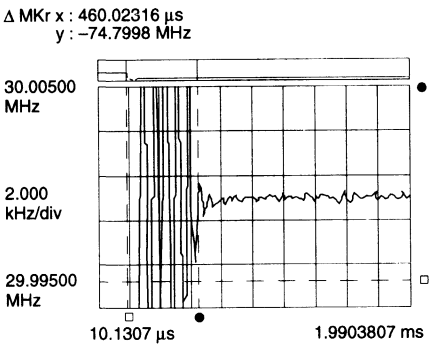
Test Circuit

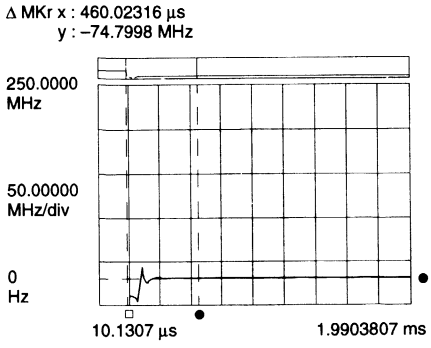


- fvco = 1835 MHz
- Kv = 87 MHz/v
- fr = 200 kHz
- fosc = 13 MHz
- LPF:

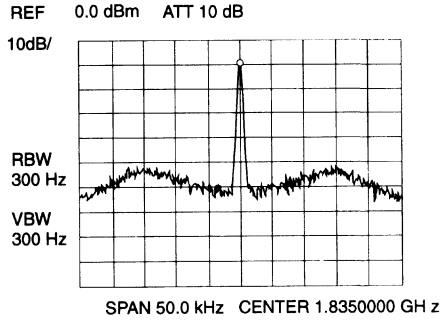


PLL Lock Up Time = 460 µs
(1797.6 MHz → 1872.4 MHz, within ± 1kHz)

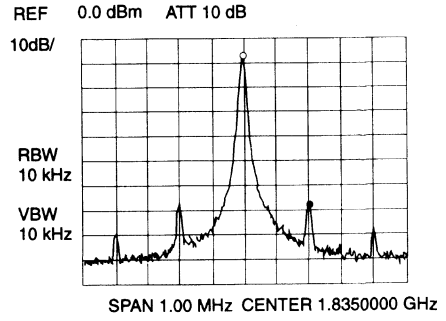




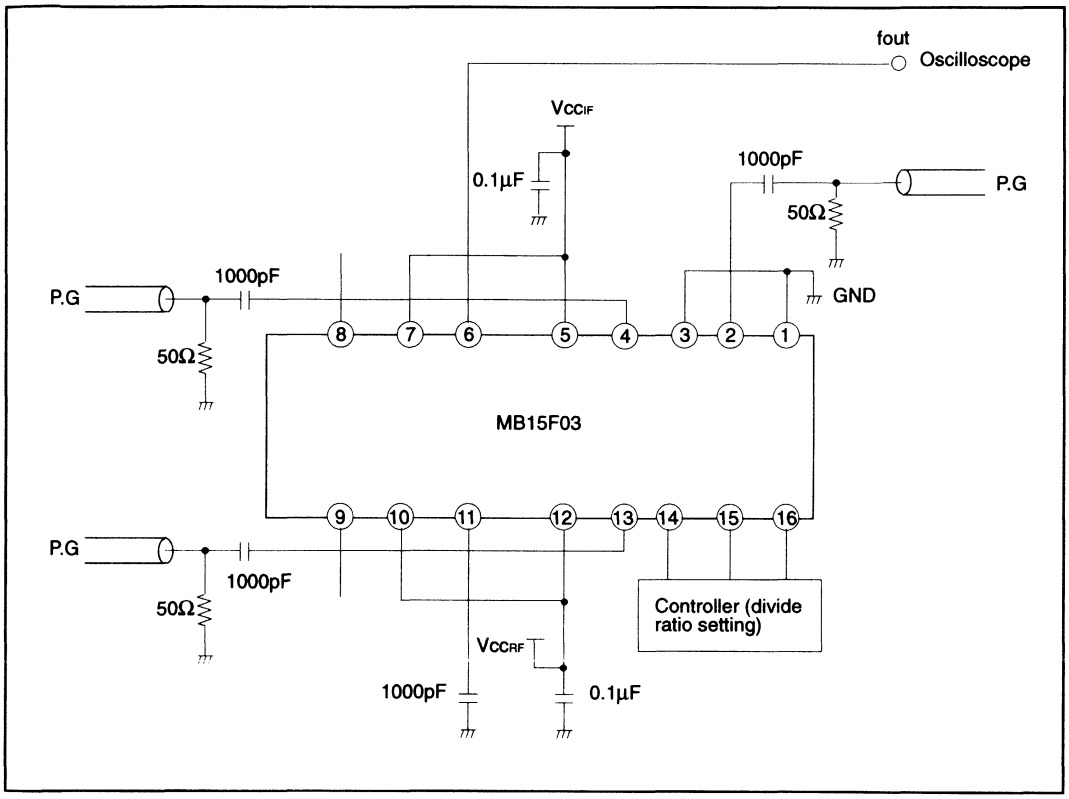
PLL Phase Noise
@ within loop band = 70.1 dBc/Hz



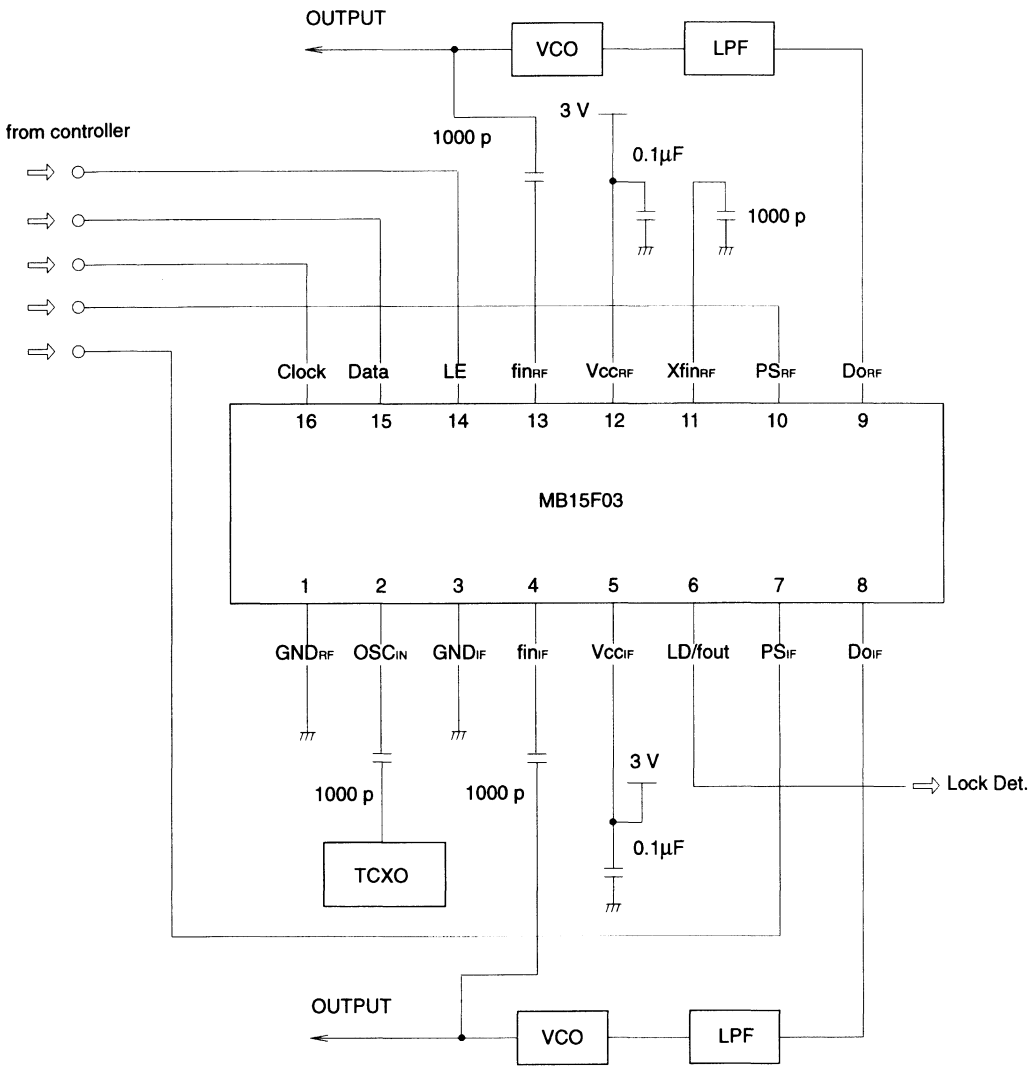
PLL Reference Leakage
@ 200 kHz offset = 59 dBc



■ TEST CIRCUIT (Prescaler Input/Programmable Reference Divider Input Sensitivity Test)



■ APPLICATION EXAMPLE



Clock, Data, LE: Schmitt trigger circuit is provided (insert a pull-down or pull-up resistor to prevent oscillation when open-circuited in the input).

■ ORDERING INFORMATION

Part number	Package	Remarks
MB15F03 PFV	16pin, Plastic SSOP (FPT-16P-M05)	

MEMO

FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-21336-1E

ASSP
Single Serial Input PLL Frequency Synthesizer
On-Chip 2.5 GHz Prescaler

MB15E06

■ DESCRIPTION

The Fujitsu MB15E06 is serial input Phase Locked Loop (PLL) frequency synthesizer with a 2.5 GHz prescaler. A 64/65 or a 128/129 can be selected for the prescaler that enables pulse swallow operation.

The latest BiCMOS process technology is used, resultantly a supply current is limited as low as 8mA typ. This operates with a supply voltage of 3.0V (typ.).

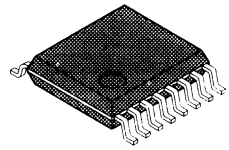
Furthermore, a super charger circuit is included to get a fast tuning as well as low noise performance. As a result of this, MB15E06 is ideally suitable for digital mobile communications, such as GPS (Global Positioning System), Wireless LAN, CATV (CAble TeleVision) etc.

■ FEATURES

- High frequency operation: 2.5 GHz max
- Low power supply voltage: V_{CC} = 2.7 to 3.6V
- Very Low power supply current : I_{CC} = 8.0 mA typ. (V_{CC} = 3V)
- Power saving function : I_{PS} = 10 µA max.
- Pulse swallow function: 64/65 or 128/129
- Serial input 14-bit programmable reference divider: R = 5 to 16,383
- Serial input 18-bit programmable divider consisting of:
  - Binary 7-bit swallow counter: 0 to 127
  - Binary 11-bit programmable counter: 3 to 2,047
- Wide operating temperature: Ta = −40 to 85°C
- Plastic 16-pin SSOP package (FPT-16P-M05)

■ PACKAGE

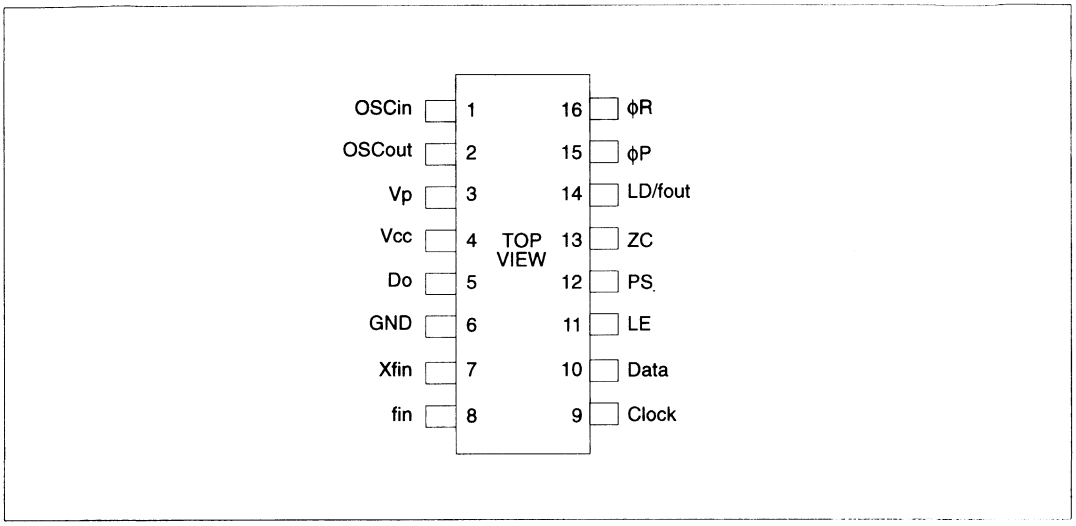
16-pin, Plastic SSOP



(FPT-16P-M05)

This device contains circuitry to protect the inputs against damage due to high static voltages or electroc fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

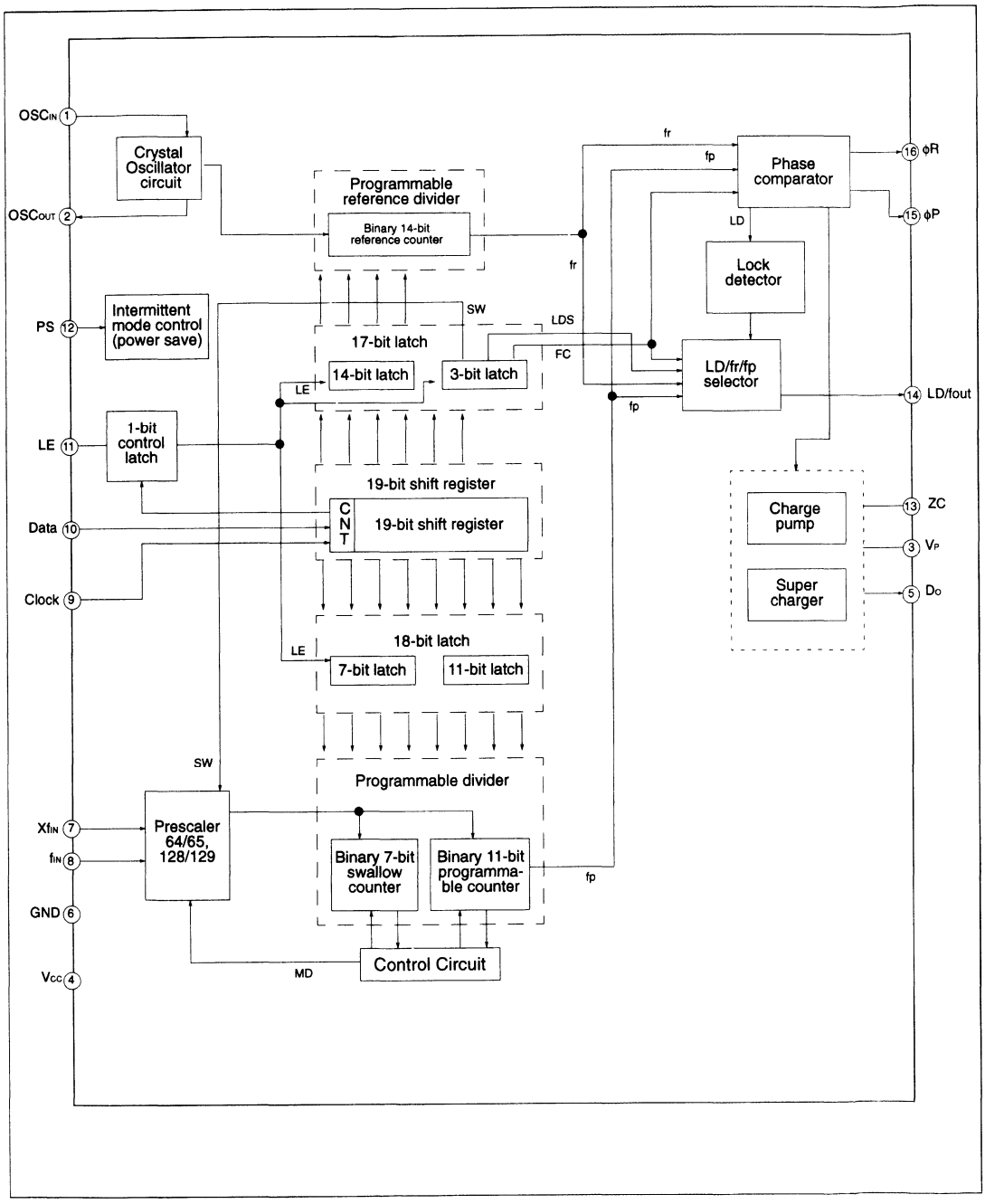
■ PIN ASSIGNMENT



■ PIN DESCRIPTIONS

Pin No.	Pin Name	I/O	Descriptions
1	OSC_{IN}	I	Programmable reference divider input. Oscillator input. Connection for an crystal or a TCXO. TCXO should be connected with a coupling capacitor.
2	OSC_{OUT}	O	Oscillator output. Connection for an external crystal.
3	V_P	–	Power supply voltage input for the charge pump.
4	V_{CC}	–	Power supply voltage input.
5	D_O	O	Charge pump output. Phase of the charge pump can be reversed by FC input.
6	GND	–	Ground.
7	Xfin	I	Prescaler complementary input, and should be grounded via a capacitor.
8	fin	I	Prescaler input. Connection with an external VCO should be done with AC coupling.
9	Clock	I	Clock input for the 19-bit shift register. Data is shifted into the shift register on the rising edge of the clock. *(Open is prohibited.)*
10	Data	I	Serial data input using binary code. The last bit of the data is a control bit. *(Open is prohibited.)* Control bit = "H" ; Data is transmitted to the programmable reference counter. Control bit = "L" ; Data is transmitted to the programmable counter.
11	LE	I	Load enable signal input *(Open is prohibited.)* When LE is high, the data in the shift register is transferred to a latch, according to the control bit in the serial data.
12	PS	I	Power saving mode control. This pin must be set at "L" at Power-ON. *(Open is prohibited.)* PS = "H" ; Normal mode PS = "L" ; Power saving mode
13	ZC	I	Forced high-impedance control for the charge pump (with internal pull up resistor.) ZC = "H" ; Normal Do output. ZC = "L" ; Do becomes high impedance.
14	LD/fout	O	Lock detect signal output(LD)/phase comparator monitoring output (fout). The output signal is selected by LDS bit in the serial data. LDS = "H" ; outputs fout (fr/fp monitoring output) LDS = "L" ; outputs LD ("H" at locking, "L" at unlocking.)
15	ϕP	O	Phase comparator output for an external charge pump.
16	ϕR	O	Phase comparator output for an external charge pump.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Remark
Power supply voltage	V_{CC}	−0.5 to +4.0	V	
	V_P	V_{CC} to +6.0	V	
Input voltage	V_I	−0.5 to V_{CC} +0.5	V	
Output voltage	V_O	−0.5 to V_{CC} +0.5	V	
Storage temperature	T_{stg}	−55 to +125	°C	

Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Remark
		Min	Typ	Max		
Power supply voltage	V_{CC}	2.7	3.0	3.6	V	
	V_P	V_{CC}	–	6.0	V	
Input voltage	V_I	GND	–	V_{CC}	V	
Operating temperature	Ta	−40	–	+85	°C	

Notes: To protect against damage by electrostatic discharge, note the following handling precautions:
-Store and transport devices in conductive containers.
-Use properly grounded workstations, tools, and equipment.
-Turn off power before inserting or removing this device into or from a socket.
-Protect leads with conductive sheet, when transporting a board mounted device.

■ ELECTRICAL CHARACTERISTICS

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Power supply current*1		I_{CC}	fin_{IF} = 2500MHz, fosc = 12MHz	–	8.0	–	mA
Power saving current*2		Ips	Vcc current at PS ="L" and ZC = "H"	–	–	10	µA
Operating frequency		fin		100	–	2500	MHz
Crystal oscillator operating frequency		fosc	min. 500mVp-p	3	–	40	MHz
Input sensitivity	fin	$Vfin_{IF}$	50Ω termination (Refer to the test circuit.)	–10	–	+2	dBm
	OSCin	V_{OSC}		500	–	V_{CC}	mVp–p
Input voltage	Data, Clock, LE, PS, ZC	V_{IH}		Vccx0.7	–	–	V
		V_{IL}		–	–	Vccx0.3	
Input current	Data, Clock, LE, PS	I_{IH}		–1.0	–	+1.0	µA
		I_{IL}		–1.0	–	+1.0	
	ZC	I_{IH}		–1.0	–	+1.0	µA
		I_{IL}	Pull up input	–100	–	0	
	OSCin	I_{IH}		0	–	+100	µA
		I_{IL}		–100	–	0	
Output voltage	φP	V_{OL}	Open drain output	–	–	0.4	V
	φR, LD/fout	V_{OH}		Vcc-0.4	–	–	V
		V_{OL}		–	–	0.4	
	Do	V_{DOH}		Vcc-0.4	–	–	V
		V_{DOL}		–	–	0.4	
High impedance cutoff current	Do	I_{OFF}		–	–	1.1	µA
Output current	φP	I_{OL}	Open drain output	1.0	–	–	mA
	φR, LD/fou	I_{OH}		–	–	–1.0	mA
		I_{OL}		1.0	–	–	
	Do	I_{DOH}	Vcc = 3.0V, Vp = 5V, V_{DOH} = 4.0V	–	–10.0*2	–	mA
		I_{DOL}	Vcc = 3.0V, Vp = 5V, V_{DOL} = 1.0V	–	10.0*2	–	

*1: Conditions ; Vcc = 3.0V, Ta = 25°C, in locking state.

*2: Conditions ; Ta = 25°C

■ FUNCTION DESCRIPTIONS

Pulse Swallow Function

The divide ratio can be calculated using the following equation:

$f_{VCO} = [(M \times N) + A] \times f_{OSC} \div R \quad (A < N)$

- f_{VCO} : Output frequency of external voltage controlled oscillator (VCO)
- N : Preset divide ratio of binary 11-bit programmable counter (5 to 2,047)
- A : Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$)
- f_{OSC} : Output frequency of the reference frequency oscillator
- R : Preset divide ratio of binary 14-bit programmable reference counter (5 to 16,383)
- M : Preset divide ratio of modules prescaler (64 or 128)

Serial Data Input

Serial data is processed using the Data, Clock, and LE pins. Serial data controls the programmable reference divider and the programmable divider separately.
Binary serial data is entered through the Data pin.
One bit of data is shifted into the shift register on the rising edge of the clock. When the load enable pin is high, stored data is latched according to the control bit data as follows:

Table.1 Control Bit

Control bit (CNT)	Destination of serial data
H	17 bit latch (for the programmable reference divider)
L	18 bit latch (for the programmable divider)

Shift Register Configuration

Programmable Reference Counter

LSB ← Data Flow → MSB

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
CNT	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	SW	FC	LDS

CNT : Control bit [Table. 1]
R1 to R14 : Divide ratio setting bit for the programmable reference counter (5 to 16,383) [Table. 2]
SW : Divide ratio setting bit for the prescaler (64/65 or 128/129) [Table. 5]
FC : Phase control bit for the phase comparator [Table. 7]
LDS : LD/fout signal select bit [Table. 6]

Note: Start data input with MSB first

Programmable Reference Counter

LSB ↓ Data Flow → MSB ↓

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
CNT	A1	A2	A3	A4	A5	A6	A7	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11

CNT : Control bit [Table. 1]
N1 to N11 : Divide ratio setting bits for the programmable counter (5 to 2,047) [Table. 3]
A1 to A7 : Divide ratio setting bits for the swallow counter (0 to 127) [Table. 4]

Note: Start data input with MSB first

Table2. Binary 14-bit Programmable Reference Counter Data Setting

Divide ratio (R)	R 14	R 13	R 12	R 11	R 10	R 9	R 8	R 7	R 6	R 5	R 4	R 3	R 2	R 1
5	0	0	0	0	0	0	0	0	0	0	0	1	0	1
6	0	0	0	0	0	0	0	0	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: • Divide ratio less than 5 is prohibited.

Table.3 Binary 11-bit Programmable Counter Data Setting

Divide ratio (N)	N 11	N 10	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1
5	0	0	0	0	0	0	0	0	1	0	1
6	0	0	0	0	0	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.	.	.	.
2047	1	1	1	1	1	1	1	1	1	1	1

Note: • Divide ratio less than 5 is prohibited.
• Divide ratio (N) range = 5 to 2,047

Table.4 Binary 7-bit Swallow Counter Data Setting

Divide ratio (A)	A 7	A 6	A 5	A 4	A 3	A 2	A 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.
127	1	1	1	1	1	1	1

Note: • Divide ratio (A) range = 0 to 127

Table. 5 Prescaler Data Setting

SW	Prescaler Divide ratio
H	64/65
L	128/129

Table. 6 LD/fout Output Select Data Setting

LDS	LD/fout output signal
H	fout signal
L	LD signal

Relation between the FC input and phase characteristics

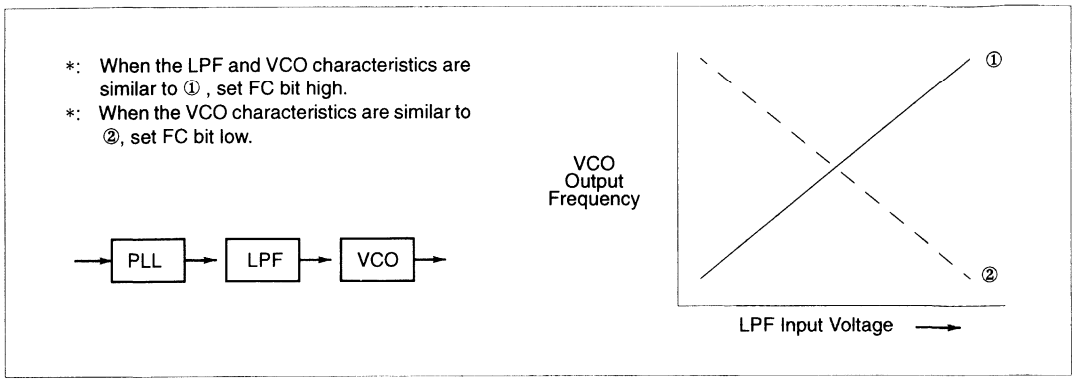
The FC bit changes the phase characteristics of the phase comparator. Both the internal charge pump output level (D_O) and the phase comparator output (ϕR, ϕP) are reversed according to the FC bit. Also, the monitor pin (f_{OUT}) output is controlled by the FC bit. The relationship between the FC bit and each of D_O, ϕR, and ϕP is shown below.

Table. 7 FC Bit Data Setting (LDS = "H")

	FC = High				FC = Low			
	Do	ϕR	ϕP	LD/fout	Do	ϕR	ϕP	LD/fout
$f_r > f_p$	H	L	L	(fr)	L	H	Z*	(fp)
$f_r < f_p$	L	H	Z*	(fr)	H	L	L	(fp)
$f_r = f_p$	Z*	L	Z*	(fr)	Z*	L	Z*	(fp)

* : High impedance

When designing a synthesizer, the FC pin setting depends on the VCO and LPF characteristics.



Power Saving Mode (Intermittent Mode Control Circuit)

Setting a PS pin to Low, the IC enters into power saving mode resultatly current sonsumption can be limited to 10μA (max.). Setting PS pin to High, power saving mode is released so that the IC works normally.
In addition, the intermittent operation control circuit is included which helps smooth start up from the power saving mode. In general, the power consumption can be saved by the intermittent operation that powering down or waking up the synthesizer. Such case, if the PLL is powered up uncontrolled, the resulting phase comparator output signal is unpredictable due to an undefined phase relation between reference frequency (f_r) and comparison frequency (f_p) and may in the worst case take longer time for lock up of the loop.
To prevent this, the intermittent operation control circuit enforces a limited error signal output of the phase detector during power up, thus keeping the loop locked.
During the power saving mode, the corresponding section except for indispensable circuit for the power saving function stops working, then current consumption is reduced to 10 μA per one PLL section.
At that time, the Do and LD become the same state as when a loop is locking. That is, the Do becomes high impedance.
A VCO control voltage is naturally kept at the locking voltage which defined by a LPF"s time constant. As a result of this, VCO's frequency is kept at the locking frequency.

Note: • *While the power saving mode is executed, ZC pin should be set at "H" or open. If ZC is set at "L" during power saving mode, approximately 10 μA current flows.*
- *PS pin must be set "L" at Power-ON.*
- *The power saving mode can be released (PS : L → H) 1μs later after power supply remains stable.*
- *During the power saving mode, it is possible to input the serial data.*

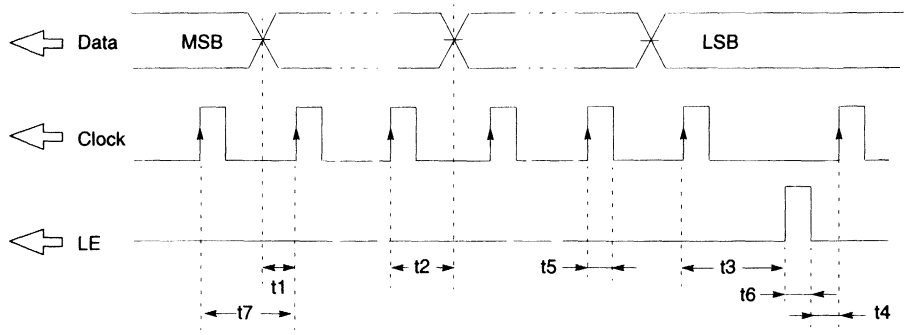
Table.8 PS Pin Setting

PS pin	Status
H	Normal mode
L	Power saving mode

Table.9 ZC Pin Setting

ZC pin	Do output
H	Normal output
L	High impedance

■ SERIAL DATA INPUT TIMING

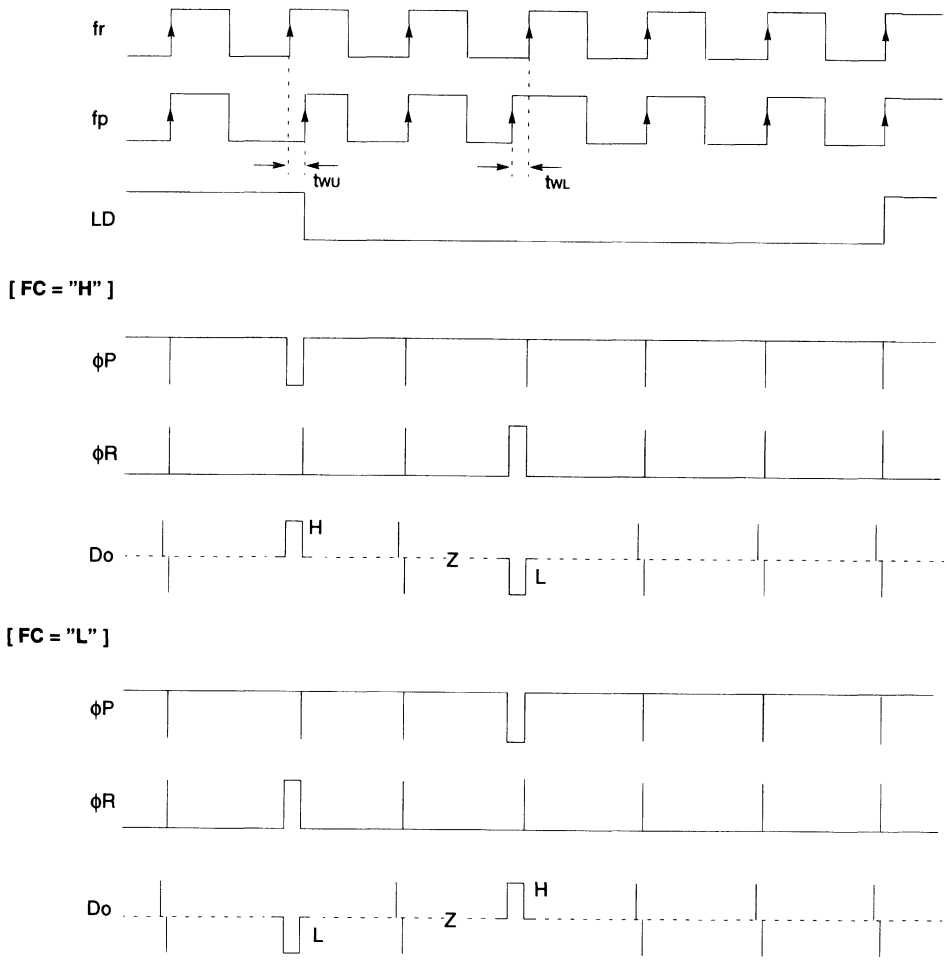


On rising edge of the clock, one bit of the data is transferred into the shift register.

Parameter	Min.	Typ.	Max.	Unit
t1	20	–	–	ns
t2	20	–	–	ns
t3	30	–	–	ns
t4	20	–	–	ns

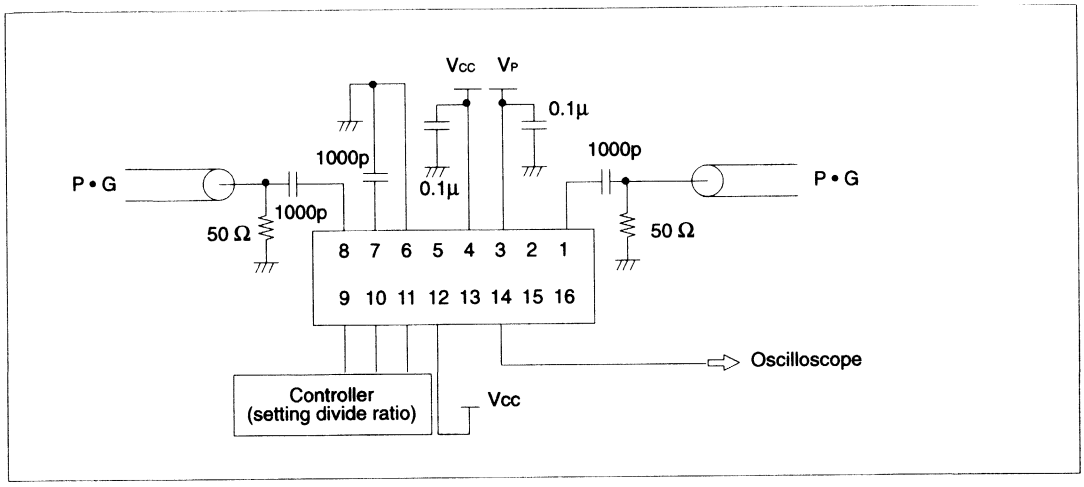
Parameter	Min.	Typ.	Max.	Unit
t5	30	–	–	ns
t6	100	–	–	ns
t7	100	–	–	ns

■ PHASE COMPARATOR OUTPUT WAVEFORM

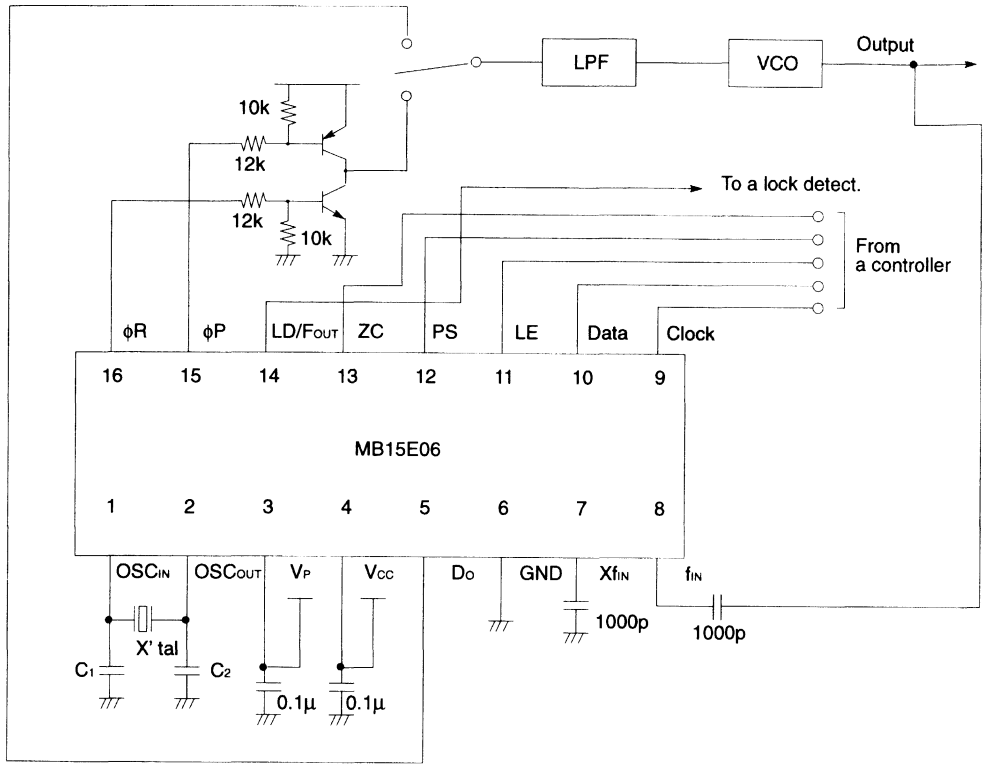


Notes:
1. Phase error detection range: -2π to $+2\pi$
2. Pulses on Do output signal during locked state are output to prevent dead zone.
3. LD output becomes low when phase is twu or more. LD output becomes high when phase error is twL or less and continues to be so for three cysles or more.
4. twu and twL depend on OSCin input frequency.
   twu ≥ 8/fosc (e. g. twu ≥ 625ns, foscin = 12.8 MHz)
   twL ≤ 16/fosc (e. g. twL ≤ 1250ns, foscin = 12.8 MHz)
5. LD becomes high during the power saving mode (PS = "L".)

■ TEST CIRCUIT (for Measuring Input Sensitivity fin/OSCin)



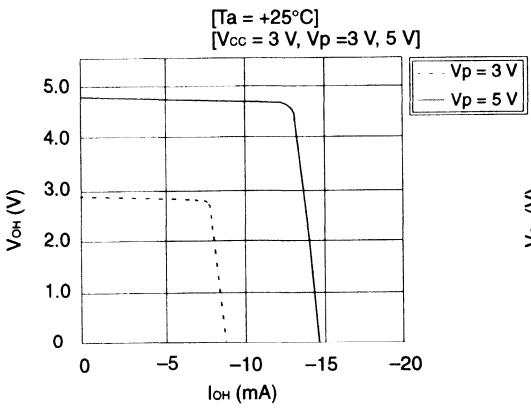
■ APPLICATION EXAMPLE

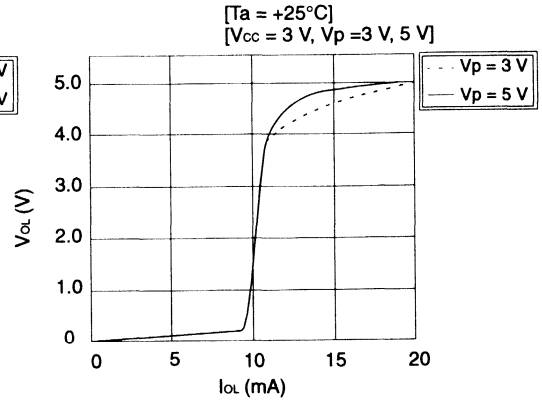


C_1, C_2 : Depend on the crystal parameters

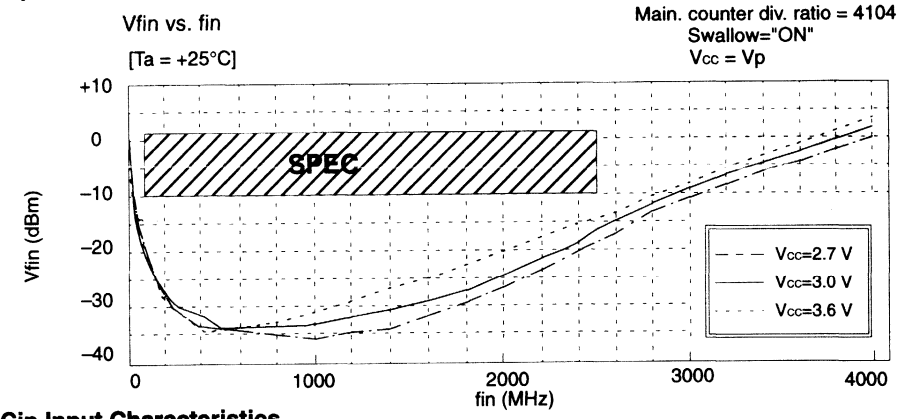
■ TYPICAL CHARACTERISTICS

Do Output Current

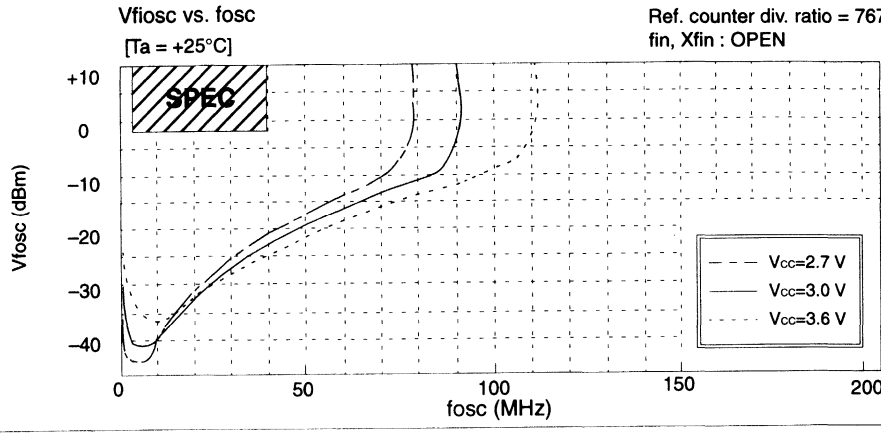




fin Input Sensitivity



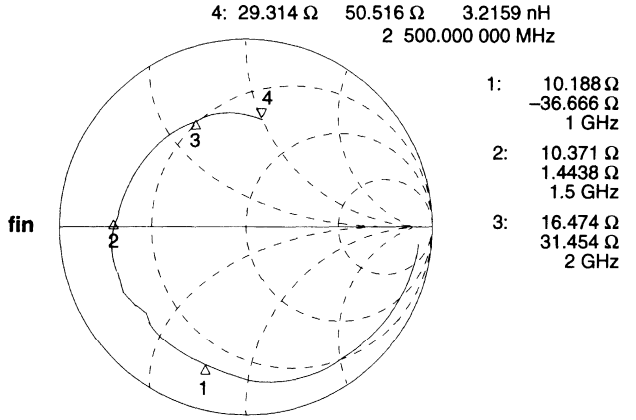
OSCin Input Characteristics



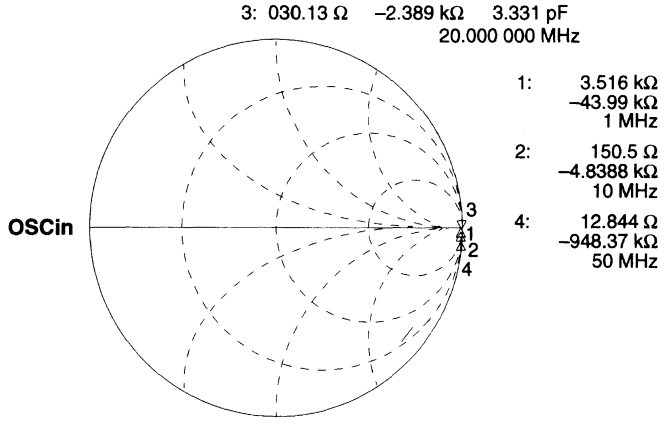
(Continued)

(Continued)

fin Input Impedance



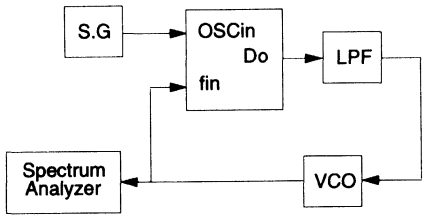
OSCin Input Impedance



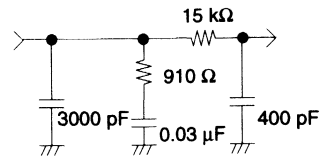
■ REFERENCE INFORMATION

Typical plots measured with the test circuit are shown below. Each plot shows lock up time, phase noise and reference leakage.

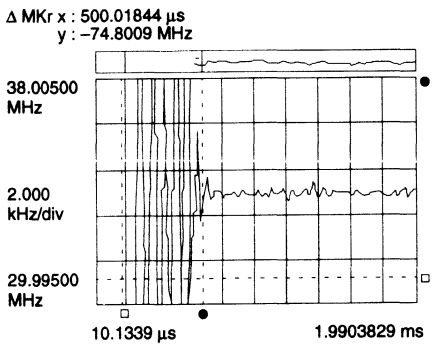
Test Circuit



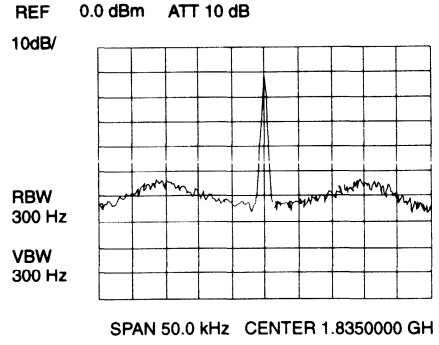
- fvco = 1835 MHz
- Kv = 87 MHz/v
- fr = 200 kHz
- fosc = 13 MHz
- LPF:

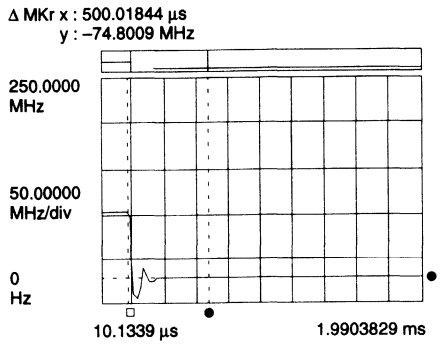


PLL Lock Up Time = 500 µs
(1797.6 MHz → 1872.4 MHz, within ± 1kHz)

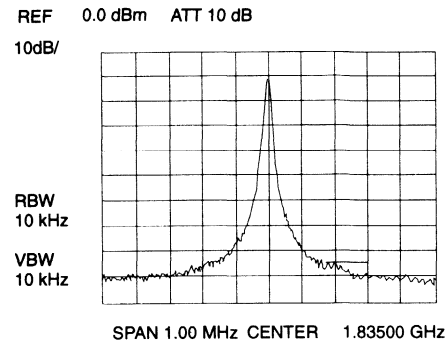


PLL Phase Noise
@ within loop band = 69.4 dBc/Hz





PLL Reference Leakage
@ 200 kHz offset = 74.6 dBc



■ ORDERING INFORMATION

Part number	Package	Remarks
MB15E06PFV1	16-pin Plastic SSOP (FPT-16P-M05)	

FUJITSU SEMICONDUCTOR
DATA SHEET

DS04–21317–2E

ASSP For DTS

Bi-CMOS

2.5GHz PLL FREQUENCY SYNTHESIZER
for built-in prescalar

MB1515

■ DESCRIPTION

The MB1515 is a serial input PLL (Phase-Locked Loop) frequency synthesizer with a built-in prescaler allowing for a pulse swallow system in the two modulus 2.5 GHz band. It is suitable for BS and TV tuners and CATV systems.

The synthesizer is powered by 5 V (typical). Using the latest proprietary process, current consumption has been reduced to Icc = 16 mA (typical).

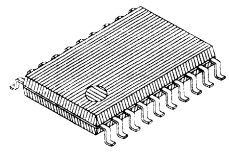
■ FEATURES

- Supply voltage: Vcc = 5 V
- High-speed operation capability: fin = 2.5 GHz (Vin = – 4 dBm)
- Low current consumption: Icc = 16 mA (typical)
- Broad operating temperature range: Ta = – 40°C to +85°C

(Continued)

■ PACKAGE

20-pin Plastic SSOP



(FPT-20P-M03)

(Continued)

- Integrated Functions

  24-bit shift register

  24-bit latch

  Reference divider

  Binary 2-bit programmable reference counter (Divide ratios: 256, 512, 1024, and 2048)

  Comparison Divider

  Binary 5-bit swallow counter (Divide ratios: 0 to 31)

  Binary 12-bit bit programmable counter (Divide ratios: 32 to 4095)

  Phase comparator with phase conversion feature

  Two modulus prescaler for 2.5 GHz band (Divide ratios: 256/272 and 512/528)

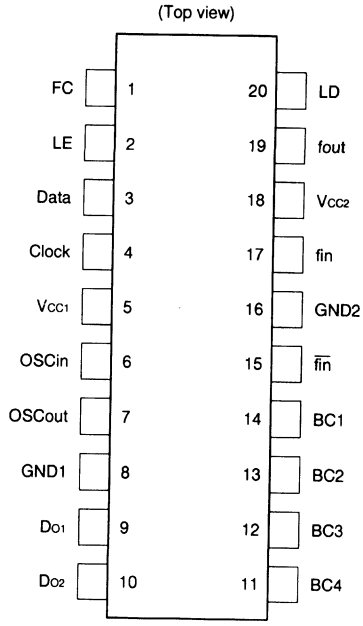
  4-bit band switching signals

  Control signal generator

  Crystal oscillator

  Charge pump

■ PIN ASSIGNMENT



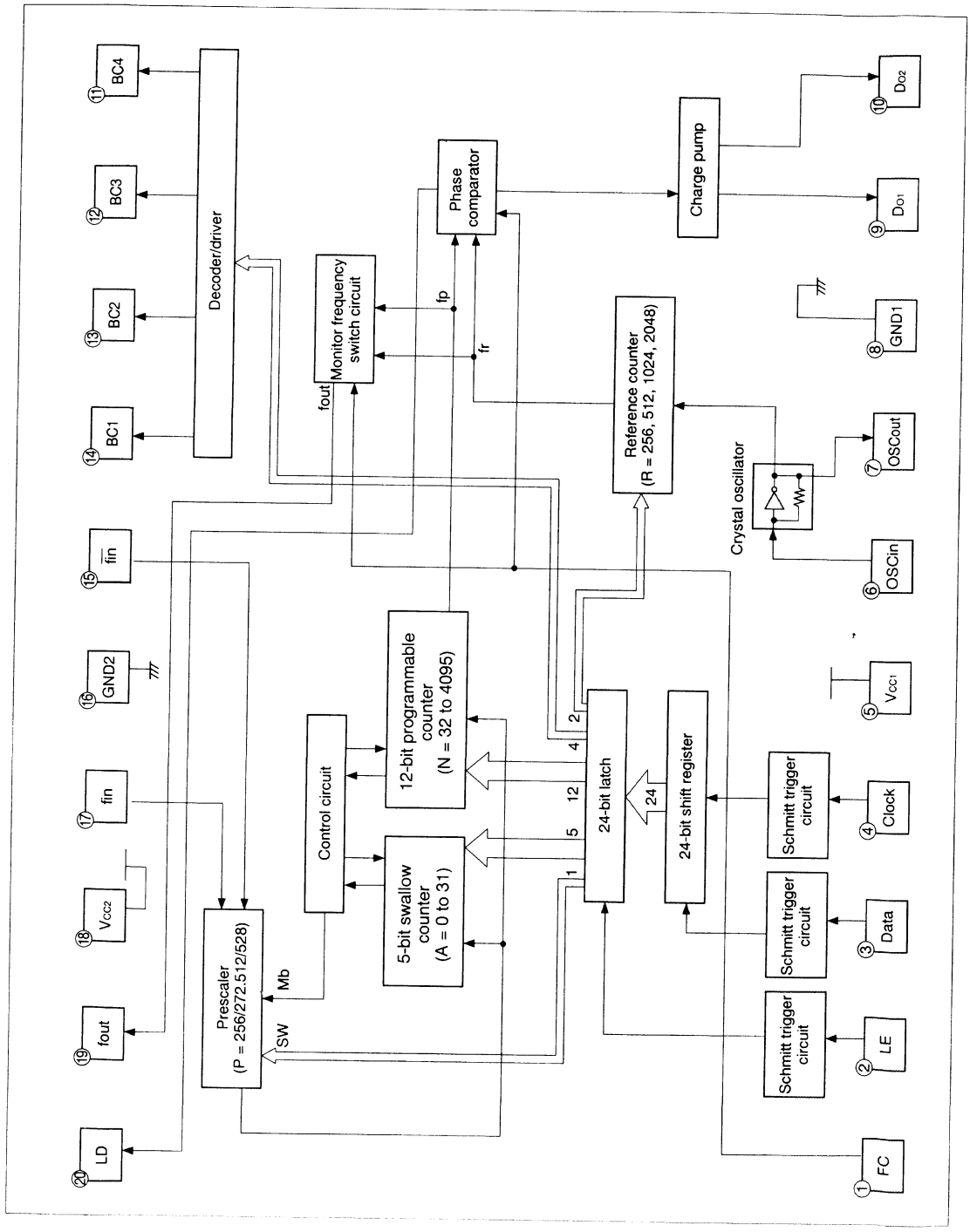
(FPT-20P-M03)

■ PIN DESCRIPTION

Pin No.	Pin name	I/O	Description
1	FC	I	Phase switch input pin to the phase comparator (with pull up resistor). This pin allows for inverting the polarity of phase comparator output, according to the polarity of the externally connected LPF and VCO. When FC is at "L" level, charge pump and phase comparator characteristics are reversed. This pin also toggles the output of the fout pin (test pin) between fr and fp.
2	LE	I	Load enable signal input pin (with Schmitt trigger circuit). The pin sends shift register contents to the latch when LE is at "H" (or open).
3	Data	I	Serial data input pin using binary codes (with Schmitt trigger circuit).
4	Clock	I	24-bit shift register clock input pin (with Schmitt trigger circuit). Data is read at the rising edge of the clock pulse.
5	V_{CC1}	—	Power supply pin (for PLL).
6	OSCin	I	Crystal oscillator connect pin and reference divider input pin. (OSCin: Oscillator input pin, OSCout: Oscillator output pin)
7	OSCout	O	
8	GND1	—	Grounding pin (for PLL)
9	D_{O1}	O	Charge pump output pin. Phase characteristics invert with FC pin settings.
10	D_{O2}	O	
11	BC4	O	Band switch output pin (open collector output). Output is controlled by the serial data band bit setting. When BCX bit is "H," the BCX output transistor turns ON. When BCX bit is "L," the BCX output transistor turns OFF. (X: 1 to 4)
12	BC3	O	
13	BC2	O	
14	BC1	O	
15	$\overline{fin}$	I	fin's complementary input pin. Connect to ground via a capacitor.
16	GND2	—	Ground pin (for prescaler).
17	fin	I	Prescaler input pin. Input using ac coupling.
18	V_{CC2}	—	Power supply pin (for prescaler).
19	fout	O	Phase comparator input monitor pin. Produces either the reference divider output (fr) or the comparison divider output (fp) signal depending on the FC pin's input level.
20	LD	O	Phase comparator output pin. LD is usually "H," and is set to "L" for the duration equivalent to the phase error between fr and fp.

FC	Output signal
"H"	fr
"L"	fp

■ BLOCK DIAGRAM



■ MAXIMUM RATINGS

Parameter	Symbol	Value	Units
Supply voltage	V_{CC}	−0.5 to +7.0	V
Output voltage	V_O	−0.5 to V_{CC}+0.5	V
Output current	I_O	±10	mA
Storage temperature	Tstg	−55 to +125	°C

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Units
		Min.	Typical	Max.	
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_I	GND	—	V_{CC}	V
Operating temperature	Ta	−40	—	+85	°C

Notes: To prevent damage caused by static electricity, an antistatic element is added and antistatic enhancement is also built into the circuit. However, the following handling cautions must be observed:

- Contain the device in a conductive case when storing or transporting it.
- Before handling, verify that the person handling the device, fixtures, and tools are not charged (grounded). Use a grounded conductive sheet as the work surface.
- Turn off power before connecting or disconnecting the device to or from the socket.
- Protect the lead with a conductive sheet when handling (such as transporting) a board on which this device is mounted.

■ ELECTRICAL CHARACTERISTICS

Parameter		Symbol	Condition	Value			Units
				Min.	Typical	Max.	
Power supply current		I_{CC}	When input at fin = 2.5GHz and OSCin = 4MHz, Vcc = 5V. Other input pins are GND and output pins are open.	—	16.0	—	mA
Operating frequency	f_{in}	f_{in}	Must be AC-coupled. The minimum operating frequency when coupled at 1000 pF.	100	—	2500	MHz
	OSC_{in}	f_{OSC}	—	—	4	10	MHz
Permissible input voltage	f_{in}	V_{fin1}	2300 to 2500 MHz	− 4	—	6	dBm
		V_{fin2}	1900 to 2300 MHz	− 7	—	6	dBm
		V_{fin3}	1000 to 1900 MHz	− 10	—	6	dBm
		V_{fin4}	100 to 1000 MHz	− 20	—	6	dBm
	OSC_{in}	V_{OSC}	—	0.5	—	—	V_{P-P}
High level input voltage	Other than f_{in} and OSC_{in}	V_{IH}	—	$V_{CC} \times 0.7 + 0.4$	—	—	V
Low level input voltage		V_{IL}	—	—	—	$V_{CC} \times 0.3 - 0.4$	V
High level input current	Data, Clock, LE	I_{IH}	—	—	1.0	—	μA
Low level input current		I_{IL}	—	—	− 1.0	—	μA
	FC	I_{ILFC}	—	—	− 60	—	μA
Input current	OSC_{in}	I_{IOSC}	—	—	± 50	—	μA
High level output voltage	Excluding Do and BC	V_{OH}	When V_{CC} = 5 V	4.4	—	—	V
Low level output voltage		V_{OL}	—	—	—	0.4	V
High impedance cutoff current	Do1, 2 BC 1 to 4	I_{OFF}	—	—	—	1.1	μA
Output current	Excluding Do and BC	I_{OH}	—	− 1.0	—	—	mA
		I_{OL}	—	1.0	—	—	mA
Output voltage breakdown	BC1 to 4	V_B	—	—	—	12	V

■ FUNCTIONAL DESCRIPTIONS

1. Formula for calculation of divide ratio

Set divider's divide ratio according to the following formula:

$$fvco = [(P \times N) + (16 \times A)] \times fosc \div R$$

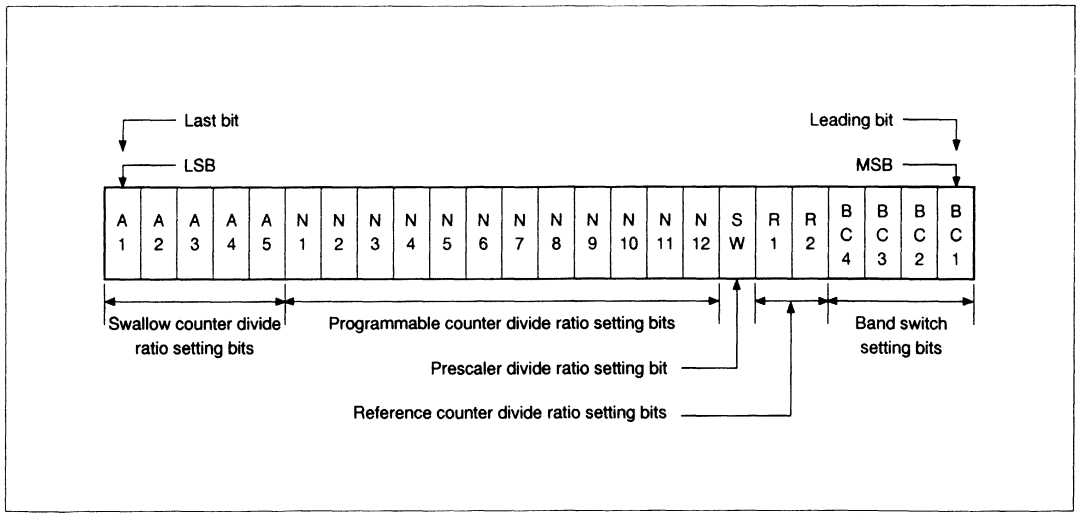
where

fvco : Externally connected VCO output frequency
P : Prescaler divide ratio (256 or 512)
N : Binary 12-bit programmable counter setting (32 to 4095)
A : Binary 5-bit swallow counter setting (0 to 31)
fosc : Reference oscillation frequency
R : Reference counter setting (256, 512, 1024, 2048)

2. Serial data input procedure

Serial data is input from three inputs, Data pin, Clock pin and LE pin, allowing for control of the 4-bit band switch setting, the 3-bit reference divider and the 17-bit comparison divider respectively. The data is sequentially fetched into the internal shift register at the rising edge of the clock and transferred to the latch when load enable is at the "H" level.

The 24-bit shift register is configured as follows:



- **Band switch setting (BC1 to BC4)**
  When data set in the band bits is at "H," output is turned ON. When data is at "L," output is turned OFF.

- **Prescaler divide ratio (SW)**
  Divided by 256/272 when data set in the SW bit is at "H." Divided by 512/528 when data is at "L."

- **Divide ratios for 5-bit swallow counter (A1 to A5)**

Divide ratio A	A5	A4	A3	A2	A1
0	0	0	0	0	0
1	0	0	0	0	1
2	0	0	0	1	0
• •	• •	• •	• •	• •	• •
31	1	1	1	1	1

(Setting: 0 to 31)

- **Reference counter divide ratios (R1 and R2)**

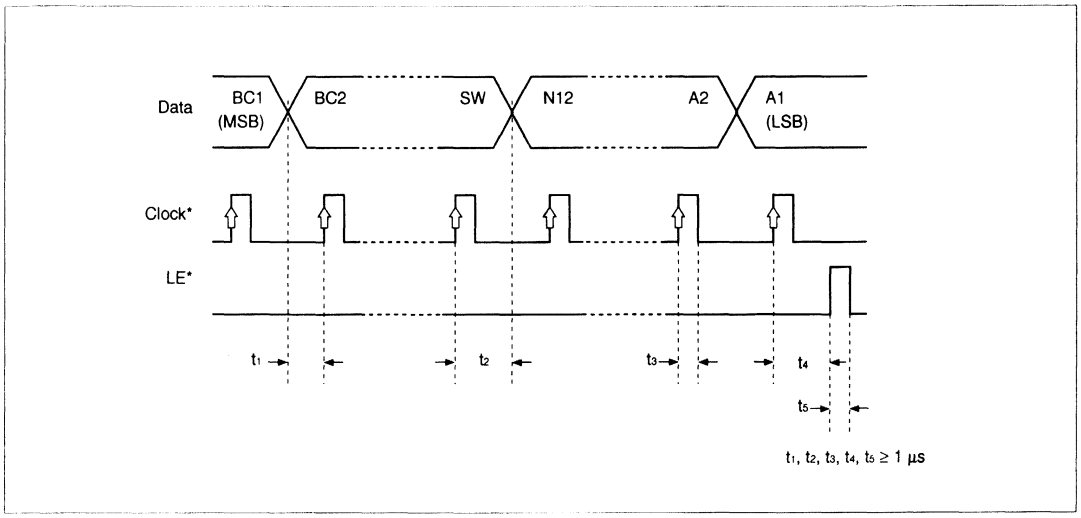
Divide ratio R	R2	R1
256	0	0
512	0	1
1024	1	0
2048	1	1

- **Divide ratios for 12-bit programmable counter (N1 to N12)**

Divide ratios	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1
0	0	0	0	0	0	0	1	0	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0	0	1
2	0	0	0	0	0	0	1	0	0	0	1	0
• •	• •	• •	• •	• •	• •	• •	• •	• •	• •	• •	• •	• •
4095	1	1	1	1	1	1	1	1	1	1	1	1

(Setting: 0 to 4095)

3. Serial data input timings



*: Fetches data at the rising edge of the clock.
*: Fetches data when LE is at "H" level.

4. FC pin input in relation to phase characteristics

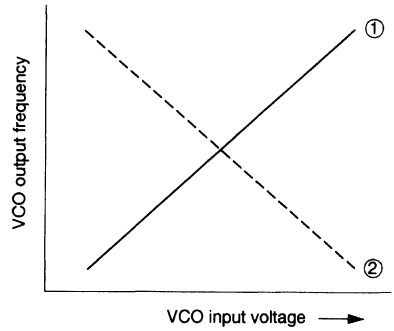
The FC pin switches the phase of the phase comparator. Phase characteristics (charge pump output) are inverted by controlling this pin. Output from the phase comparator input monitor pin (fout) is also controlled by this FC pin. The relation of FC pin input with Do and fout is as follows:

	FC: "H" (or open)		FC: "L"	
	D_{O1}, D_{O2}	fout	D_{O1}, D_{O2}	fout
fr > fp	H	Outputs reference divider output (fr)	L	Outputs comparison divider output (fp)
fr = fp	Z		Z	
fr < fp	L		H	

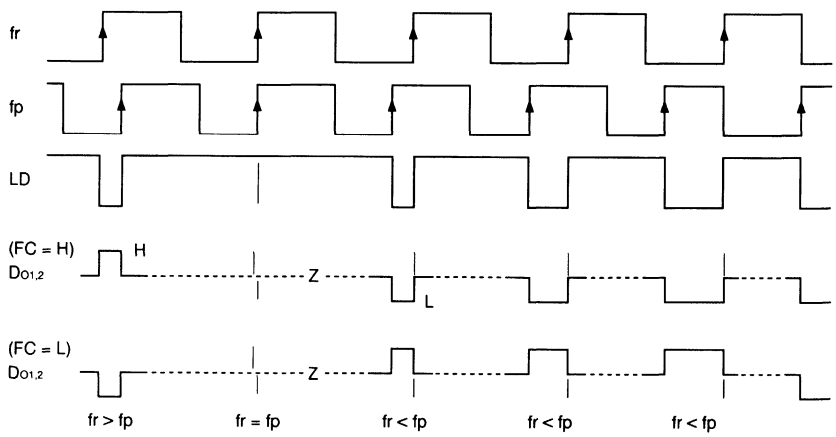
Z: high impedance

When designing the synthesizer, control the FC pin according to the VCO polarity.

- When the VCO polarity is ① in the figure, the FC pin is either at "H" or open.
- When the VCO polarity is ② in the figure, the FC pin is at "L".

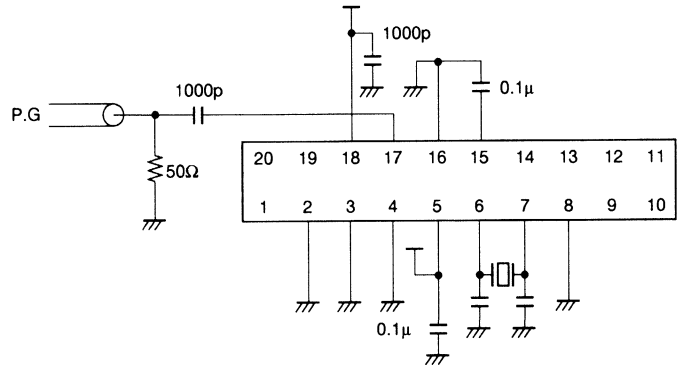


■ PHASE COMPARATOR OUTPUT WAVEFORMS



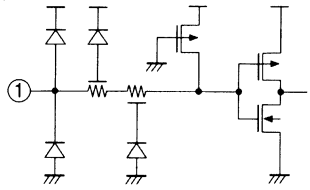
Notes:
- The phase error is detected in a range of -2π to $+2\pi$.
- Output of a "glitch" varies slightly with charge pump characteristics. This "glitch" is output to eliminate an dead band.

■ EXAMPLE MEASUREMENT CIRCUIT (PRESCALER INPUT SENSITIVITY)

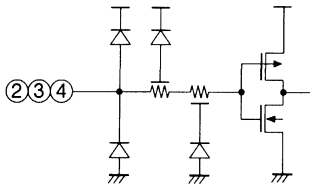


■ EQUIVALENT CIRCUIT DIAGRAM

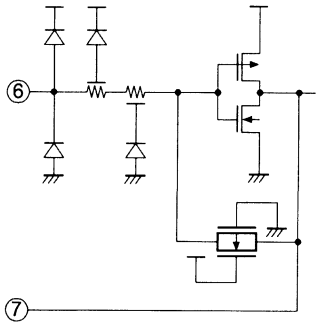
• FC



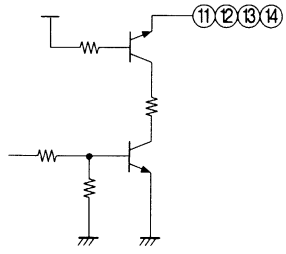
• LE, Data, clock



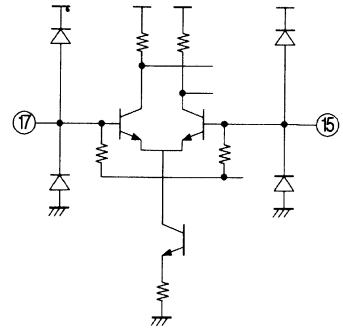
• OSCin, OSCout



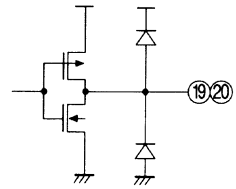
• BC1, BC2, BC3, BC4



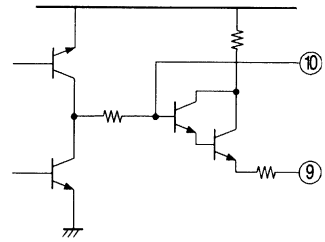
• $\overline{fin}$, fin



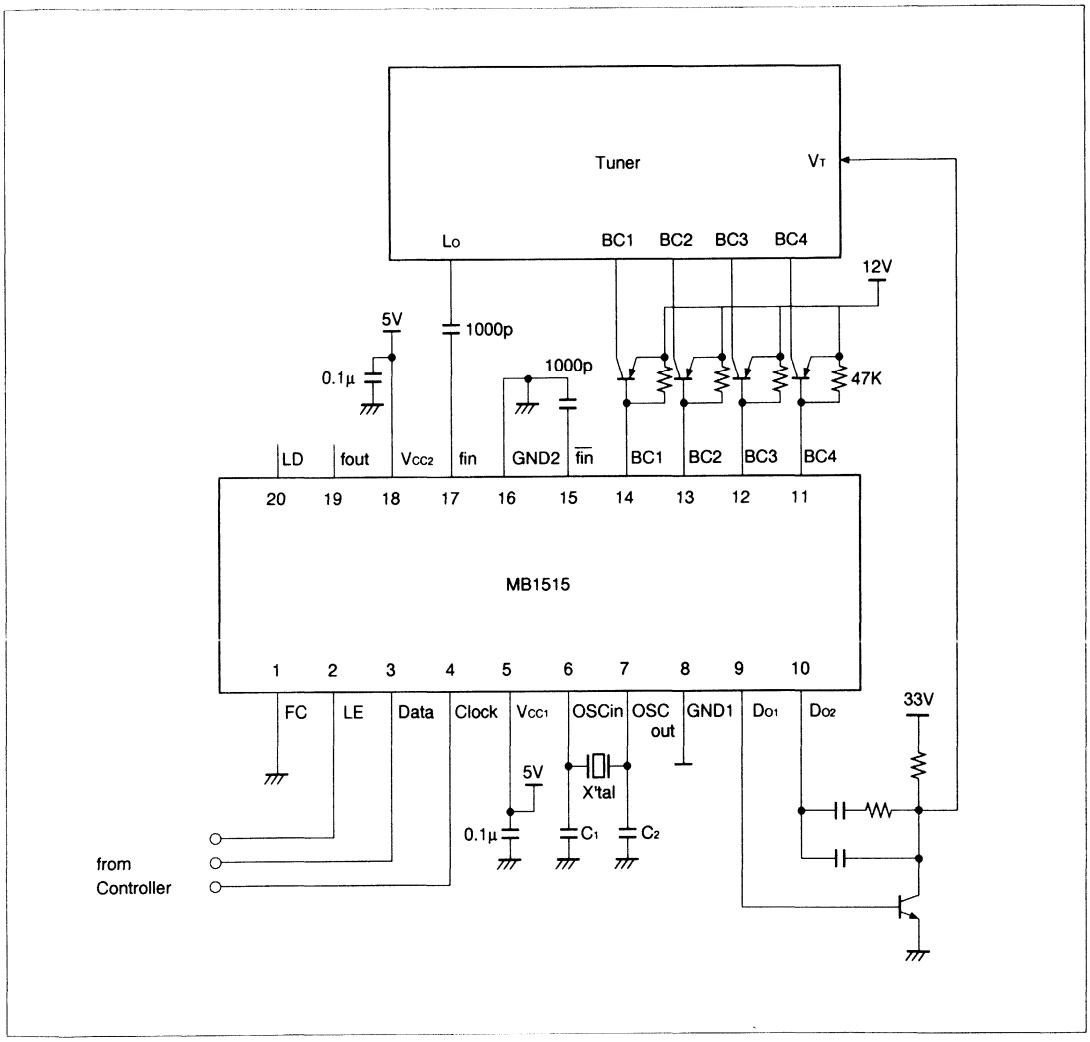
• LE, Data, clock



• LE, Data, clock



■ EXAMPLE APPLICATION



C_1, C_2: Determined by the crystal oscillator

FC: with pull up resistor

■ ORDERING INFORMATION

Parts Number	Package	Notes
MB1515PFV	Plastic SSOP, 20 pins (FPT-20P-M03)	

FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-21344-1E

ASSP
IF Band PLL Frequency Synthesizer

MB15S01

■ DESCRIPTION

The Fujitsu MB15S01 is an exclusive Intermediate Frequency (IF) band Phase Locked Loop (PLL) frequency synthesizer with pulse swallow operation. The reference divider and comparison divider have fixed divide ratios, so that it is not required to set the divide ratios by a microcontroller externally.

It operates with a supply voltage of 3.0 V typ. and dissipates 3.5 mA typ. Low power consumption is realized through the use of Fujitsu's Bi-CMOS technology.

RF synthesizer block of digital cellular phones can be realized easily as well as compactly with MB15S01 and MB1517A (2.0 GHz; SSOP-16), which is Fujitsu's standard product developed for digital cellular phones.

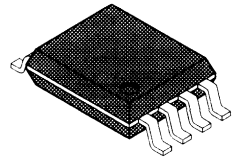
The MB15S01 is ideally suitable for PHS systems.

■ FEATURES

- Prescaler operating frequency : 300 MHz max.
- Low power supply current: I_{CC} (total) = 3.5 mA typ. (V_{CC} = 3 V)
- Pulse swallow function; Prescaler: 16/17
- Setting frequency (Selectable by Div input.)
  - fosc = 19.2 MHz, fIF = 233.15 MHz (Div = "L")
  - fosc = 19.2 MHz, fIF = 259.20 MHz (Div = "H")
- Rapid synchronization at powering up
  Fujitsu's original charge pump "supply charger circuit" is included, that enables rapid synchronization at powering up.
- Lock detector
- Low power supply voltage: V_{CC} = 2.7 to 3.6 V
- Wide operating temperature: T_a = –40 to 85°C
- Plastic 8-pin SSOP packages

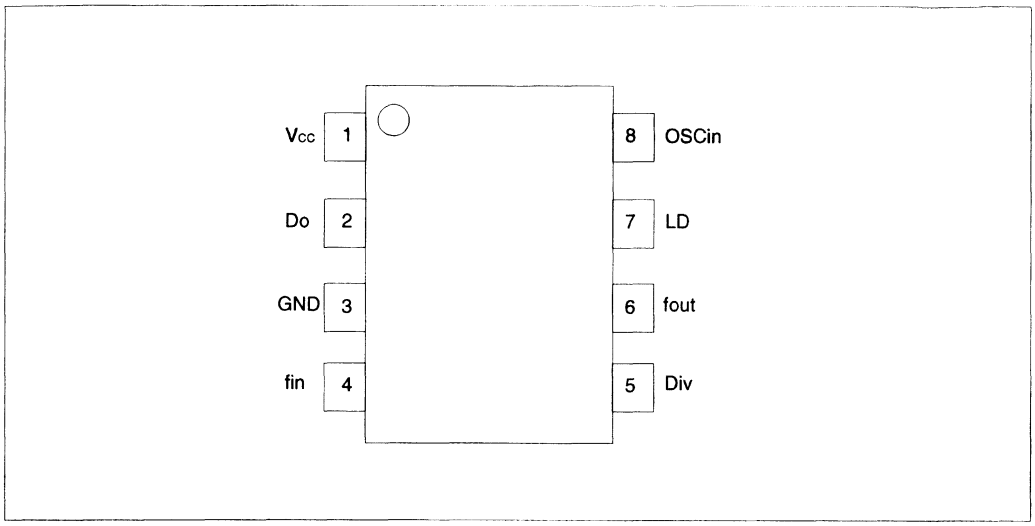
■ PACKAGE

8-pin, Plastic SSOP



(FPT-8P-M03)

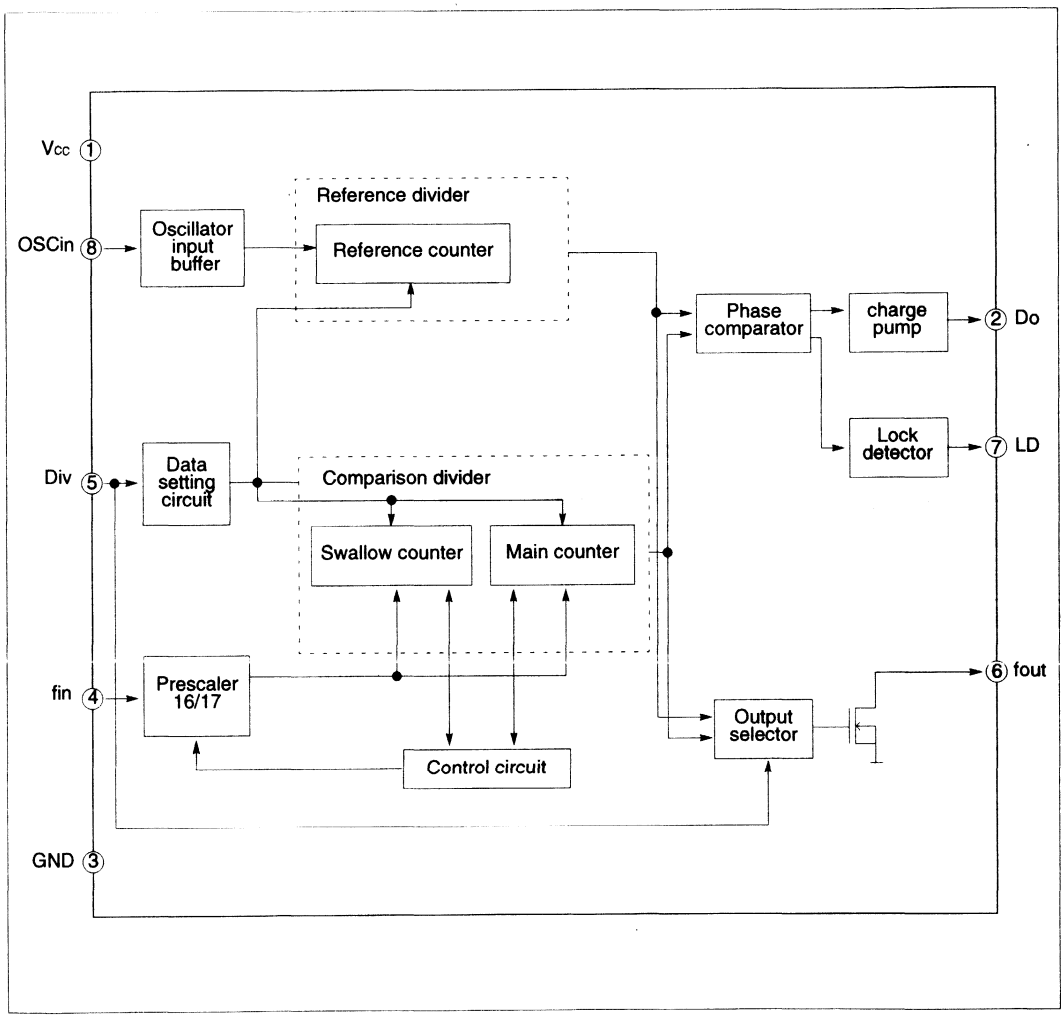
■ PIN ASSIGNMENT



■ PIN DESCRIPTIONS

Pin No.	Pin name	Descriptions
1	Vcc	Power supply voltage input (2.7 V to 3.6 V).
2	Do	Charge pump output
3	GND	Ground
4	fin	Prescaler input. Connection should be with AC coupling.
5	Div	Divide ratio switching input. Two kinds of divide ratios are selectable by Div input "H" or "L".
6	fout	Test purpose output. This pin is an open drain output so that should be left open usually.
7	LD	Lock detector output.
8	OSCin	Reference counter input. Connection should be with AC coupling.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{CC}	–0.5 to +5.0	V
Inputt voltage	V_I	–0.5 to V_{CC} +0.5	V
Output voltage	V_{OUT}	–0.5 to V_{CC} +0.5	V
Output current	I_{OUT}	0 to 5	mA
Storage temperature	T_{STG}	–55 to +125	°C

Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power supply voltage	V_{CC}	2.7	3.0	3.6	V	
Input voltage	V_{IN}	GND	–	V_{CC}	V	
Operating temperature	Ta	–40	–	+85	°C	

Handling Precautions

- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover workbenches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

■ ELECTRICAL CHARACTERISTICS

Recommended operating conditions unless otherwise noted.

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Power supply current	I_{CC}	PLL is locked. V_{CC} = 3.0 V, Ta = 25°C	–	3.5	5.0	mA
Operating frequency	fin	AC coupling by 1000 pF capacitor	10	–	270	MHz
Oscillator input frequency	fosc	AC coupling by 1000 pF capacitor	–	12	23	MHz
Input sensitivity	Vin	AC coupling by 1000 pF capacitor	–10	–	+2	dBm
Oscillator input sensivity	OSCin	AC coupling by 1000 pF capacitor	500	–	–	mVpp
Input voltage (Div)	V_{IH}		V_{CC} × 0.7	–	–	V
	V_{IL}		–	–	V_{CC} × 0.3	V
Input current (Div)	I_{IH}		–	–	1.0	µA
	I_{IL}		–1.0	–	–	µA
Input current (OSCin)	I_{OSC}		–100		100	µA
Output voltage	V_{OH}	V_{CC} = 3.0 V	2.6	–	–	V
	V_{OL}	V_{CC} = 3.0 V	–	–	0.4	V
High impedance cut off current (Do)	I_{OFF}	V_{Do} ≤ 3.6 V	–	–	1.1	µA

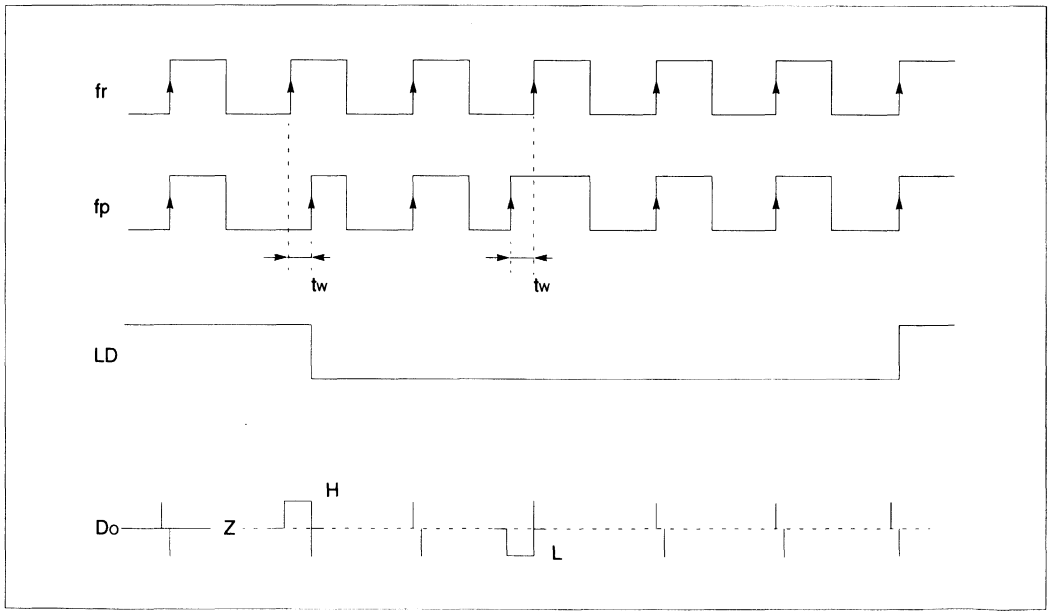
■ FUNCTIONAL DESCRIPTIONS

Two different frequencies can be selected by Div input "H" or "L".
The divide ratios are calculated using the following equation:

$f_{VCO} = \{(P \times N) + A\} \times f_{OSC} \div R \quad (A < N)$

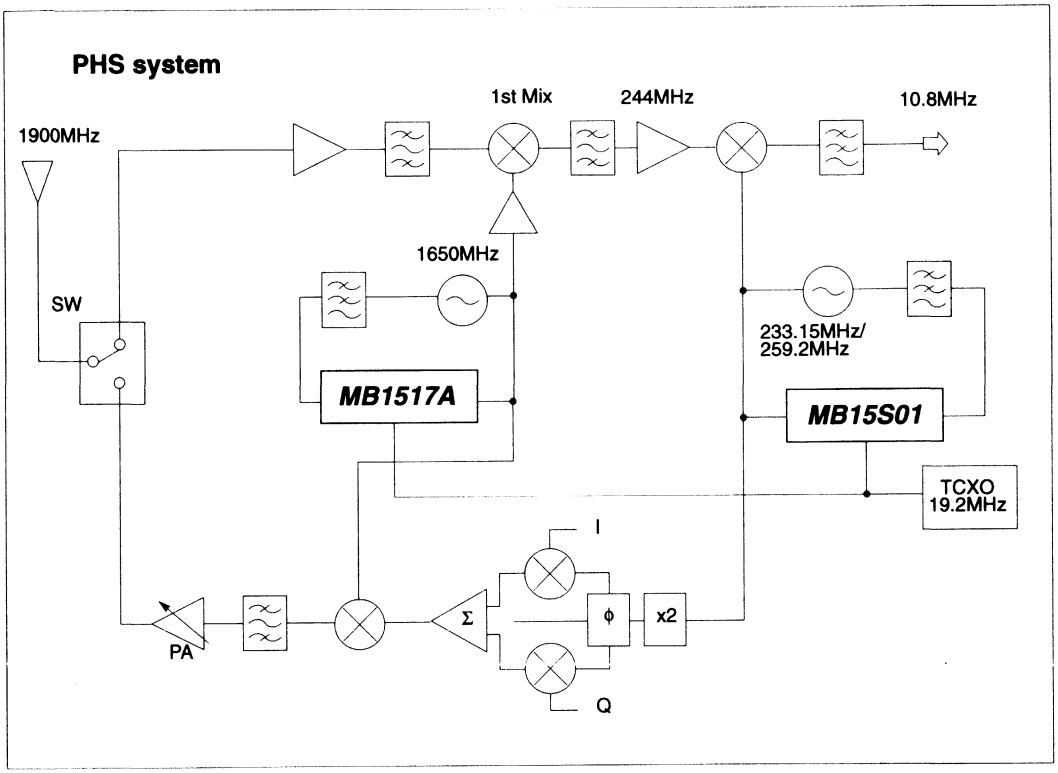
Symbol	Description	Div = "H"	Div = "L"
fvco	Output frequency of external VCO	233.15 MHz	259.20 MHz
fosc	Reference oscillation frequency	19.2 MHz	19.2 MHz
N	Divide ratio of the main counter	291	33
A	Divide ratio of the swallow counter	7	12
P	Preset divide ratio of dual modulus prescaler	16/17	16/17
R	Divide ratio of the reference counter	384 (fr = 50 kHz)	40 (fr = 480 kHz)

■ PHASE DETECTOR TIME CHART



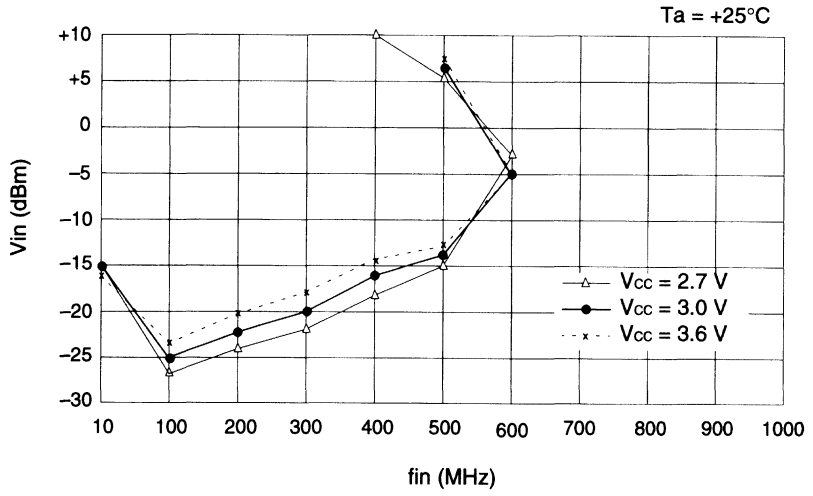
Note: • Phase defference detection range = -2π to $+ 2\pi$
- Spikes on Do pulse during locking state are output to prevent dead zone.
- LD output becomes low when phase difference is tw or more.
- LD output becomes high when phase difference is tw or less and continues to be so for three cycles or more.
- tw depends on OSCin input frequency.
(e.g. tw 625 ns to 1250 ns when foscin = 12.8 MHz)

■ APPLICATION EXAMPLE

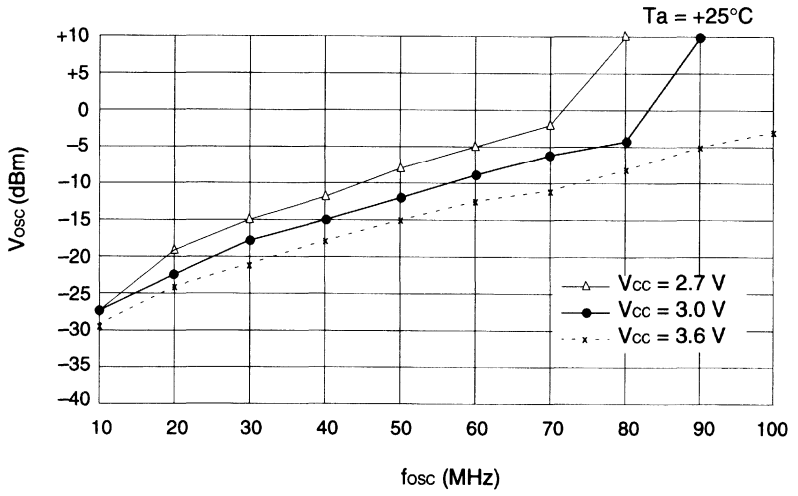


■ TYPICAL CHARACTERISTICS

Input Sensitivity (fin Pin)



Input Sensitivity (OSCin Pin)



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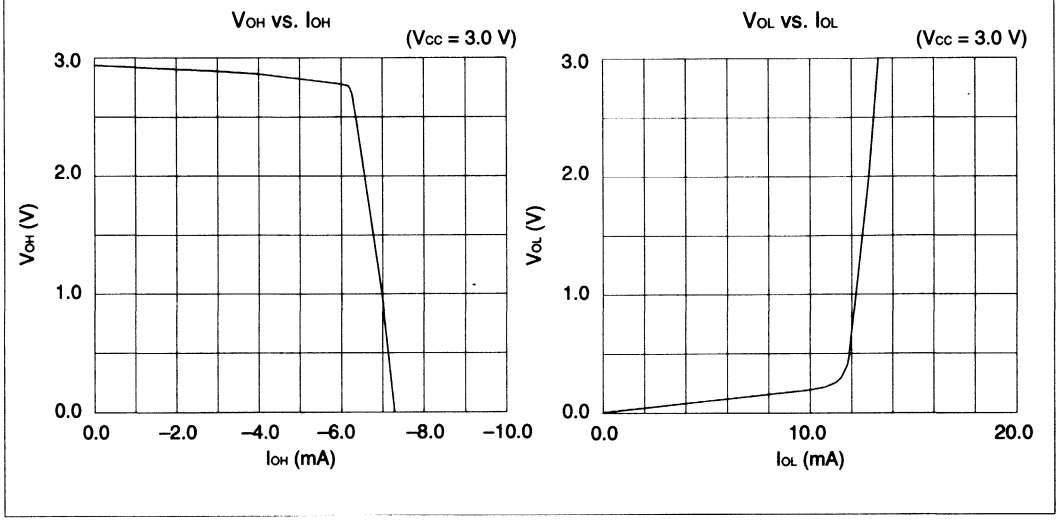
Charge Pump Current vs. Voltage (Do Pin)



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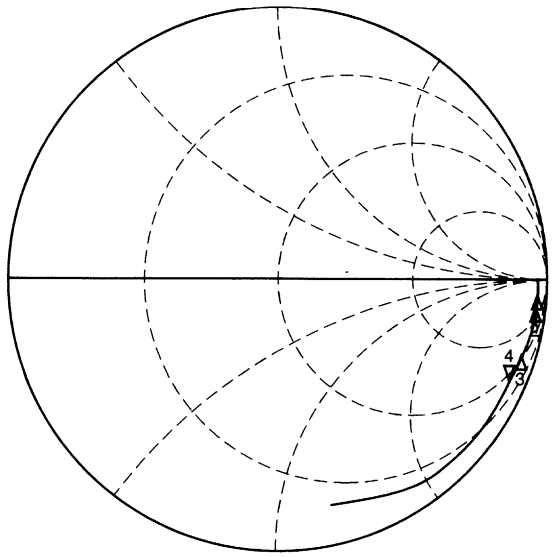
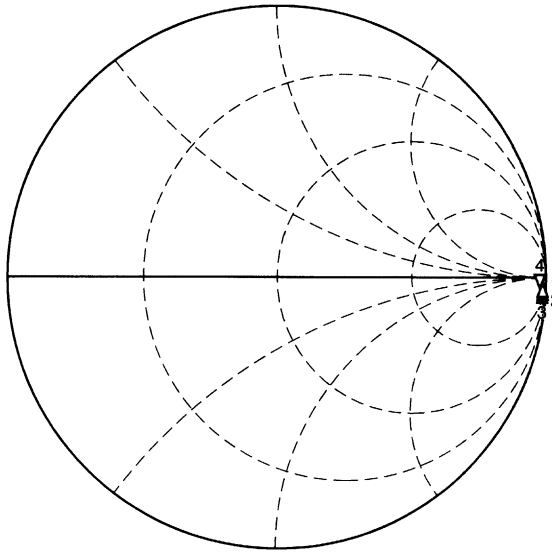
Input Impedance

fin Pin



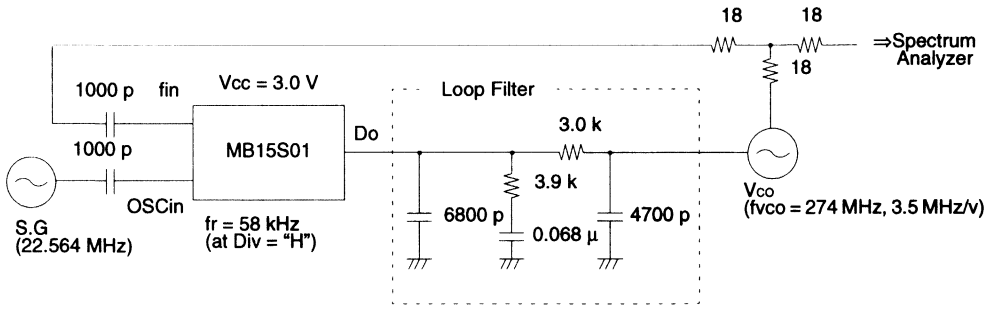
OSCin Pin



■ APPLICATION INFORMATION

• Loop Characteristics (Div = "L")

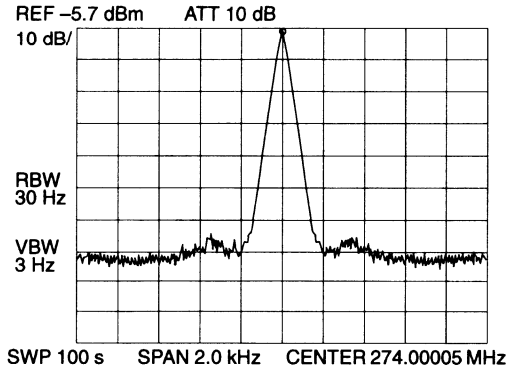
(Measurement Circuit)



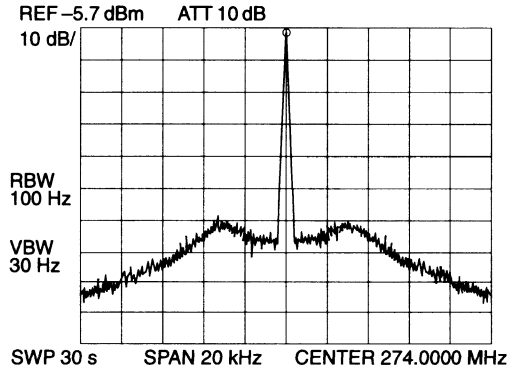
• (Measurement Results)

Parameter		Results	Unit	Note
PLL loop band width		5	kHz	f_{-3dB} at fvco
PLL phase noise	Δf = 1 kHz	86	dBc/Hz	
	Δf = 10 kHz	103		
	Δf = 100 kHz	123		
	Δf = 1 MHz	134		
PLL reference spurious		87	dBc	Δf = 58 kHz
PLL lock-up time (in ± 1 kHz)		1.8	ms	from Un-Lock to Lock

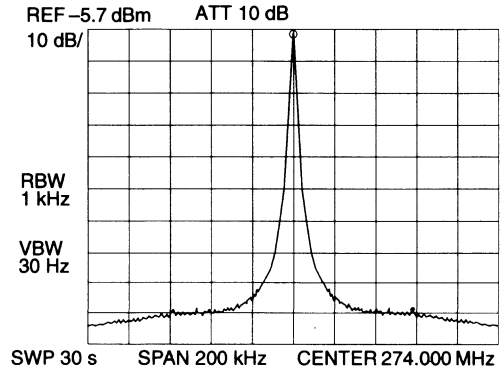
SPAN 2.0 kHz



SPAN 20 kHz



SPAN 200 kHz



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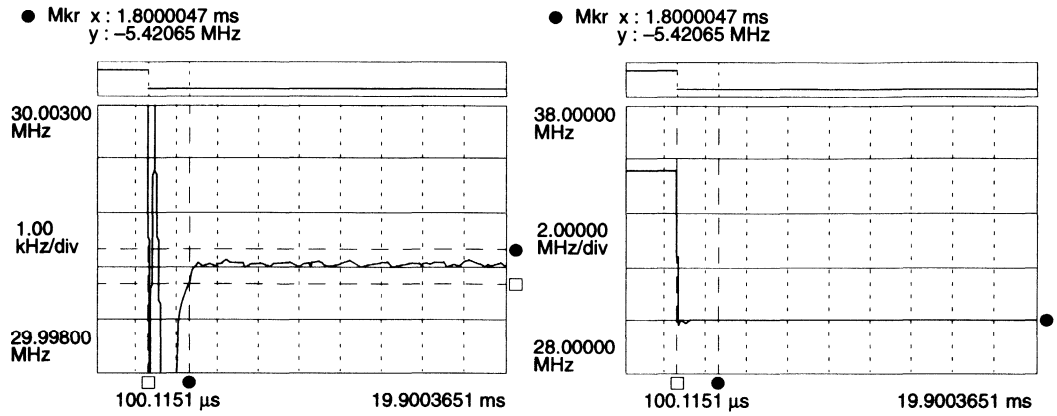
Lock-up Time (From Un-Lock to Lock)



■ ORDERING INFORMATION

Part number	Package	Remarks
MB15S01PFV	8 pin, Plastic SSOP (FPT-8P-M03)	

FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-21338-1E

ASSP
IF Band PLL Frequency Synthesizer

MB15S02

■ DESCRIPTION

The Fujitsu MB15S02 is an exclusive Intermediate Frequency (IF) band Phase Locked Loop (PLL) frequency synthesizer with pulse swallow operation. The reference divider and comparison divider have fixed divide ratios, so that it is not required to set the divide ratios by a microcontroller externally.

It operates with a supply voltage of 3.0V typ. and dissipates 3.5 mA typ. of current realized through the use of Fujitsu's Bi-CMOS technology.

RF synthesizer block of digital cellular phones can be realized easily as well as compactly with MB15S02 and MB15A16 (1.2 GHz; SSOP-16), which is Fujitsu's standard product developped for digital cellular phones.

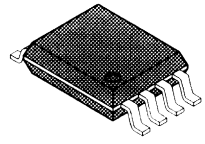
The MB15S02 is ideally suitable for GSM systems.

■ FEATURES

- Prescaler operating frequency : 300MHz max.
- Low power supply current: I_{CC} (total) = 3.5 mA typ. (V_{CC} = 3V)
- Pulse swallow function; Prescaler: 16/17
- Setting frequency (Selectable by Div input.)
  – fosc = 13.0MHz, fIF = 284.0MHz (Div = "H")
  – fosc = 13.0MHz, fIF = 116.0MHz (Div = "L")
- Rapid synchronization at powering up
  Fujitsu's original charge pump "super charger circuit" is included, that enables rapid synchronization at powering up.
- Lock detector
- Low power supply voltage: V_{CC} = 2.7 to 3.6V
- Wide operating temperature: T_a = –40 to 85°C
- Plastic 8-pin SSOP packages

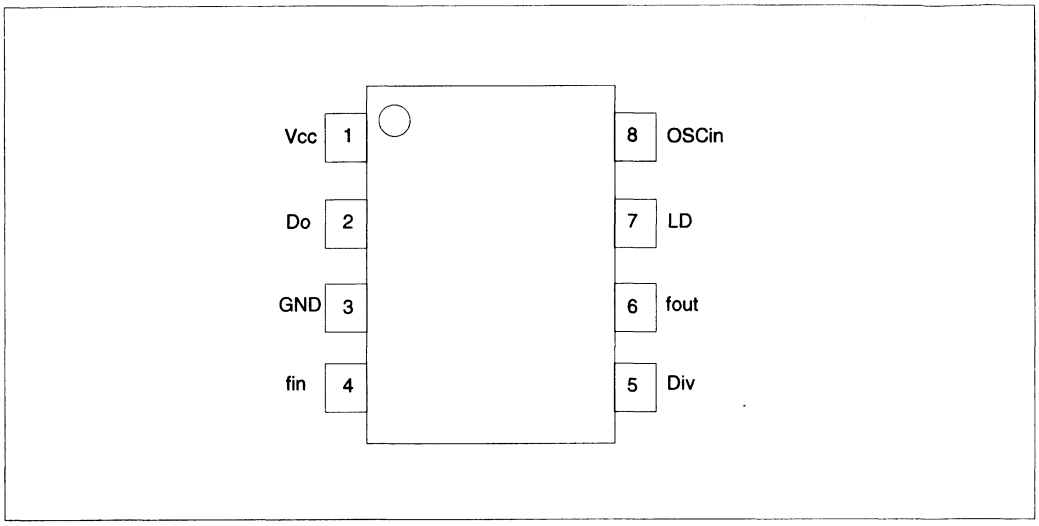
■ PACKAGE

8-pin, Plastic SSOP



(FPT-8P-M03)

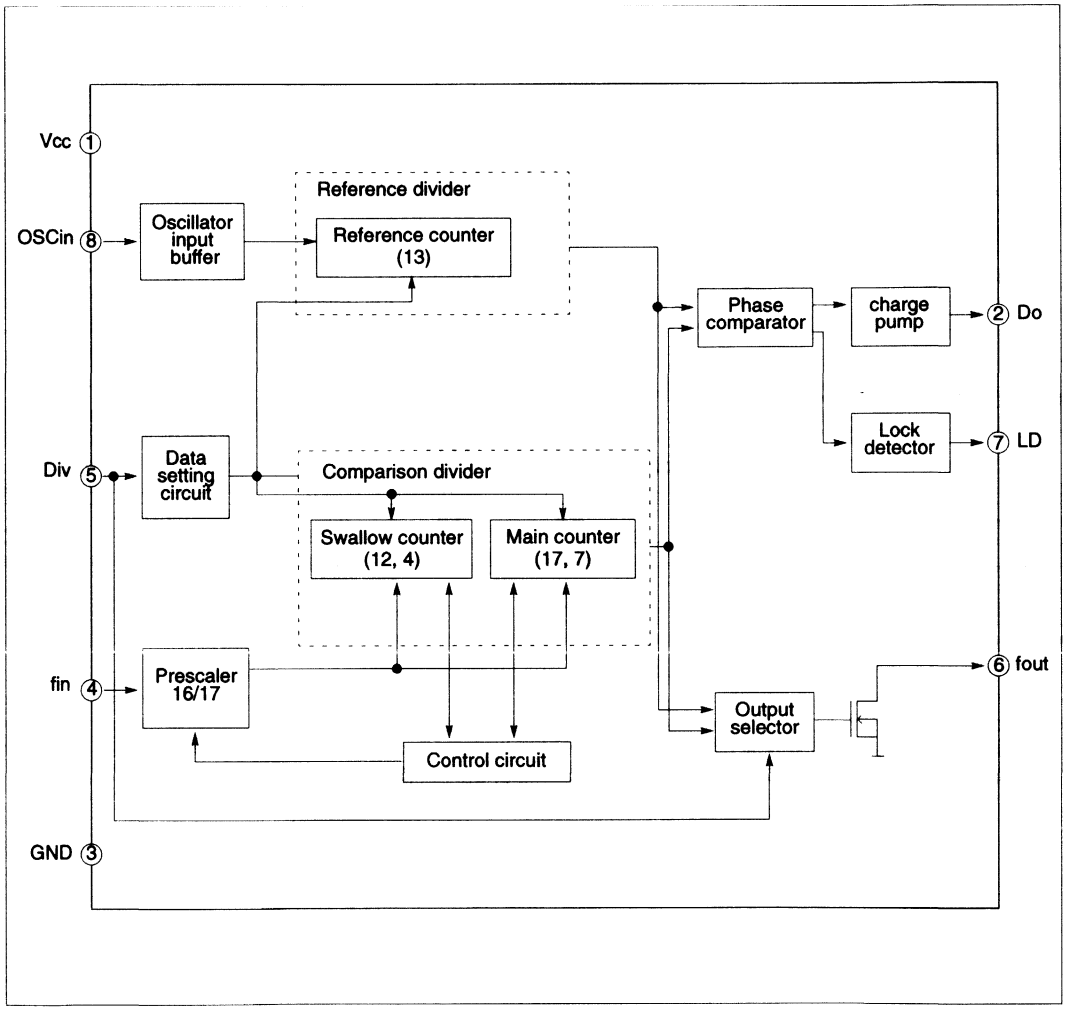
■ PIN ASSIGNMENT



■ PIN DESCRIPTIONS

Pin No.	Pin name	Descriptions
1	V_{CC}	Power supply voltage input (2.7V to 3.6V).
2	D_O	Charge pump output
3	GND	Ground
4	fin	Prescaler input. Connection should be with AC coupling.
5	Div	Divide ratio switching input. Two kinds of divide ratios are selectable by Div input "H" or "L".
6	fout	Test purpose output. This pin is an open drain output so that should be left open usually.
7	LD	Lock detector output.
8	OSCin	Reference counter input. Connection should be with AC coupling.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{CC}	–0.5 to +5.0	V
Inputt voltage	V_I	–0.5 to V_{CC} +0.5	V
Output voltage	V_{OUT}	–0.5 to V_{CC} +0.5	V
Output current	I_{OUT}	0 to 5	mA
Storage temperature	T_{STG}	–55 to +125	°C

Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Note
		Min	Typ	Max		
Power supply voltage	V_{CC}	2.7	3.0	3.6	V	
Input voltage	V_{IN}	GND	–	V_{CC}	V	
Operating temperature	Ta	–40	–	+85	°C	

Handling Precautions

- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover workbenches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

■ ELECTRICAL CHARACTERISTICS

Recommended operating conditions unless otherwise noted.

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Power supply current	I_{CC}	PLL is locked. Vcc = 3.0V, Ta = 25°C	–	3.5	5.0	mA
Operating frequency	fin	AC coupling by 1000pF capacitor	80	–	300	MHz
Oscillator input frequency	fosc	AC coupling by 1000pF capacitor	–	13	23	MHz
Input sensitivity	Vin	AC coupling by 1000pF capacitor	–10	–	+2	dBm
Oscillator input sensivity	OSCin	AC coupling by 1000pF capacitor	500	–	–	mVp p
Input voltage (Div)	V_{IH}		$V_{CC} \times 0.7$	–	–	V
	V_{IL}		–	–	$V_{CC} \times 0.3$	V
Input current (Div)	I_{IH}		–	–	1.0	µA
	I_{IL}		–1.0	–	–	µA
Input current (OSCin)	I_{OSC}		–100		100	µA
Output voltage	V_{OH}	V_{CC} = 3.0V	2.6	–	–	V
	V_{OL}	V_{CC} = 3.0V	–	–	0.4	V
High impedance cut off current (Do)	I_{OFF}	$VD_O \leq 3.6V$	–	–	1.1	µA

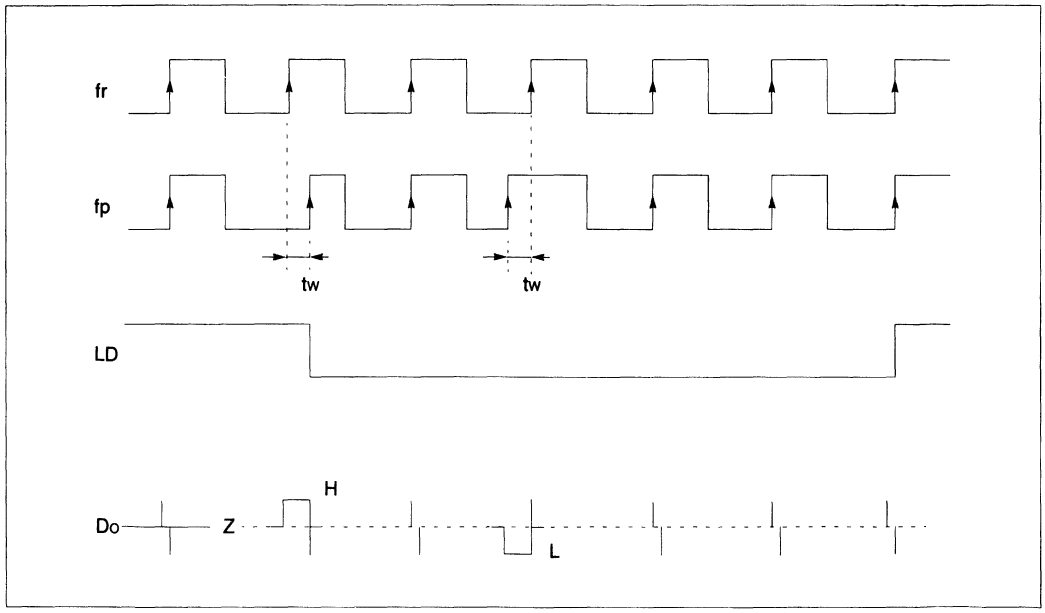
■ FUNCTIONAL DESCRIPTIONS

Two different frequencies can be selected by Div input "H" or "L".
The divide ratios are calculated using the following equation:

$f_{VCO} = \{(P \times N) + A\} \times f_{OSC} \div R \quad (A < N)$

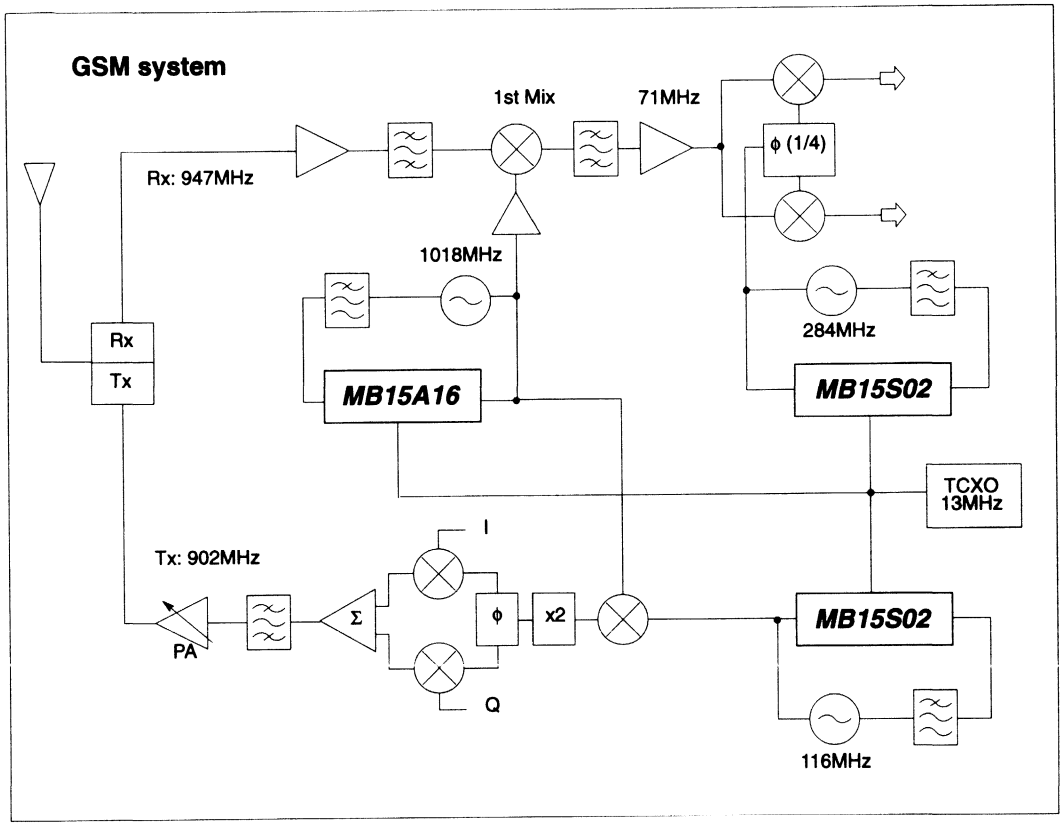
Symbol	Description	Div = "H"	Div = "L"
fvco	Output frequency of external VCO	284.0 MHz	116.00 MHz
fosc	Reference oscillation frequency	13.0 MHz	13.0 MHz
N	Divide ratio of the main counter	17	7
A	Divide ratio of the swallow counter	12	4
P	Preset divide ratio of dual modulus prescaler	16/17	16/17
R	Divide ratio of the reference counter	13 (fr = 1 MHz)	13 (fr = 1 MHz)

■ PHASE DETECTOR TIME CHART



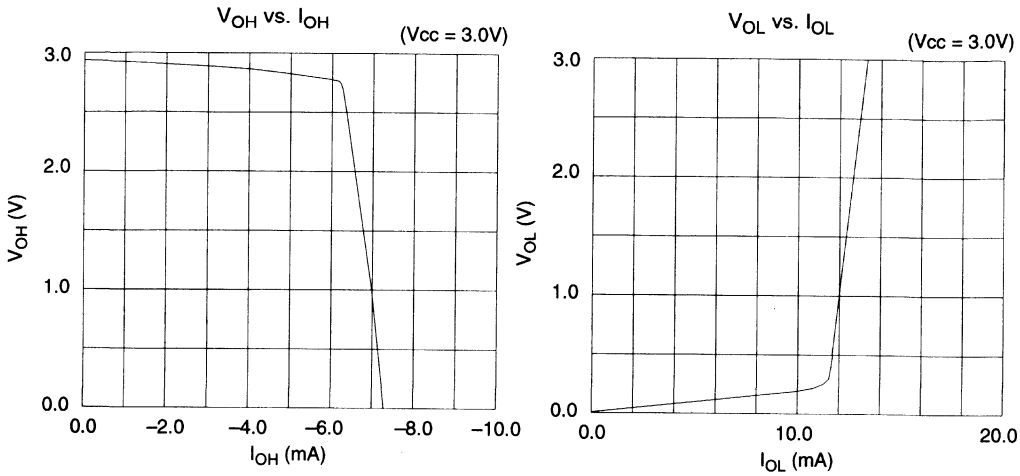
Note: • Phase defference detection range = -2π to $+ 2\pi$
- Spikes on Do pulse during locking state are output to prevent dead zone.
- LD output becomes low when phase difference is tw or more.
- LD output becomes high when phase difference is tw or less and continues to be so for three cycles or more.
- tw depends on OSCin input frequency.
  (e.g. tW635ns to 1250ns when foscin = 12.8 MHz)

■ APPLICATION EXAMPLE



■ TYPICAL CHARACTERISTICS

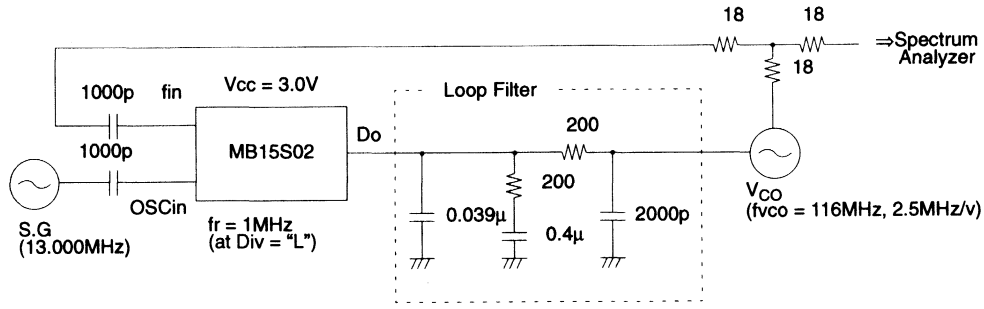
Charge Pump Current vs. Voltage (Do Pin)



■ APPLICATION INFORMATION

• Loop Characteristics (Div = "L")

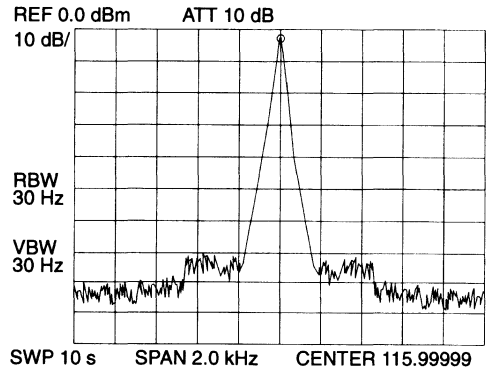
(Measurement Circuit)



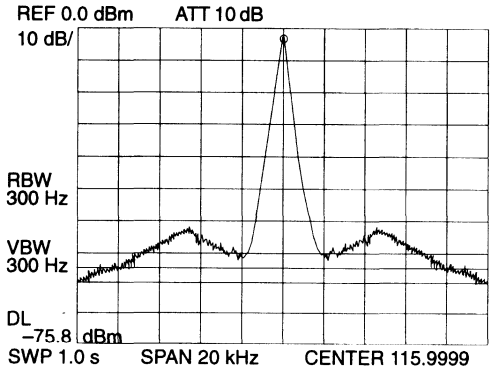
• (Measurement Results)

Parameter		Results	Unit	Note
PLL loop band width		8	kHz	f_{-3dB} at fvco
PLL phase noise	Δf = 1kHz	96	dBc/Hz	
	Δf = 10kHz	102		
PLL reference spurious		86	dBc	Δf = 1MHz
PLL lock-up time (in ± 1kHz)		3.7	ms	from Vcc OFF to Vcc ON

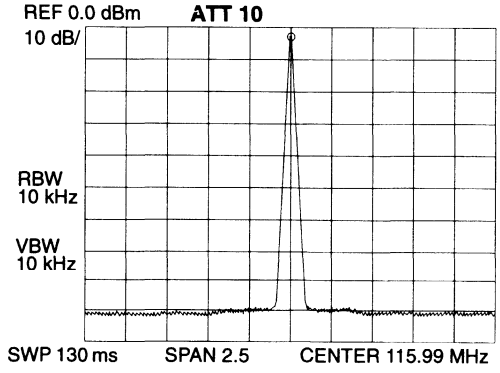
SPAN 2.0 kHz



SPAN 20



SPAN 2.5 MHz



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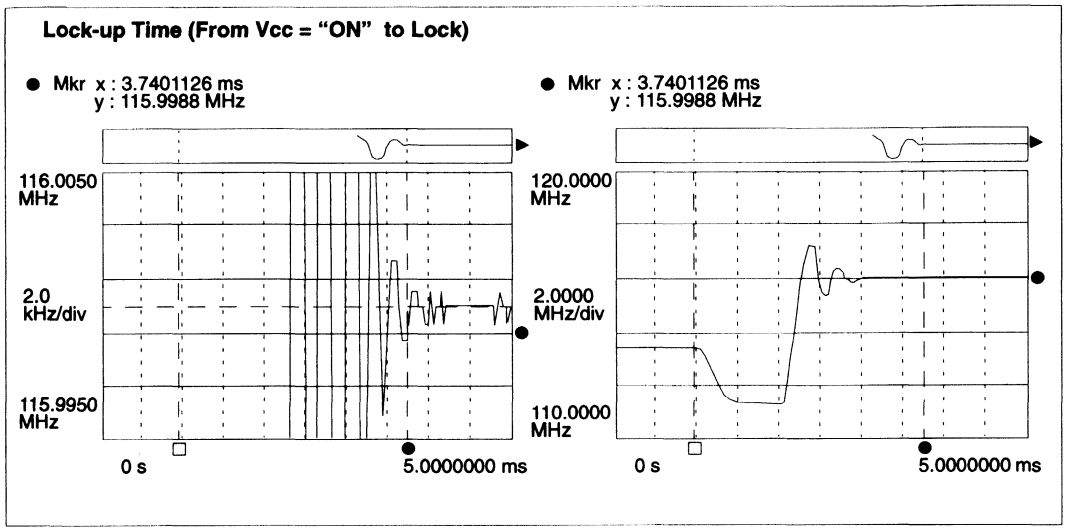
Lock-up Time (From Vcc = "ON" to Lock)



■ ORDERING INFORMATION

Part number	Package	Remarks
MB15S02PFV	8 pin, Plastic SSOP (FPT-8P-M03)	

FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-21345-1E

ASSP
IF Band PLL Frequency Synthesizer

MB15S03

■ DESCRIPTION

The Fujitsu MB15S03 is an exclusive Intermediate Frequency (IF) band Phase Locked Loop (PLL) frequency synthesizer with pulse swallow operation. The reference divider and comparison divider have fixed divide ratios, so that it is not required to set the divide ratios by a microcontroller externally.

It operates with a supply voltage of 3.0 V typ. and dissipates 3.5 mA typ. of current realized through the use of Fujitsu's Bi-CMOS technology.

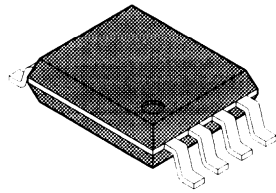
The MB15S03 is ideally suitable for PDC systems.

■ FEATURES

- Prescaler operating frequency : 200 MHz max.
- Low power supply current: I_{CC} (total) = 3.5 mA typ. (V_{CC} = 3 V)
- Pulse swallow function; Prescaler: 16/17
- Setting frequency (Selectable by Div input.)
  – fosc = 12.8 MHz, fIF = 178.00 MHz (Div = "H")
  – fosc = 12.8 MHz, fIF = 129.55 MHz (Div = "L")
- Rapid synchronization at powering up
  Fujitsu's original charge pump "super charger circuit" is included, that enables rapid synchronization at powering up.
- Lock detector
- Low power supply voltage: Vcc = 2.7 to 3.6 V
- Wide operating temperature: Ta = −40 to 85°C
- Plastic 8-pin SSOP package

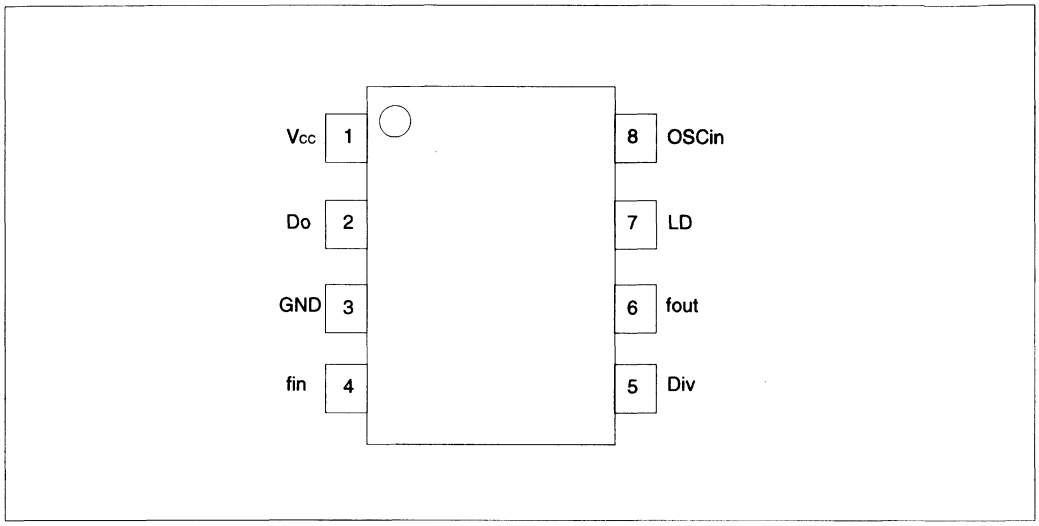
■ PACKAGE

8-pin, Plastic SSOP



(FPT-8P-M03)

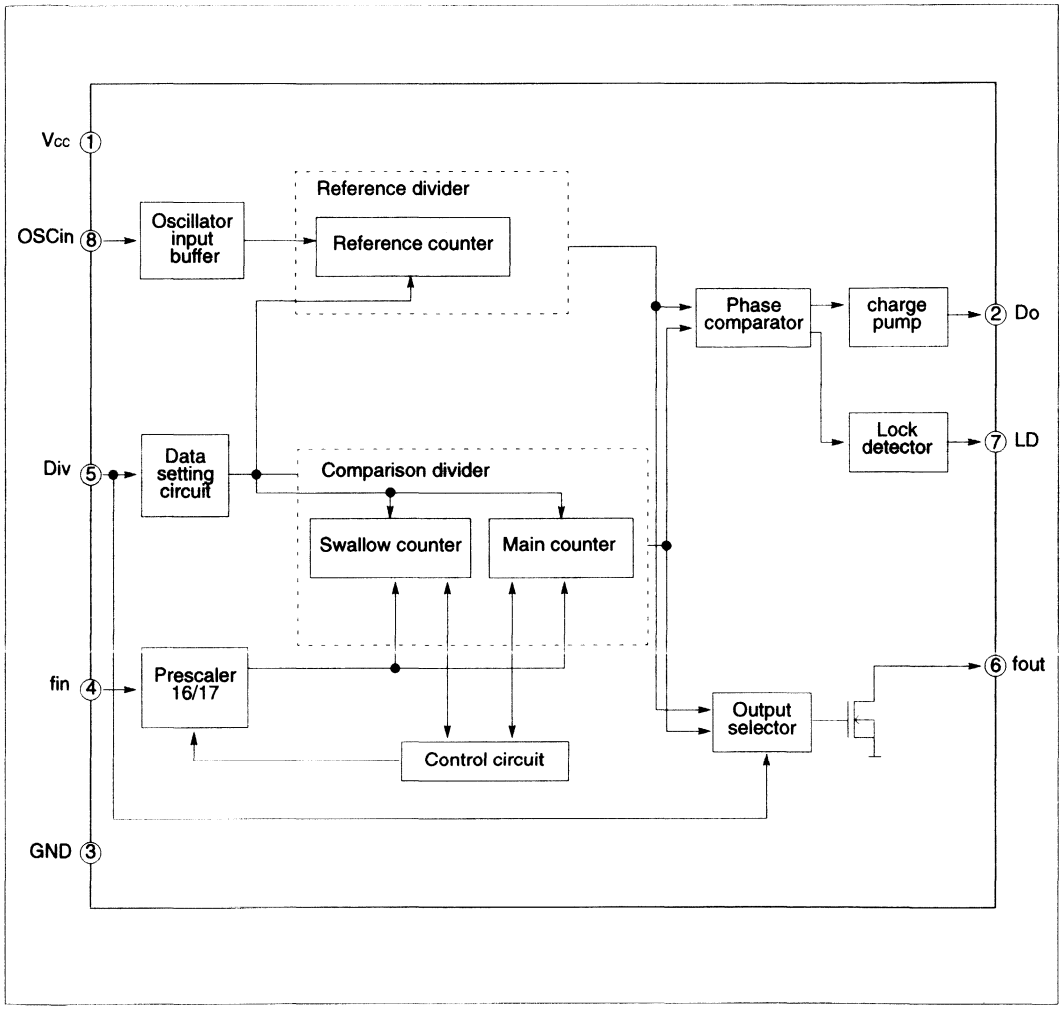
■ PIN ASSIGNMENT



■ PIN DESCRIPTIONS

Pin No.	Pin name	Descriptions
1	Vcc	Power supply voltage input (2.7 V to 3.6 V).
2	Do	Charge pump output
3	GND	Ground
4	fin	Prescaler input. Connection should be with AC coupling.
5	Div	Divide ratio switching input. Two kinds of divide ratios are selectable by Div input "H" or "L".
6	fout	Test purpose output. This pin is an open drain output so that should be left open usually.
7	LD	Lock detector output.
8	OSCin	Reference counter input. Connection should be with AC coupling.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{CC}	–0.5 to +5.0	V
Inputt voltage	V_I	–0.5 to V_{CC} +0.5	V
Output voltage	V_{OUT}	–0.5 to V_{CC} +0.5	V
Output current	I_{OUT}	0 to 5	mA
Storage temperature	T_{STG}	–55 to +125	°C

Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power supply voltage	V_{CC}	2.7	3.0	3.6	V	
Input voltage	V_{IN}	GND	–	V_{CC}	V	
Operating temperature	Ta	–40	–	+85	°C	

Handling Precautions

- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover workbenches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

■ ELECTRICAL CHARACTERISTICS

Recommended operating conditions unless otherwise noted.

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Power supply current	I_{CC}	PLL is locked. V_{CC} = 3.0 V, Ta = 25°C	–	3.5	5.0	mA
Operating frequency	fin	AC coupling by 1000 pF capacitor	100	–	200	MHz
Oscillator input frequency	fosc	AC coupling by 1000 pF capacitor	–	12	23	MHz
Input sensitivity	Vin	AC coupling by 1000 pF capacitor	–10	–	+2	dBm
Oscillator input sensivity	OSCin	AC coupling by 1000 pF capacitor	500	–	–	mVpp
Input voltage (Div)	V_{IH}		$V_{CC} \times 0.7$	–	–	V
	V_{IL}		–	–	$V_{CC} \times 0.3$	V
Input current (Div)	I_{IH}		–	–	1.0	µA
	I_{IL}		–1.0	–	–	µA
Input current (OSCin)	I_{OSC}		–100		100	µA
Output voltage	V_{OH}	V_{CC} = 3.0 V	2.6	–	–	V
	V_{OL}	V_{CC} = 3.0 V	–	–	0.4	V
High impedance cut off current (Do)	I_{OFF}	$V_{DO} \leq$ 3.6 V	–	–	1.1	µA

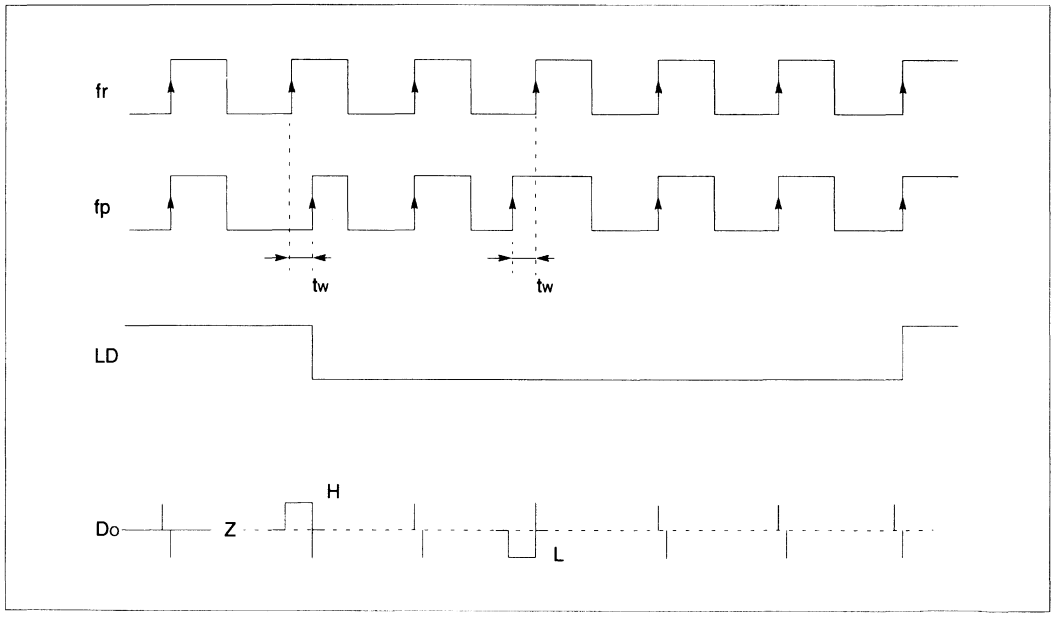
■ FUNCTIONAL DESCRIPTIONS

Two different frequencies can be selected by Div input "H" or "L".
The divide ratios are calculated using the following equation:

$f_{VCO} = \{(P \times N) + A\} \times f_{OSC} \div R \quad (A < N)$

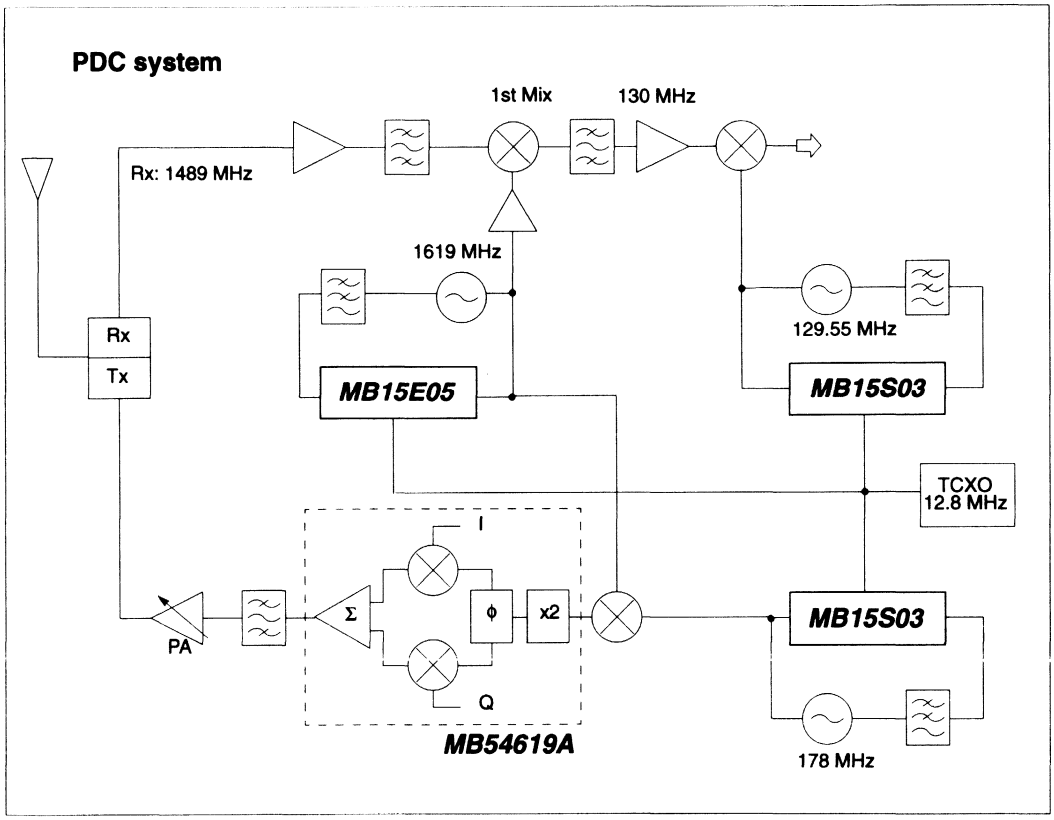
Symbol	Description	Div = "H"	Div = "L"
fvco	Output frequency of external VCO	178.0 MHz	129.55 MHz
fosc	Reference oscillation frequency	12.8 MHz	12.8 MHz
N	Divide ratio of the main counter	27	161
A	Divide ratio of the swallow counter	13	15
P	Preset divide ratio of dual modulus prescaler	16/17	16/17
R	Divide ratio of the reference counter	32 (fr = 400 kHz)	256 (fr = 50 kHz)

■ PHASE DETECTOR TIME CHART



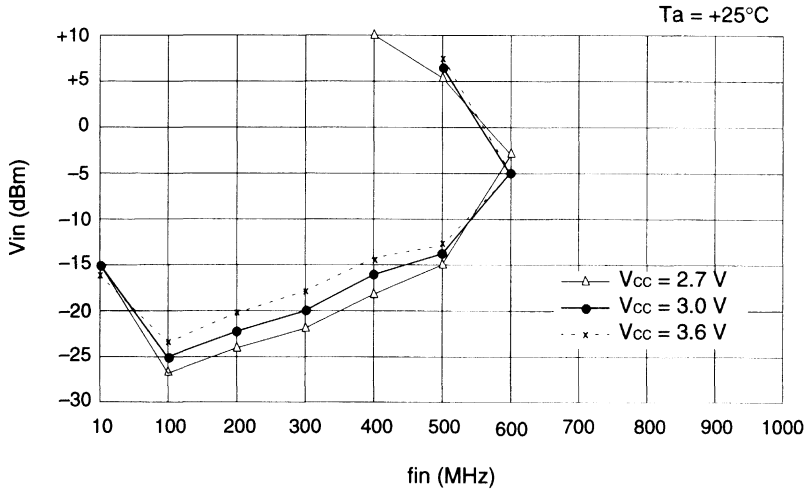
Note: • Phase defference detection range = -2π to $+2\pi$
- Spikes on Do pulse during locking state are output to prevent dead zone.
- LD output becomes low when phase difference is tw or more.
- LD output becomes high when phase difference is tw or less and continues to be so for three cycles or more.
- tw depends on OSCin input frequency.
  (e.g. tw 625 ns to 1250 ns when foscin = 12.8 MHz)

■ APPLICATION EXAMPLE

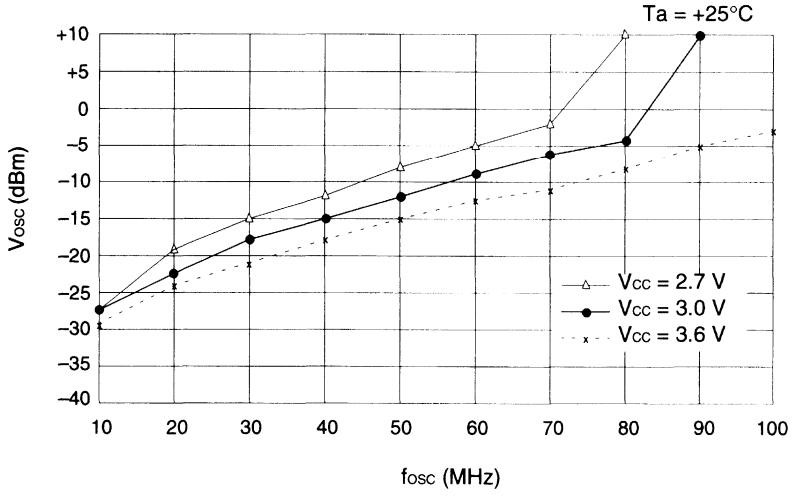


■ TYPICAL CHARACTERISTICS

Input Sensitivity (fin Pin)



Input Sensitivity (OSCin Pin)



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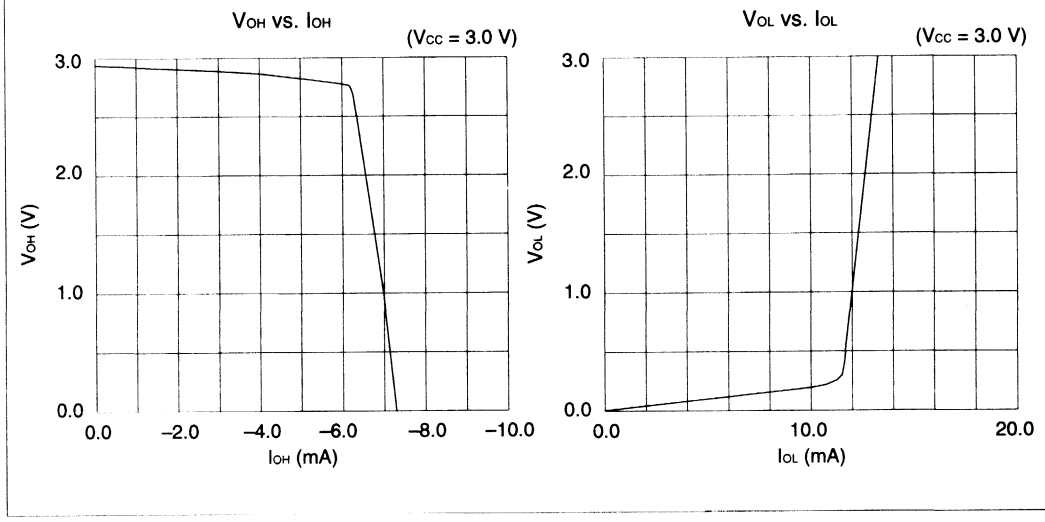
Charge Pump Current vs. Voltage (Do Pin)



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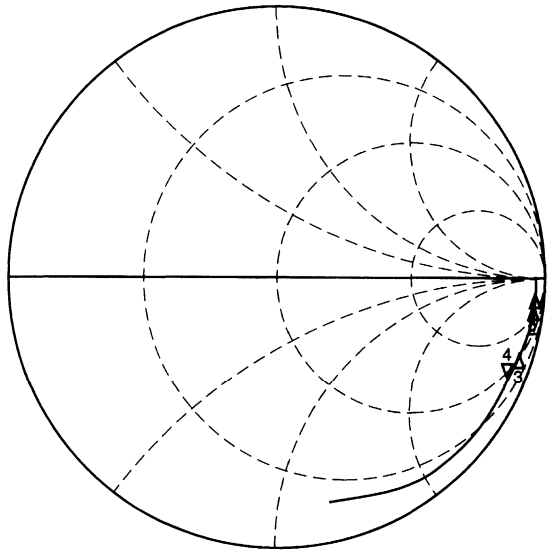
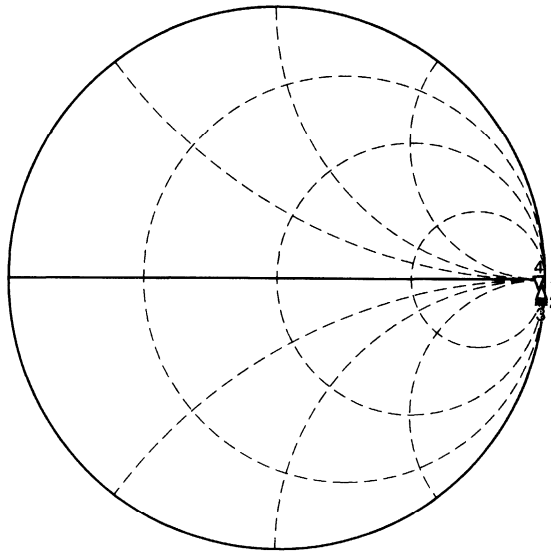
Input Impedance

fin Pin



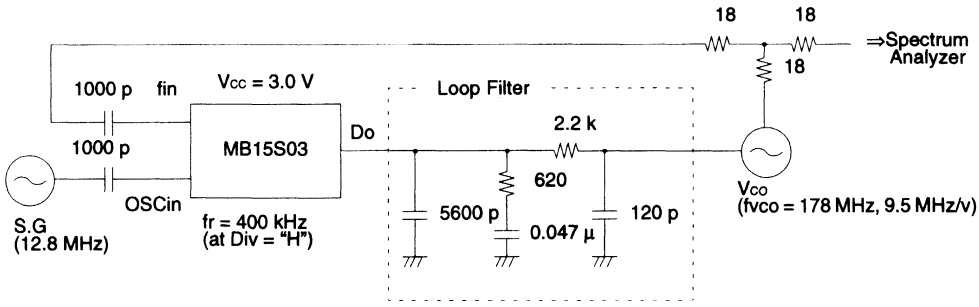
OSCin Pin



■ APPLICATION INFORMATION

• Loop Characteristics (Div = "L")

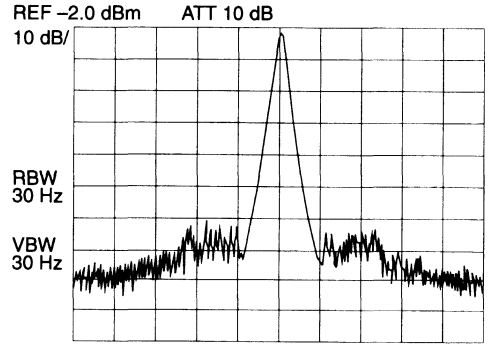
(Measurement Circuit)



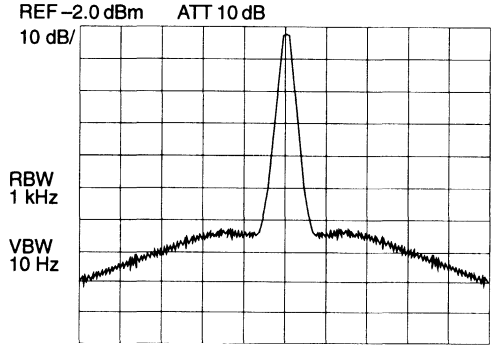
• (Measurement Results)

Parameter		Results	Unit	Note
PLL loop band width		24	kHz	f_{-3dB} at fvco
PLL phase noise	Δf = 1 kHz	95.1	dBc/Hz	f_{OSC} = 12.8 MHz f_{VCO} = 178 MHz
	Δf = 10 kHz	89.3		
	Δf = 1 MHz	132		
PLL reference spurious		80.4	dBc	Δf = 400 kHz
PLL lock-up time	(fin ±1 kHz)	195	µs	from Un-Lock to Lock
		1.0	ms	from V_{CC} OFF to V_{CC} ON

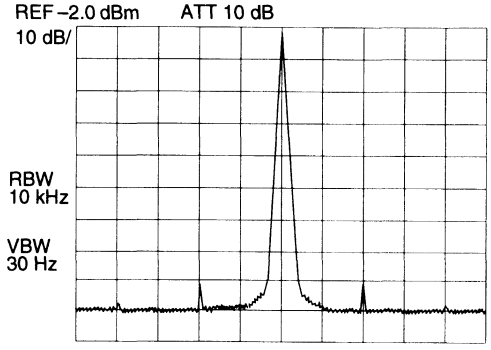
SPAN 2.0 kHz



SPAN 100 kHz



SPAN 2.0 MHz



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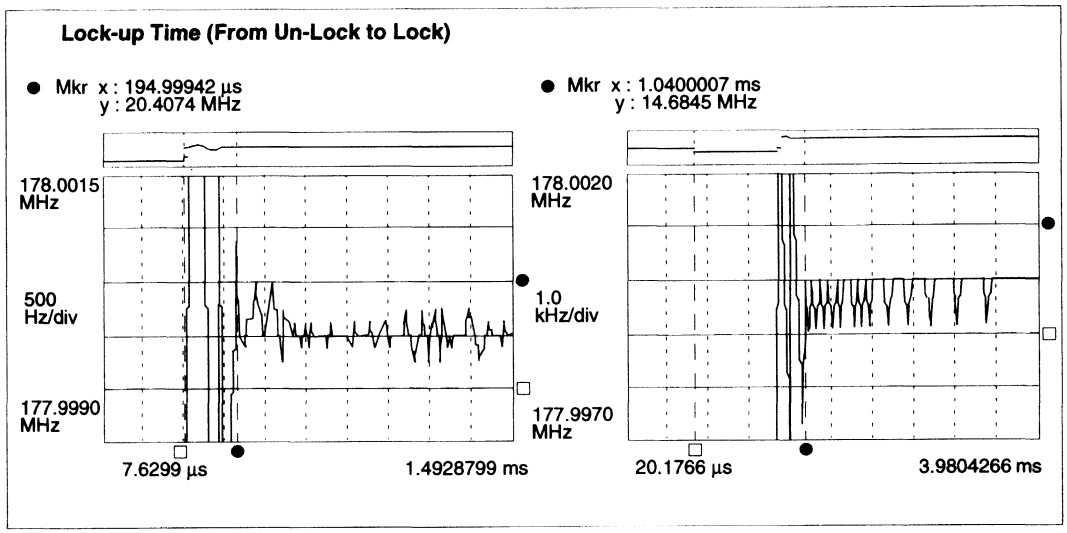
Lock-up Time (From Un-Lock to Lock)



■ ORDERING INFORMATION

Part number	Package	Remarks
MB15S03PFV	8 pin, Plastic SSOP (FPT-8P-M03)	

FUJITSU SEMICONDUCTOR
DATA SHEET

DS06-70101-3E

Semicustom

ASTRO MASTER Specification

MB1520/MB1530/MB1540/MB1550 Series

ADVANCED SEMICUSTOM TECHNOLOGY OF SUPER PLL WITH RF SYSTEM ON LSI

DESCRIPTION

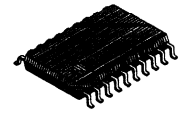
The Fujitsu ASTRO MASTER MB1520/1530/1540/1550 series are semicustom LSI IC's based on a master slice method. Super PLL (PLL and Prescaler) macros and high frequency analog macros, such as VCO's, IF amplifiers, RF amplifiers, and mixers can be realized on a single chip in accordance with customer requests. This is achieved by means of predefined blocks (Super PLL's and analog macros) laid out on the respective frames in a number of different combinations. The performance of each block is custom specified.
The ASTRO MASTER makes it possible to compose single chip silicon front ends for mobile communication systems. Due to the design process is used, development cycles and costs are greatly reduced over standard full custom LSI designs, resulting in lower system cost solutions and reduced time-to-market.

FEATURES

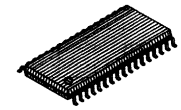
- Super PLL's as well as high frequency analog circuits, such as VCO's, mixers, RF and IF amplifiers.
- Four available frame sizes, offering various combinations of Super PLL's and analog macros.
- Choice of a wide variety of exsisting Super PLL's and analog functions, as well as custom specifications of the same.
- Choice of power supply voltages between 2.7V and 5.5V. (Minimum 2.0V with some restrictions available.)
- Available high speed lock up circuit for digital mobile communications such as DECT, GSM, PDC, and so on.
- A number of standard features, such as power saving modes, phase shifter circuit, analog switches, charge pumps, depending on the frame size.
- Development cycle is typical 14 weeks.

APPLICATION EXAMPLES

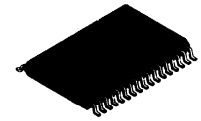
- MB1520 series : BS tuner, car navigation systems
- MB1530 series : MCA wireless for business use, analog cordless phones
- MB1540 series : Analog cellular phones, trunked radios
- MB1550 series : Digital cellular and digital cordless phones



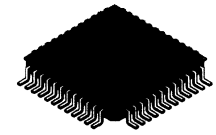
FPT-20P-M03



FPT-34P-M01

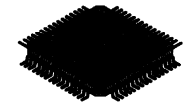


FPT-34P-M03



FPT-48P-M04

FPT-48P-M05



FPT-64P-M03

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ASTRO MASTER SERIES

ASTRO MASTER series are based on a master–slice method that features predefined blocks which are floor planned. Four series, MB1520/1530/1540/1550 are available depending on the combinations of the predefined blocks. (Please refer to "Chip Layout".) Table 1 shows representative blocks and features of each series.
Master–slice methodology means that wafers of a particular frame are prefabricated as much as a finished diffusion processes, forming the basic elements, such as transistors, resistors and capacitors. The remaining contact and wiring process steps than determine and configure the function and value of each element according to customer needs.

Table1. ASTRO MASTER Series

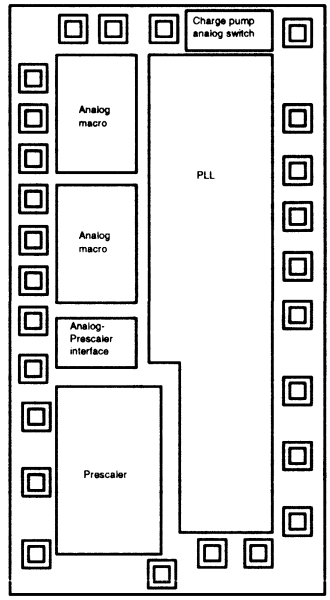
Series Name	Prescaler	PLL	Analog macro	Operating frequency (max.)	Package		
					SSOP	QFP	SQFP
MB1520	1 circuit	1 circuit	2 circuits	2.4GHz	20-pin	–	–
MB1530	2 circuits	2 circuits	4 circuits	1.9GHz	34-pin**	–	–
MB1540	2 circuits	2 circuits	6 circuits	2.4GHz	–	48-pin	48-pin
MB1550	3 circuits*	3 circuits	8 circuits	2.4GHz	–	48-pin	64-pin

*: 1 Prescaler or 90° phase shifter
**: Two packages are available.

CHIP LAYOUT

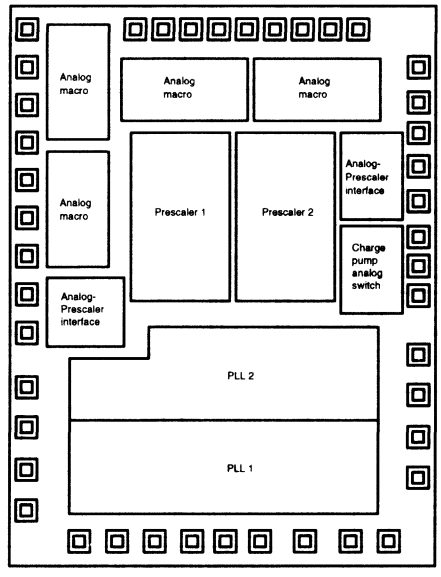
MB1520 Series

1 Prescaler
1 PLL
2 Analog Macros



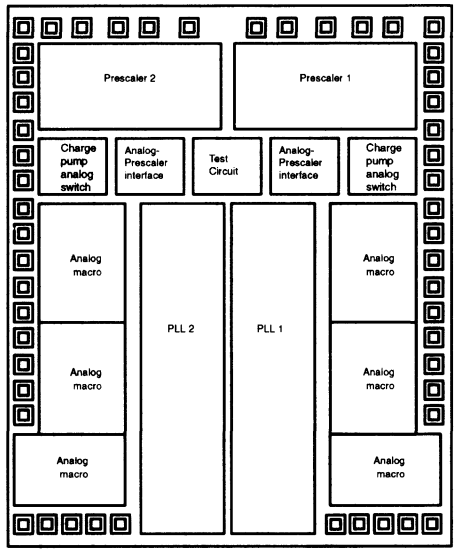
MB 1530 Series

2 Prescalers
2 PLL's
4 Analog Macros



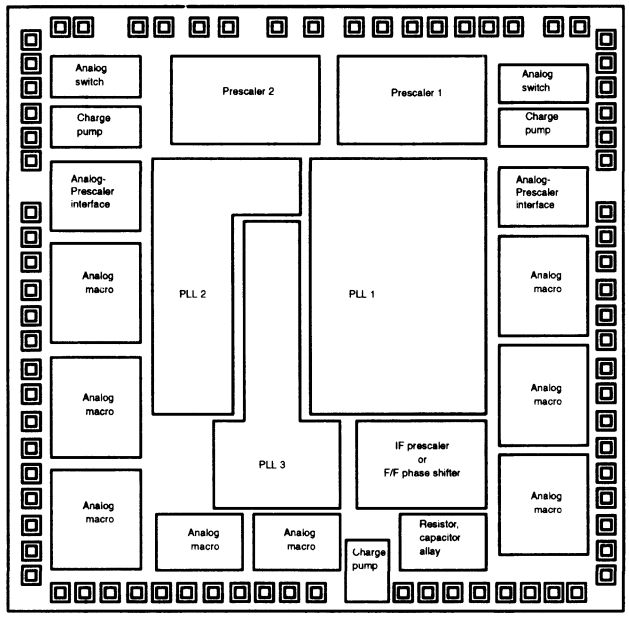
MB1540 Series

2 Prescalers
2 PLL's
6 Analog Macros

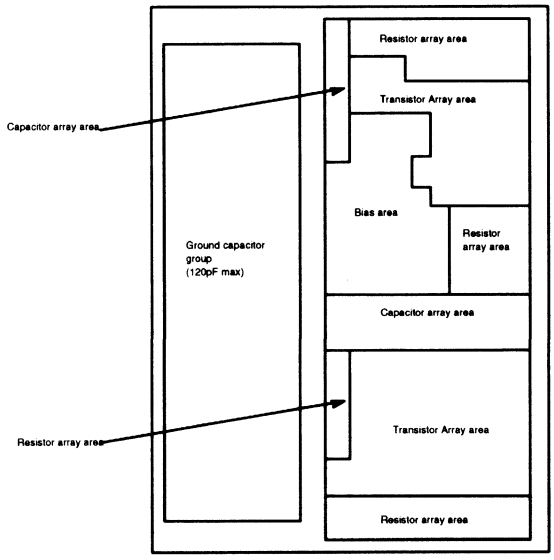


MB 1550 Series

2 Prescalers
3 PLL's
8 Analog Macros
1 Prescaler or
90°phase shifter



Analog cell


Resistor array area
Transistor Array area
Capacitor array area
Bias area
Resistor
array area
Ground capacitor
group
(120pF max)
Capacitor array area
Transistor Array area
Resistor array area
Resistor array area

ABSOLUTE MAXIMUM RATINGS

(Reference voltage is GND.)

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_{IN}	−0.5 to V_{CC}+0.5	V
Output Current	I_{OUT}	± 10	mA
Ambient Temperature	T_{STG}	−50 to +125	°C

NOTE: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

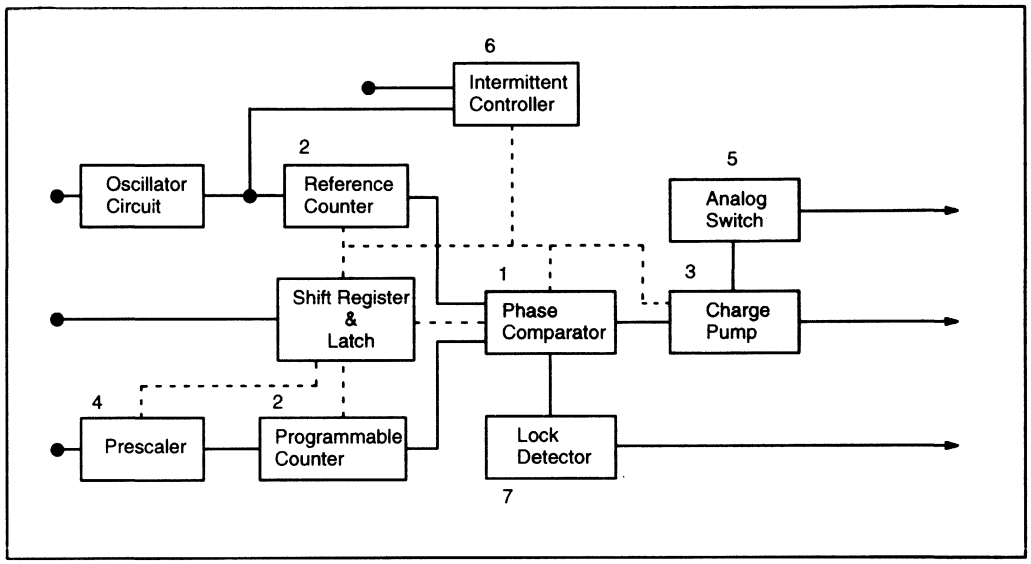
(Reference voltage is GND.)

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
Power Supply Voltage	V_{CC}	2.7*	–	5.5	V
	GND	–	0	–	V
Ambient Temperature	T_a	−40	–	+85	°C

* : The minimum operating voltage is at 2.0V, but some restriction may apply.

MACRO CELLS DESCRIPTIONS

1. Super PLL (PLL and Prescaler)



1.1. Functional Descriptions

When designing "super PLL block", some functions may be restricted depending on the kind of frames (MB1520/1530/1540/1550). Availability of main functions is summarized in Table 2.

1. Phase comparator

Phase difference detection range is -2π (pie) to $+2\pi$ (pie). In order to minimize the dead zone area, the phase comparator is designed to deliver a minimum signal to the charge pump even when the phase difference is zero. Also, it is possible to choose the characterisitcs of the phase comparator to meet polarity of VCO.

2. Counter (Reference Counter and Programmable Counter)

Two types of counters are available for PLL1 and PLL2 of all series : programmable or fixed
Regarding PLL3, one type of counter is available : Fixed

3. Charge pump

All charge pumps are based on bipolar technology. Their voltage levels at "H" depend on the power supply voltage chosen. It is possible to optimize charge pump characteristics individually according to customer needs.

*High speed lock up circuit

This circuit is an option to further increase the lock up time of the PLL, and is available for PLL1 and PLL2 (except PLL3). It will mainly be required for the new emerging digital communication standards.

4. Prescaler

Divide ratio can be chosen freely, so can two modulus type and fixed type. However, regarding PLL3, only the fixed type is available and the divide ratio can be chosed from 1/2, 1/4, and 1/8.

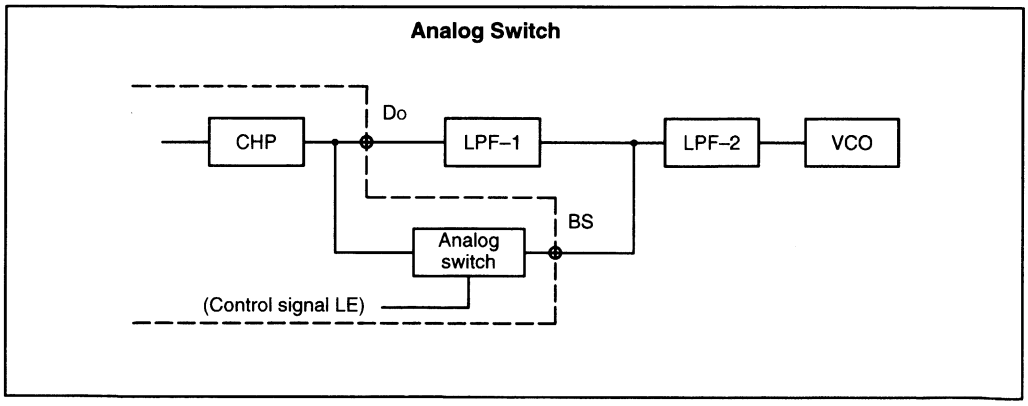
Table 2. Super PLL Function Table

		Prescaler	Programmable Counter	Reference Counter	High Speed Lock Up Function	Power Save Mode
MB1520	PLL1	T	P/F	P/F	×	×
MB1530	PLL1	T	P/F	P/F*	×	×
	PLL2	T	P/F		–	–
MB1540	PLL1	T	P/F	P/F	×	×
	PLL2	T	P/F	P/F	–	×
MB1550	PLL1	T	P/F	P/F	×	×
	PLL2	T	P/F	P/F	×	×
	PLL3	S	F	F	–	×

Note;
T:Two Modulus S:Single Modulus(1/2, 1/4, or 1/8) P/F:Programmable or Fixed
F:Fixed X:Available *:Common for PLL1 and 2

5. Analog Switch

This switch is controlled by the LE signal. When LE is "H", the analog switch is closed(ON). In this mode, the charge pump output(Do) is fed in parallel to the pin BS. This decrease the time constant of the loop filter and reduces the charge pump load. This result is an increased lock up speed.



6. Intermittent operation control circuit

The intermittent operation reduces the power consumption by powering down or waking up parts of the PLL circuitry. All, the transmission, the reception and IF block PLL may be controlled by this circuit.

If a PLL is powered up uncontrolled, the resulting phase comparator output signal is unpredictable due to an undefined phase relation between the reference frequency(f_R) and the comparison frequency(f_P) and may in the worst case take longer time for lock up of the loop.

To prevent this, the intermittent operation control circuit enforces a limited error signal output of the phase detector during power up, thus keeping the loop locked.

The circuit can be controlled externally or internally, depending on customer requirements. If controlled externally, the circuit is activated by an external signal to the PS pin. If controlled internally, the intermittent control circuit follows the power state set by the analog cells. When the power supply for the analog cells is shut down, the stand by state is automatically selected. When the analog cells are supplied with power, the active state is selected. The charge pump output is in a high impedance state during stand by, so that the VCO control voltage is being clamped at the active state level.

During the stand by state, the latches store the data which they held at the time of power down. The shift register data, on the contrary may be renewed during stand by.

NOTE:

Powering up of the digital blocks (V_{CCRD}, V_{CCTD}), (after they were disconnected) has to be done during stand by mode.

Table 3. Standard Stand by State of PLL block

		Circuit State	
		Active Mode	**Stand by Mode**
Rx	Reception circuits	×	PD
	Oscillator circuit	×	×*
	Reference counter	×	–
Tx	Transmission circuits	×	PD
	Oscillator circuit	×	×
	Reference counter	×	–
IF	IF circuits	×	PD
	Oscillator circuit	×	×
	Reference counter	×	–

Note:

X: Active state PD: Power down mode –: Stops working

*: Oscillator circuit can be stopped in parallel with RX's PS signal.

7. Lock detector circuit

LD output is selected by setting the "T" bit.(See 1.2 Serial data format.)
When the phase difference is equal or higher than tw (see diagram below), LD goes into "L". When the phase difference is tw or less and continues to be so for three cycles or more, the LD goes into "H". For example, in case of a 12.8MHz oscillator frequency tw is 625ns to 1250ns. The relation between LD and PLL circuit is shown in Table 4.

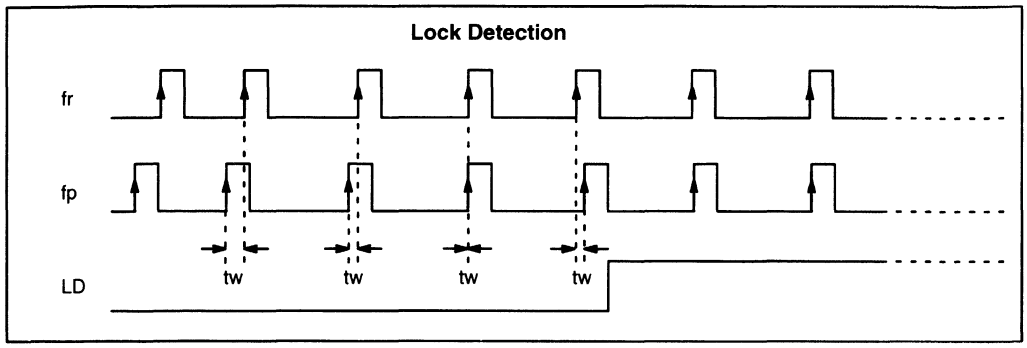


Table 4. Relation between LD signal and the circuit state

Operation mode	PLL circuit	LD output
Stand–by	Stand–by	L
Active	Unlock	L
	Lock	H

1.2 Serial Data Format

The PLL operation is controlled by serial data inputs. The parameters of this serial data are shown below. The data input starts with the MSB bit. The data length may vary between 22 and 37 bits. The actual data format is being worked out with the customer.

Table 5. Serial data format

Name		Function	Typical bit number
Control bit (CNT bit)		Selects direction of data transfer (Rx or Tx)	1 to 2
LD select bit (T bit)		Selects the LD output	1 to 2
FC bit (F bit)		Switches phase of the comparator	1
Programmable counter bit (N bit)		Sets programmable counter's divide ratio	11
Swallow counter bit (A bit)		Sets swallow counter's divide ratio	7
Reference counter bit (R bit)	Fixed	Sets reference counter's divide ratio	1 to 2
	Programmable	Sets reference counter's divide ratio	14

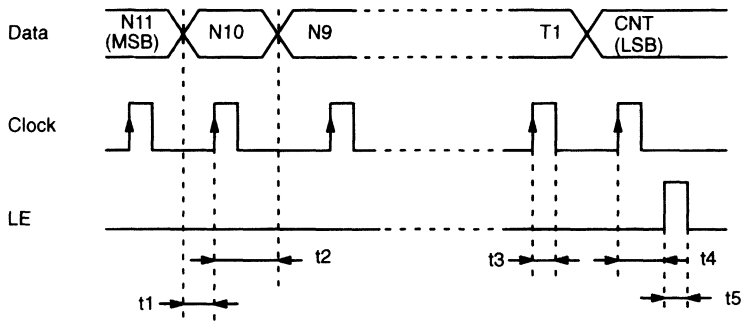
1.3 Serial Data Input Timing

Binary data is entered using the Data, Clock, and LE pins. The serial data separately controls the programmable reference divider as well as the programmable divider.
Each data bit is shifted into the internal shift register at the rising edge of each clock pulse. When the LE pin is "H", stored data is transferred from the shift register into the latch, chosen by the control bit. A schmitt trigger at each input improves noise immunity.

Note;

1) One clock pulse always shifts one data bit into the shift register, even during stand by state.
2) Input voltages (Data, Clock and LE pins) should always be lower than VCC.

Serial Data Input Timing



t1 : Data set up time (≥ 1μsec) t2 : Data hold time (≥ 1μsec) t3 : Clock pulse width (≥ 1μsec)

t4 : LE setup time to the rising edge of last clock (≥ 1μsec) t5 : LE pulse width (≥ 1μsec)

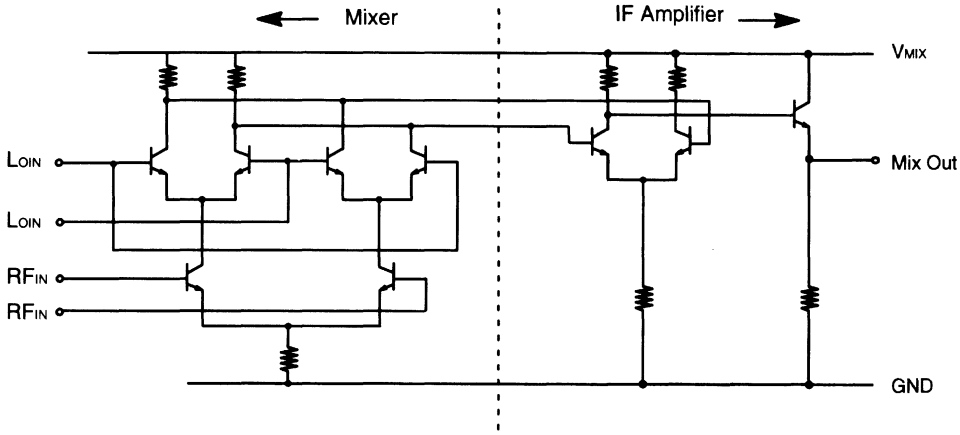
2. Mixer, IF Amplifier

Some basic examples for achievable circuits are showen below. However, concerning circuitry and performance it is possible to configure each analog macro cell to customer requirements.

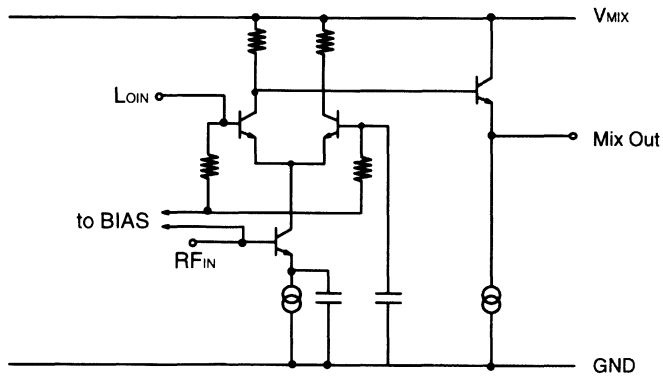
2.1 Basic Construction

Mixer circuit can either be of DBM (Double Balanced Mixer) or SBM (Single Balances Mixer) type. LO and RF inputs can be connected with the internal bias circuit, if necessary. The mixer output is connected with its own power supply (V_{MIX}) via a load resistor, than connected with the following IF amplifier.
The IF amplifier consists of a differential amplifier and NPN transistor, which forms the emitter follower output.

<Basic equivalent circuit (1)>



<Basic equivalent circuit (2)>

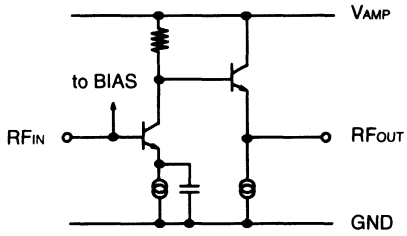


3. RF Amplifier

3.1 Basic Construction

The output signal from the common emitter circuit will be supplied through an emitter follower.

<Basic equivalent circuit>

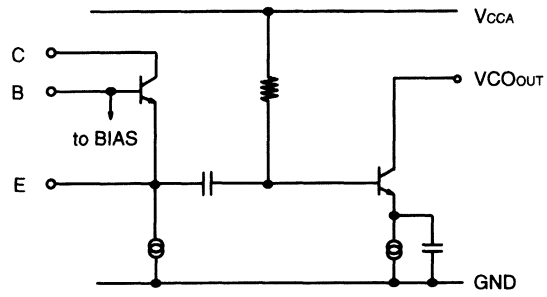


4. VCO

4.1 Basic Construction

The VCO circuit consists of an output buffer transistor and an oscillation transistor, which construct a base grounded colpitts circuit. Resonator and varicap can't be integrated in the chip. They need to be connected externally.

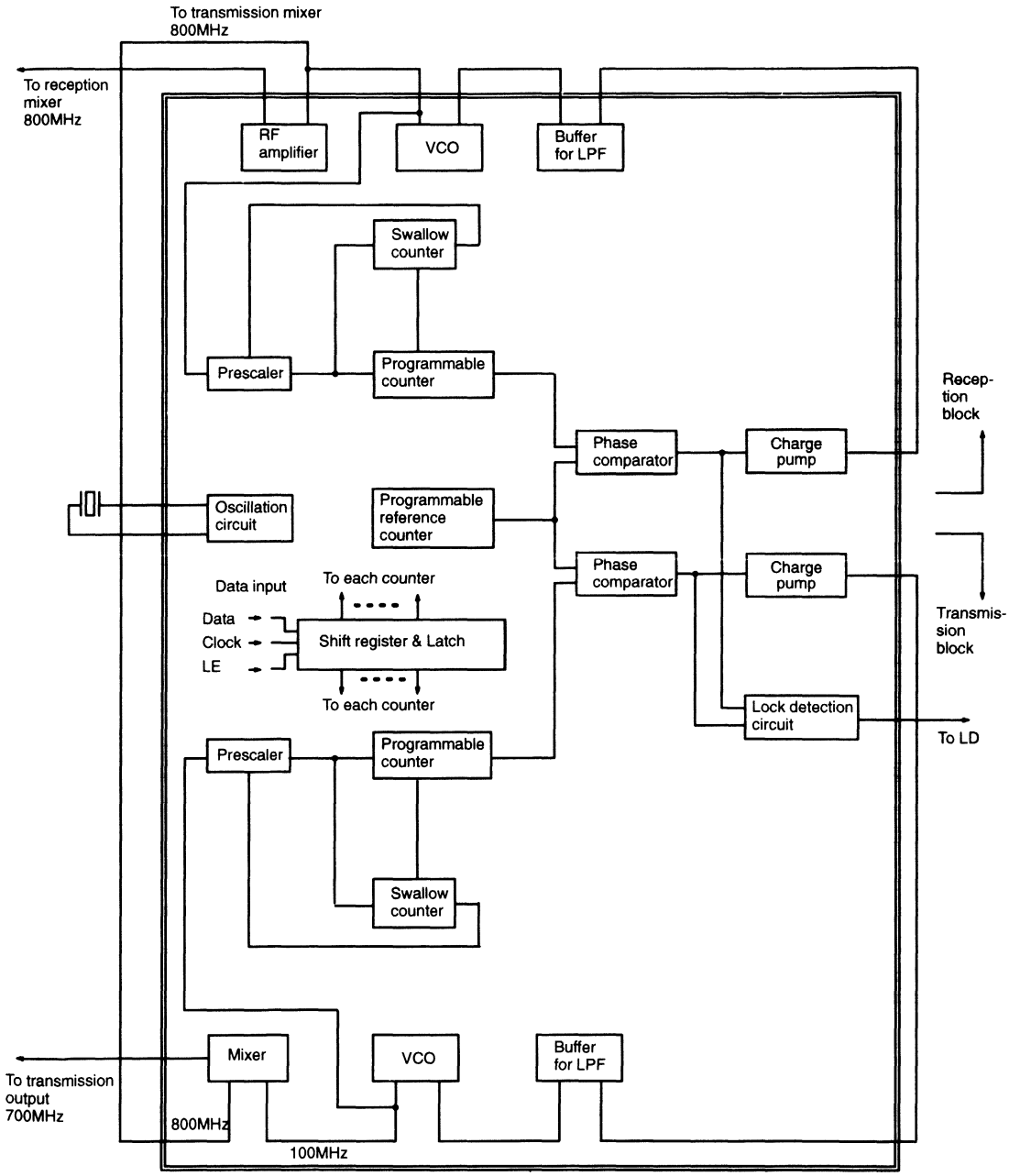
<Basic equivalent circuit>



ANALOG CIRCUITS BASIC CHARACTERISTICS EXAMPLE

Parameter	Value			Unit	Conditions
	Min.	Typ.	Max.		
VCO					
Supply Voltage	4.5	–	5.5	V	
Current Consumption	–	6	–	mA	
Operating Frequency	–	–	400	MHz	
C/N	–	70	–	dB	Offset frequency = 25kHz, BW = 15 kHz
S/N	–	50	–	dB	
Output power	–	–5	–	dBm	
Conversion Gain	–	3	–	MHz/V	
MIXER					
Supply Voltage	4.5	–	5.5	V	
Current Consumption	–	6	–	mA	
Gain	–	13	–	dB	
Maximum Output Voltage	–	–5	–	dBm	
1dB Compression Point	–	–10	–	dBm	Output Level
Intercept Point	–	–16	–	dBm	Input Level
Noise Figure	–	10	–	dB	DSB measurement
RF–Lo Isolation	–	20	–	dB	
AMPLIFIER					
Supply Voltage	4.5	–	5.5	V	
Current Consumption	–	6	–	mA	
Operating Frequency	–	400	–	MHz	
Gain	–	20	–	dB	f = 400MHz (small signal input)
Maximum Output Voltage	–	–3	–	dBm	f = 400MHz
1 dB Compression Point	–	–10	–	dBm	f = 400MHz, Output level
Intercept Point	–	–19	–	dBm	f = 400MHz, 400.1MHz, Input level
Noise Figure	–	3	–	dB	f = 400MHz

MB 1540 APPLICATION CIRCUIT EXAMPLE



DEVELOPMENT PROCEDURE

1. Study about product development

(1)The customer submits technical and commercial requests to Fujitsu, Fujitsu reviews the customer requirements, if necessary simulation is done.

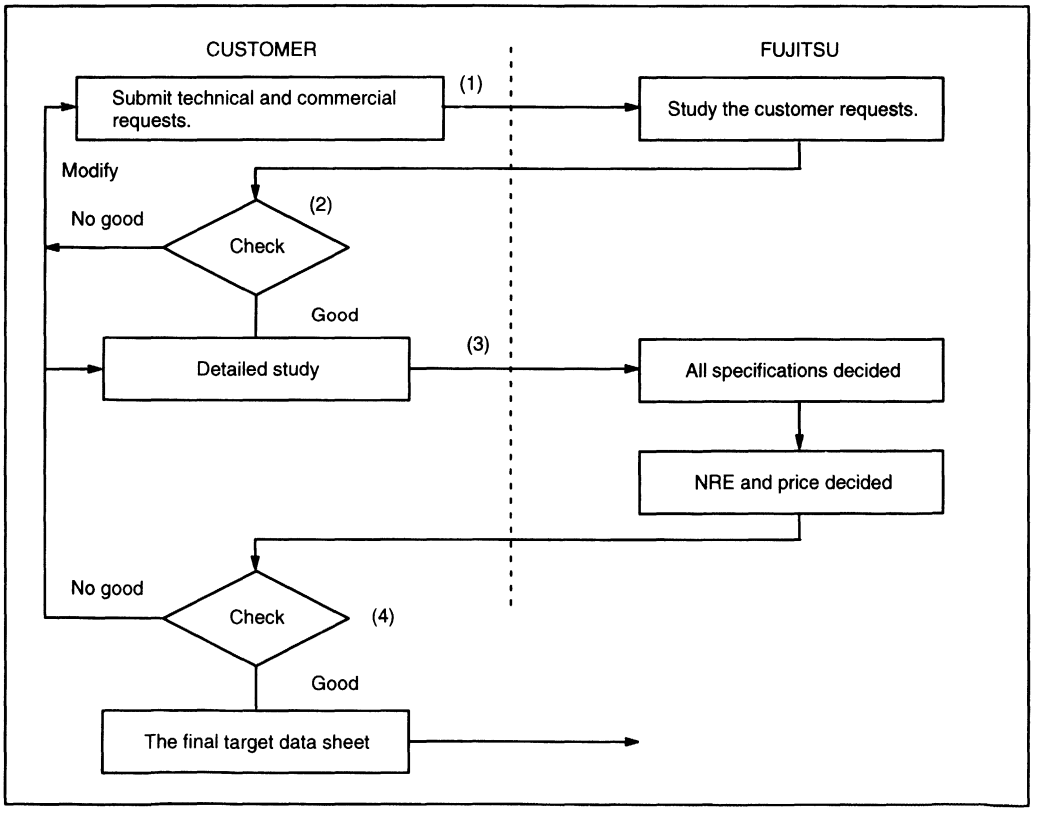
[Technical request]
Functions : Functional descriptional material, I/O signal descriptional material, Block diagram, etc.
Specifications: Prescaler, PLL, VCO, Mixer, Amplifier, etc.

[Commercial request]
Delivery and price : Development schedule, development assignment plan, demand, NRE, target price. etc.

(2)Fujitsu submits a counter proposal. And the final target specification evolves from the discussions about proposal/counter proposals between the customer and Fujitsu.

(3)Detailed circuit and test specifications are studied. Then all of the specifications will be fixed. After that development schedule, NRE, quotation are negotiated.

(4)After the customer and Fujitsu agree to develop the device, the final specification (data sheet) is submitted to the customer to confirm the specifications.

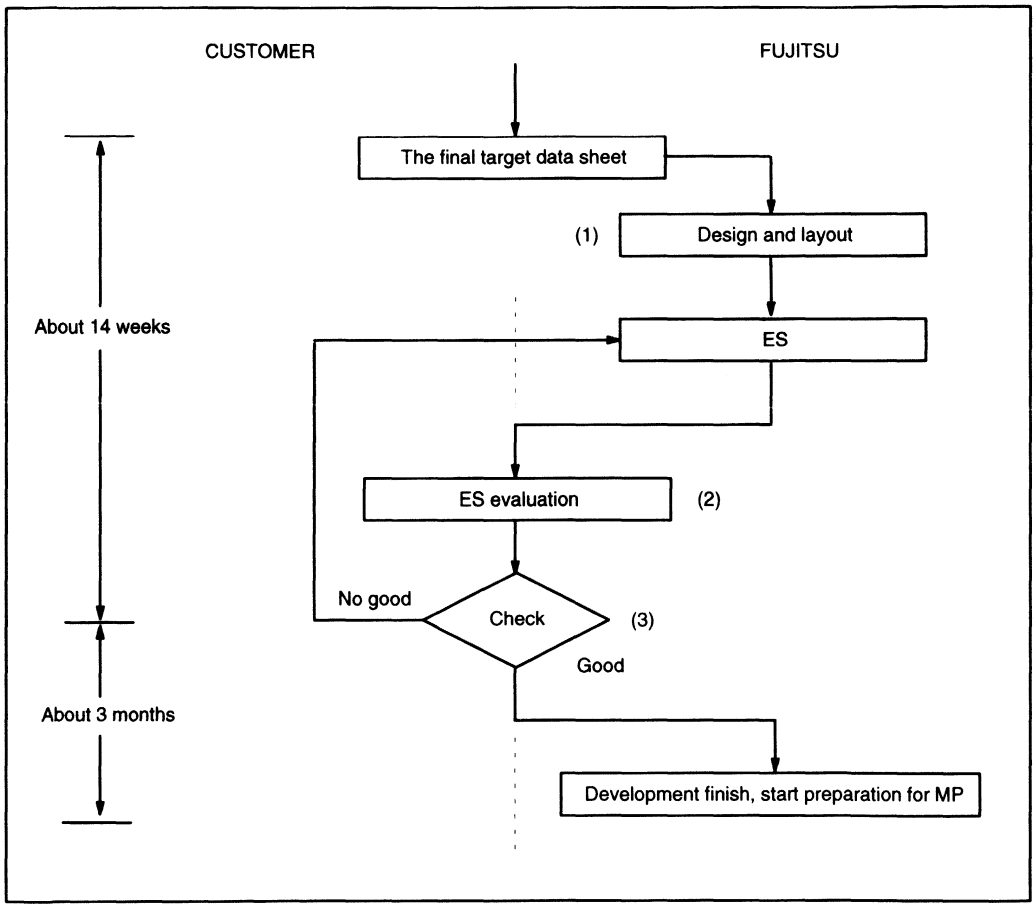


2. Development of IC

(1)Design and layout of the chip starts. First engineering samples become available approximately 14 weeks after the final target data sheet is issued.

(2)ES is evaluated by the customer and Fujitsu.

(3)If the customer satisfied with evaluation result, preparation for mass production is started. Typically 3 months are necessary for the first shipment from then.



TARGET SPECIFICATION BLANK

MB1520 Series

Vcc = ____ to ____ V, Ta = ____ to ____ °C

Parameter		Symbol	Request value			Unit	Note
			Min.	Typ.	Max.		
Power supply current		I_{CCD}				mA	Digital section
		I_{CCA}				mA	Analog section
Power supply voltage		V_{CCD}				V	Digital section (PLL, Prescaler)
		V_{CCA}				V	Analog section (VCO)
VCO	Operating frequency range	f_{VCO}				MHz	
	Output power	P_{out}				dBm	
	C/N ratio	C/N				dB	Detuning Δ f : ____ kHz Band width : ____ kHz
	S/N ratio	S/N				dB	Reference diviation: __ kHz/dev Band width : __ kHz to __ kHz
	Conversion gain	Δ f_{VCO}				MHz/V	Control voltage V_T : __ to __ V
RF-AMP	Operating frequency range	f_{AMP}				MHz	
	Gain	Gain				dB	
	Noise figure	NF				dB	
	Intercept point	IP_3				dBm	Input Level
	1 dB compression point	CP				dBm	Output Level
	In–out isolation	I_{SO}				dB	

MB1520 Series (Continued)

Vcc = ____ to ____ V, Ta = ____ to ____ °C

Parameter		Symbol	Request value			Unit	Note
			Min.	Typ.	Max.		
Mixer	Operating frequency	f_{RF}				MHz	
		f_{LO}				MHz	
		f_{IF}				MHz	Output frequency
	Gain	GAIN				dB	
	Noise figure	NF				dB	Measurement method; SSB or DSB measurement value
	Intercept point	IP_3				dBm	Input Level
	1dB compression point	CP				dBm	Output Level
	LO–RF isolation	Iso				dB	
PLL	Oscillation frequency	fosc				MHz	Comparison frequency; fr = ____ kHz
	Lock up time	T_{LR}				ms	Step frequency; Δ f = ____ kHz
Memo							

* If you have any question, please fill in the above "Memo" column.

Customer name:

Application:

ES request day:

CS request day:

Expected quantity:

TARGET SPECIFICATION BLANK

MB1530/MB1540 Series

Vcc = _____ to _____ V, Ta = _____ to _____ °C

Parameter		Symbol	Request value			Unit	Note
			Min.	Typ.	Max.		
Power supply current		I_{CCR}				mA	Reception
		I_{CCT}				mA	Transmission
Power supply voltage		V_{CCD}				V	Digital block (PLL, Prescaler)
		V_{CCA}				V	Analog block (VCO)
TX-VCO	Operating frequency range	f_{VCO}				MHz	
	Output power	P_{OUT}				dBm	
	C/N ratio	C/N				dB	Detuning Δ f : _____ kHz Band width : _____ kHz
	S/N ratio	S/N				dB	Reference diviation: __ kHz/dev Band width : __ kHz to __ kHz
	Conversion gain	Δ f_{VCO}				MHz/V	Control voltage V_T : __ to __ V
RX-VCO	Operating frequency range	f_{VCO}				MHz	
	Output power	P_{OUT}				dBm	
	C/N ratio	C/N				dB	Detuning Δ f : _____ kHz Band width : _____ kHz
	S/N ratio	S/N				dB	Reference diviation: _ kHz/dev Band width : __ kHz to __ kHz
	Conversion gain	Δ f_{VCO}				MHz/V	Control voltage V_T : __ to __ V
RF amplifier	Operating frequency range	f_{AMP}				MHz	
	Gain	Gain				dB	
	Noise figure	NF				dB	
	Intercept point	IP_3				dBm	Input Level
	1 dB compression point	CP				dBm	Output Level
	In–out isolation	Iso				dB	

MB1530/MB1540 Series (Continued)

Vcc = ____ to ____ V, Ta = ____ to ____ °C

Parameter		Symbol	Request value			Unit	Note	
			Min.	Typ.	Max.			
Mixer	Operating frequency	f_{RF}				MHz		
		f_{LO}				MHz		
		f_{IF}				MHz	Output frequency	
	Gain	GAIN				dB		
	Noise figure	NF				dB	Measurement method; SSB or DSB measurement value	
	Intercept point	IP_3				dBm	Input Level	
	1dB compression point	CP				dBm	Output Level	
	LO–RF isolation	Iso				dB		
PLL	Oscillation frequency	fosc				MHz	Comparison frequency; fr = ____ kHz	
	Lock up time	T_{LR}				ms	Reception	Step frequency, Δ f = ____ kHz
		T_{LT}				ms	Transmission	
Memo								

* If you have any question, please fill in the above "Memo" column.

Customer name:

Application:

ES request day:

CS request day:

Expected quantity:

MEMO

FUJITSU SEMICONDUCTOR
DATA SHEET

DS06-70102-1E

Semicustom ASTRO MASTER II

BIPOLAR

Semi-Custom LSI for High Frequency Analog Circuits

MB54500 Series

■ DESCRIPTION

ASTRO MASTER II is a semicustom LSI that uses master-slice technology and is suitable for high frequency front-end analog circuits such as VCOs, amplifiers, and mixers.

The MB54500 series consists of two sets of analog cells with the same analog circuits as the ASTRO MASTER I. These enable the use of standard macro cells and design to suit user specifications.

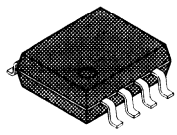
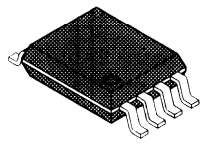
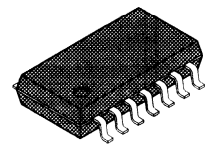
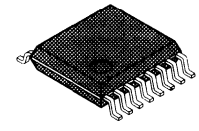
The LSI is available in ultra-small flat packages enabling integration of high frequency analog circuits.

ASTRO: Advanced Semi-custom Technology of RF system On LSI

■ FEATURES

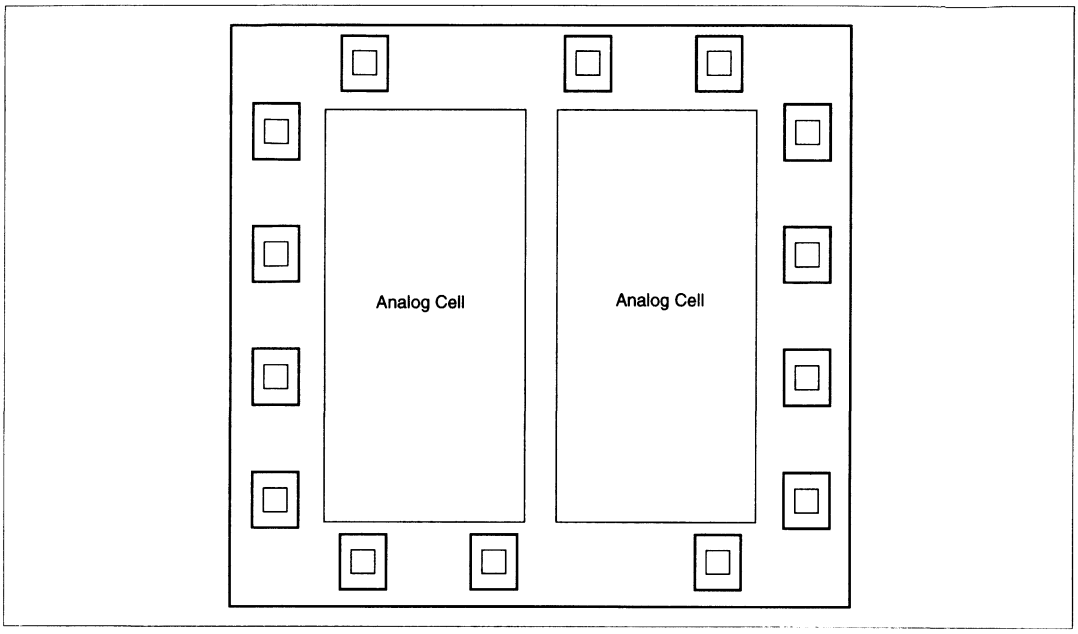
- Ideal for high frequency front-end analog circuits in mobile communications equipment such as mobile telephones.
- The circuit configuration can be customized, including adjustment of resistance values.
- High frequency response: up to 2 GHz
- Supply voltage: 2.7 V to 5.5 V
- Operating temperature range: –40°C to +85°C
- Development period: Typically ten weeks after specifications confirmed.
- A power saving circuit can be configured.
- Available in an ultra-small package (SSOP 8-pin)

■ PACKAGES

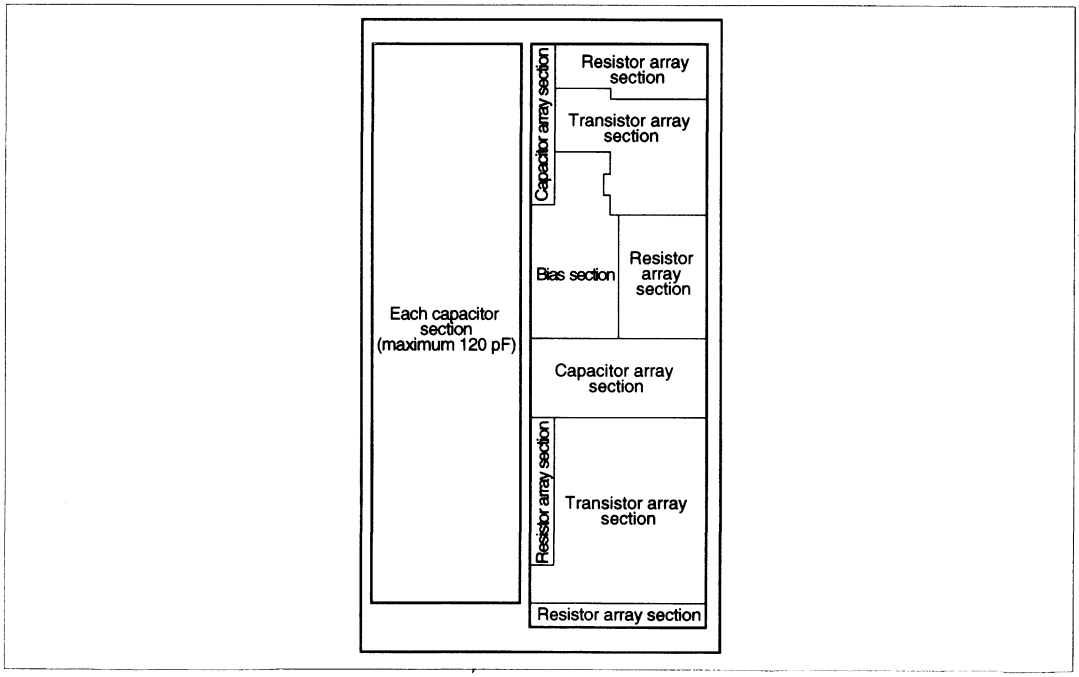
8-pin, Plastic SOP	8-pin, Plastic SSOP	14-pin, Plastic SOP	16-pin, Plastic SSOP
			
(FPT-8P-M01)	(FPT-8P-M03)	(FPT-14P-M04)	(FPT-16P-M05)

■ CHIP LAYOUT

• MB54500 Series



• Analog Cell



■ MACRO CELL DESCRIPTIONS
High Frequency Analog Cells

- Mixer

  Active double-balanced mixer

- IF amplifier

  The IF amplifier consists of a differential amplifier and NPN transistor. The differential amplifier output uses an emitter-follower circuit.

- RF amplifier

  The output signal of a grounded emitter circuit is output via an emitter-follower circuit. The RF input can be connected to the internal bias circuit.

- VCO

  Consists of the oscillator transistor of a grounded-base Colpitts oscillator circuit and an output buffer transistor. Use with an external varicap, resonator, or similar.

Note: Circuit types and other specifications can be modified on request.

■ FAMILY

The MB54500 series are semi-custom LSIs that can be developed to specific application specifications. The series uses master-slice technology with standard element arrays (bulk).

The following three ASSP models are available.

MB54501: 1.1GHz band, front end LSI
MB54502: 1.1GHz band, low-noise, low-current amplifier
MB54503: 1.1GHz band, high-power amplifier

The MB531 and MB539 are also available as ASSP using the same technology.

MB531: 1.1GHz band transmit mixer
MB539: 1.6GHz band low-noise amplifier

■ ABSOLUTE MAXIMUM RATINGS

(Voltages are relative to GND)

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{CC}	−0.5 to +7.0	V
Input voltage	V_{IN}	−0.5 to V_{CC} +0.5	V
Output current	I_{OUT}	±10	mA
Storage temperature	Tstg	−50 to +125	°C

Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Power supply voltage	V_{CC}	2.7	—	5.5	V
	GND	—	0	—	V
Operating temperature	Ta	−40	—	+85	°C

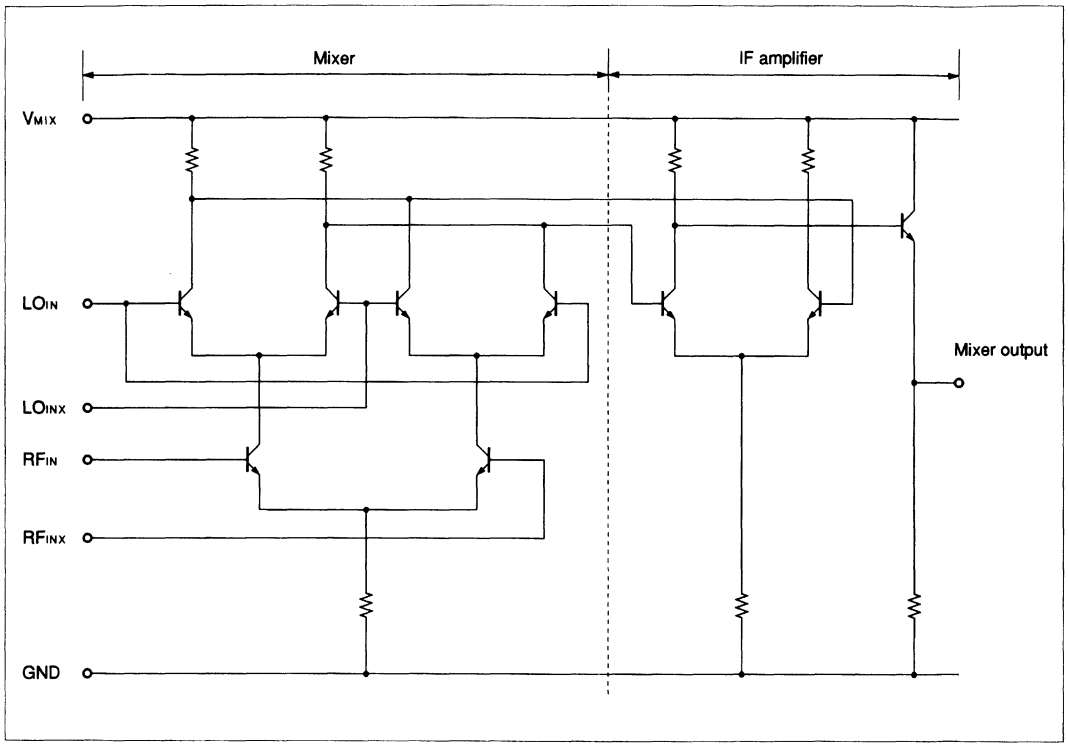
■ BASIC CHARACTERISTICS OF THE ANALOG CIRCUITS (EXAMPLE)

Circuit	Parameter		Conditions	Value			Unit
				Min.	Typ.	Max.	
VCO	Power supply voltage		—	4.5	—	5.5	V
	Current consumption		—	—	5	—	mA
	Operating frequency		—	—	—	400	MHz
	C/N ratio		Offset frequency = 25kHz, BW = 15kHz	—	70	—	dB
	S/N ratio		—	—	46	—	dB
	Output power		—	—	–5	—	dBm
	Conversion gain		—	—	6	—	MHz/V
Mixer	Power supply voltage		—	4.5	—	5.5	V
	Current consumption		—	—	13	—	mA
	Operating frequency	RF	—	—	870	—	MHz
		LO	P_{LO} = 0 dBm	—	780	—	MHz
		IF	$f_{IF} = f_{RF} - f_{LO}$	—	90	—	MHz
	Gain		—	—	14	—	dB
	Maximum output power		—	—	0	—	dBm
	1dB compression point		Output level	—	–3	—	dBm
	Intercept point		Input level	—	–6	—	dBm
	NF		DSB value	—	12	—	dB
	Isolation		Between RF-LO	—	20	—	dB
Amplifier	Power supply voltage		—	4.5	—	5.5	V
	Current consumption		—	—	6	—	mA
	Operating frequency		—	—	400	—	MHz
	Gain		f = 400MHz (–30 dBm in)	—	17	—	dB
	Maximum output power		f = 400MHz	—	0	—	dBm
	1dB compression point		f = 400MHz, Output level	—	–4	—	dBm
	Intercept point		f = 400MHz, 400.1MHz input level	—	–10	—	dBm
	NF		f = 400MHz	—	3	—	dB

■ BASIC EQUIVALENT CIRCUITS FOR THE ANALOG CIRCUITS

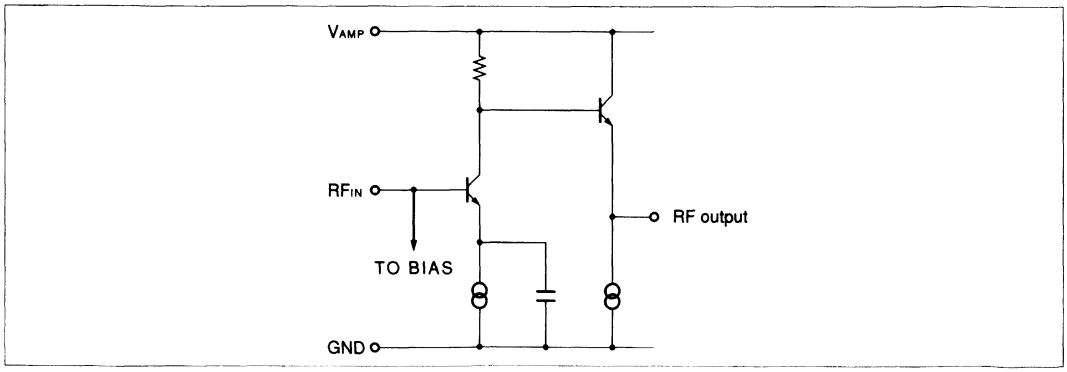
1. Mixer, IF Amplifier

The mixer is an active, double-balanced mixer. The LO and RF outputs can be connected to an internal bias circuit. The mixer output has an internal load resistor connected to its power supply and connects to the IF amplifier in the next stage. The IF amplifier consists of a differential amplifier with an emitter-follower output.



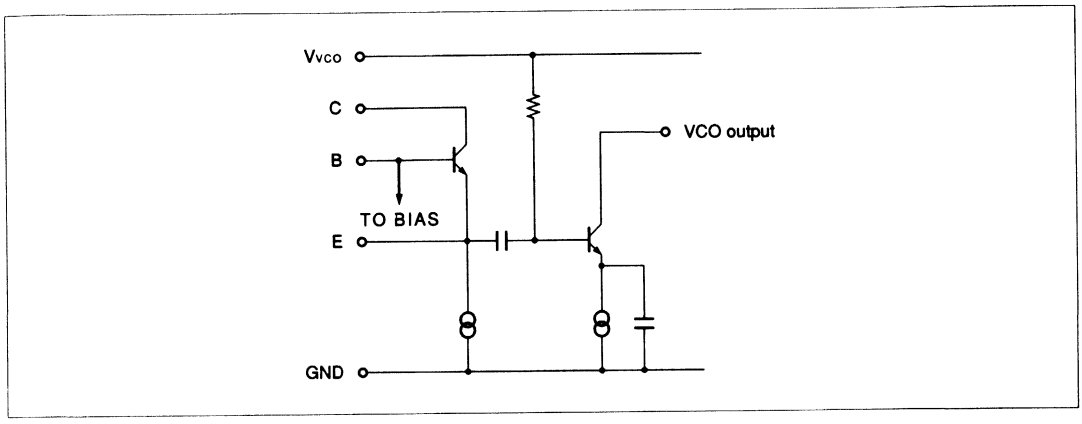
2. RF Amplifier

The output signal of a grounded-emitter circuit is output via an emitter-follower circuit. The RF input can be connected to the internal bias circuit.



3. VCO

Consists of the oscillator transistor of a grounded-base Colpitts oscillator circuit and an output buffer transistor. Use with an external varicap, resonator, or similar.



■ DEVELOPMENT PROCESSES

The following describes the ASTRO MASTER II development process. The process starts with materials provided by the customer.

1. Product Viability Study

(1) Study of product specifications and development process

Fujitsu evaluates the technical and economic viability of the product by performing simulations and other analysis based on the data provided by the customer.

- Product data

  Function data: Function description, I/O signal description, block diagram
  Characteristics data: VCO, mixer, amplifier, etc.

- Development data

  Schedule data: Development schedule, development workload plan
  Cost estimate data: Number of items to be purchased, development costs, target price

(2) Product viability study

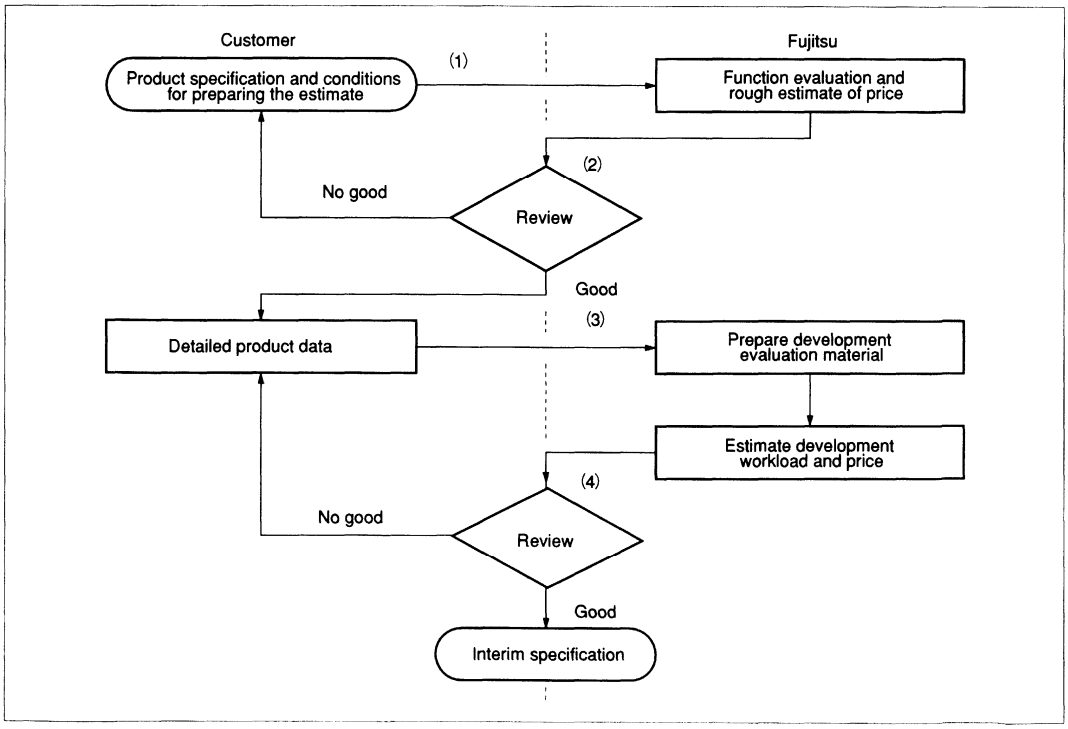
The customer and Fujitsu study whether the product is viable based on the evaluation results.

(3) Specification preparation

Circuit functions and circuit characteristics are studied in detail. Circuit specifications and test specifications are studied. A final estimate of the development workload, development period, development cost, and product price is made after the specification is confirmed.

(4) Confirm interim specification

After deciding whether or not to proceed with product development, the customer and Fujitsu exchange an interim specification.



2. LSI Development

(1) LSI design and prototyping

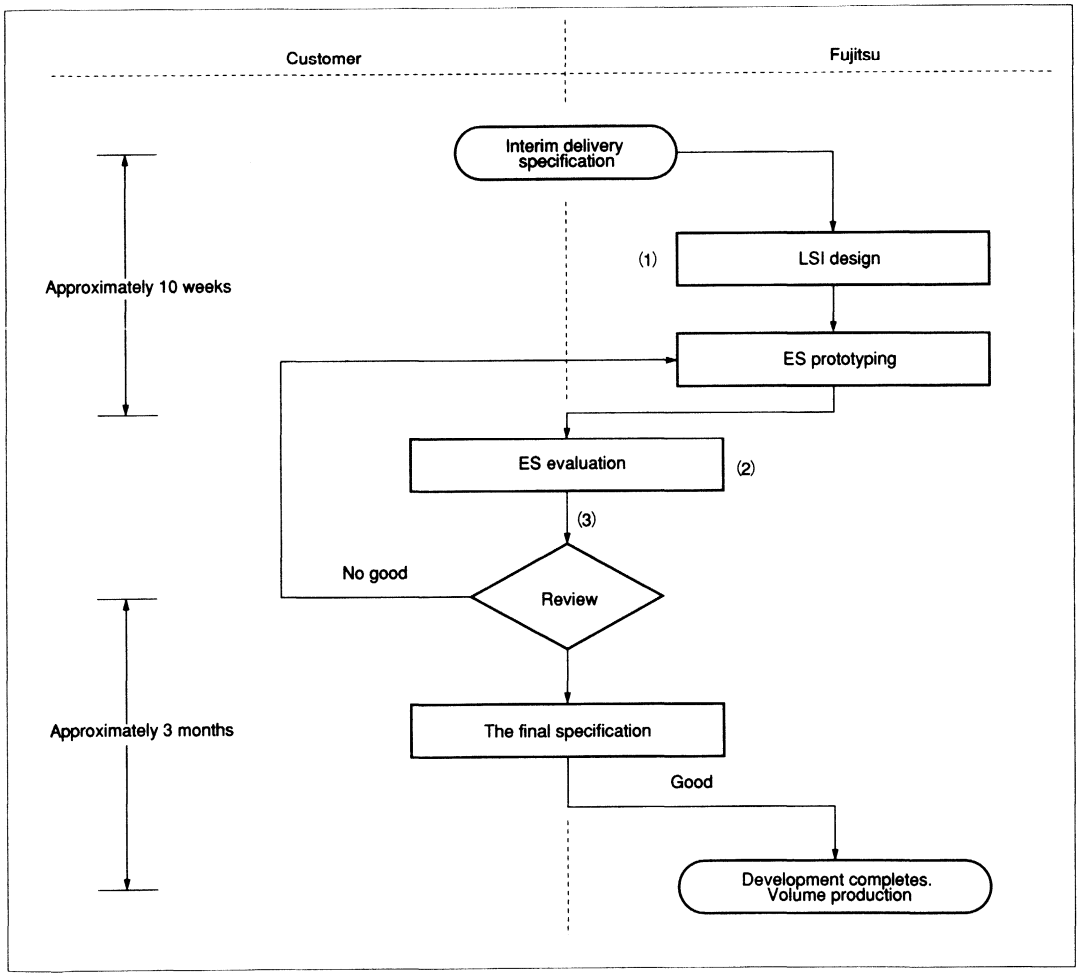
The LSI design and prototypes are prepared based on the interim specification exchanged between the customer and Fujitsu. The typical time required to produce engineering samples is approximately ten weeks after the interim specification is confirmed.

(2) Engineering sample (ES) evaluation

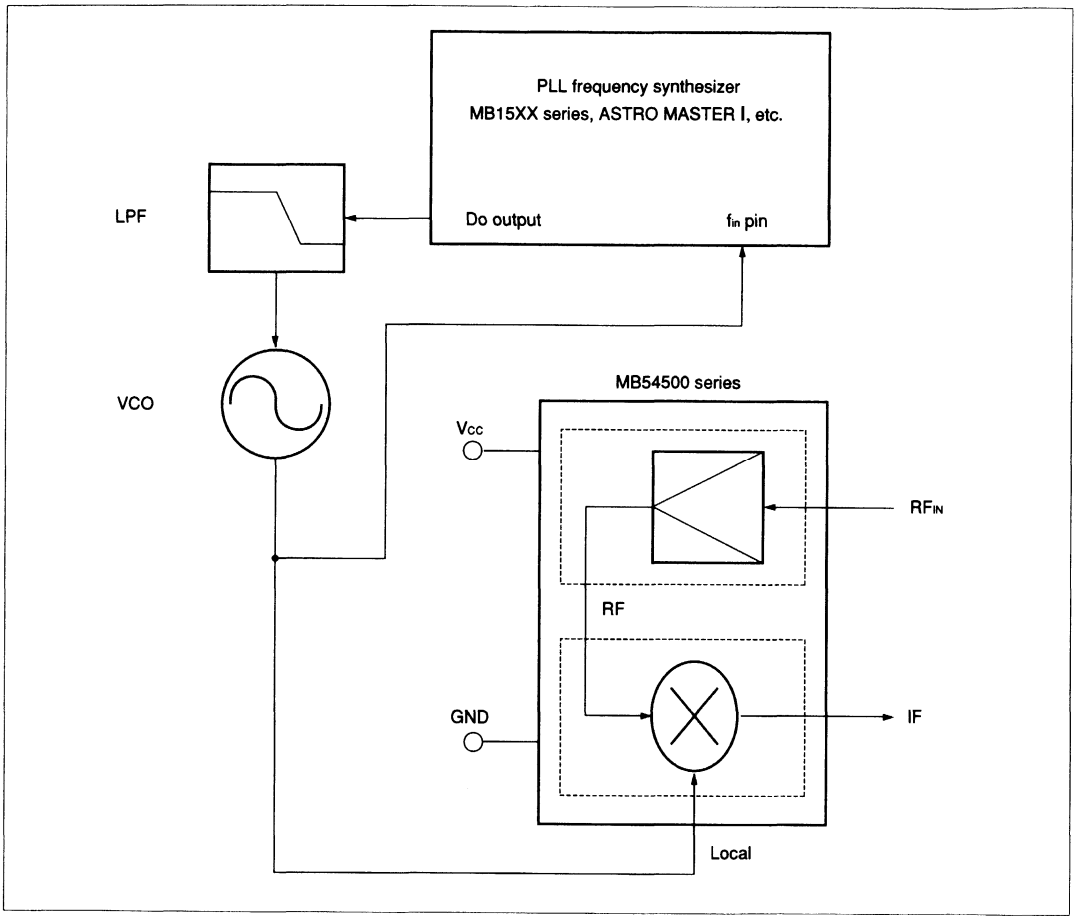
The customer and Fujitsu independently evaluate the engineering samples based on the interim specification.

(3) Final confirmation

If there are no problems with the evaluation results, the customer and Fujitsu exchange the final specification. This completes development. The next stage is volume production. The time required until volume production shipment is typically about three months.



■ APPLICATION EXAMPLE



■ ORDERING INFORMATION

Part number	Package	Remarks
MB545xx PF	8pin, Plastic SOP (FPT-8P-M01)	
MB545xx PFV	8pin, Plastic SSOP (FPT-8P-M03)	
MB545xx PF	14pin, Plastic SOP (FPT-14P-M04)	
MB545xx PFV	14pin, Plastic SSOP (FPT-16P-M05)	

MEMO

FUJITSU SEMICONDUCTOR
DATA SHEET

DS06-70103-1E

Semicustom ASTRO MASTER III

BIPOLAR

Semi-Custom LSI for High Frequency Analog Circuits

MB54600 Series

■ DESCRIPTION

ASTRO MASTER III is a semicustom LSI that uses master-slice technology and is suitable for high frequency front-end analog circuits such as VCOs, amplifiers, mixers, and quadrature modulator/demodulators.

The MB54600 series consists of six analog cells with further enhanced versions of the ASTRO MASTER I analog circuits, two phase shift cells, and one prescaler cell. These enable use of standard macro cells and design to suit user specifications.

The LSI uses the latest wafer process technology to achieve low power consumption. Also, the device is available in ultra-small flat packages, contributing to secrecy of circuit design and enabling smaller and lighter systems to be developed by reducing the component count.

The product is ideal for digital-specification mobile communications equipment.

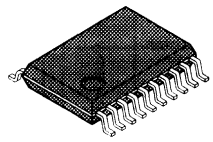
ASTRO: Advanced Semi-custom Technology of RF system On LSI

■ FEATURES

- Ideal for high frequency front-end analog circuits in mobile communications equipment such as mobile telephones.
- Uses high performance bipolar transistors with high f_T (20 GHz max.)
- High frequency response: up to 3 GHz
- Supply voltage: 2.7 V to 3.3 V
- Operating temperature range: –40°C to +85°C
- Development period: Typically ten weeks after specifications confirmed.
- A power saving circuit can be configured.
- Available in an ultra-small package (SSOP 20-pin, SSOP 34-pin)

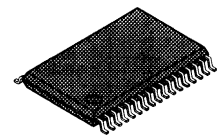
■ PACKAGES

20-pin, Plastic SSOP



(FPT-20P-M03)

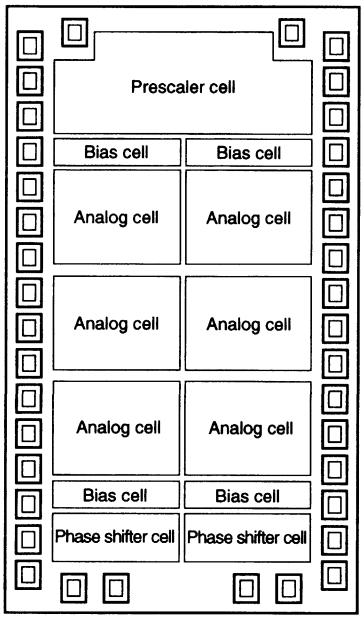
34-pin, Plastic SSOP



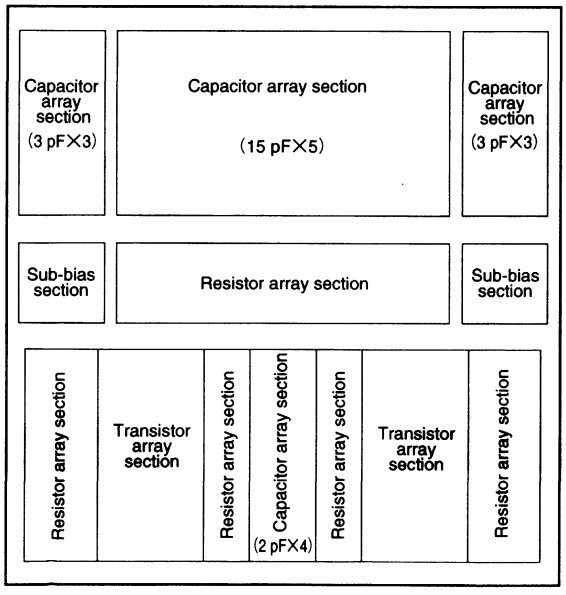
(FPT-34P-M03)

■ CHIP LAYOUT

• MB54600 Series



• Analog Cell



■ MACRO CELL DESCRIPTIONS
High Frequency Analog Cells

- Mixer

  Active double-balanced mixer

- IF amplifier

  The IF amplifier consists of a differential amplifier and NPN transistor. The differential amplifier output uses an emitter-follower circuit.

- RF amplifier

  The output signal of a grounded emitter circuit is output via an emitter-follower circuit. The RF input can be connected to the internal bias circuit.

- VCO

  Consists of an oscillator transistor for a grounded-base Colpitts oscillator circuit and an output buffer transistor. Use with an external varicap, resonator, or similar.

Prescaler Cell

Enables a MB501UL or MB517 equivalent prescaler to be formed. Supports low-current operation.

Phase Shifter Cell

A flip-flop type 90° phase shift circuit can be formed for use in a quadrature modulator or quadrature demodulator.

Note: Circuit types and other specifications can be modified on request.

■ ABSOLUTE MAXIMUM RATINGS

(Voltages are relative to GND)

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{CC}	−0.5 to +4.0	V
Input voltage	V_{IN}	−0.5 to V_{CC} +0.5	V
Output current	I_{OUT}	±10	mA
Storage temperature	Tstg	−50 to +125	°C

Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

(Voltages are relative to GND)

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Power supply voltage	V_{CC}	2.7	3.0	3.3	V
	GND	—	0	—	V
Operating temperature	Ta	−40	—	+85	°C

■ BASIC CHARACTERISTICS OF THE ANALOG CIRCUITS (EXAMPLE)

Circuit	Parameter		Conditions	Value			Unit
				Min.	Typ.	Max.	
VCO	Power supply voltage		—	2.7	3.0	3.3	V
	Current consumption		—	—	8	—	mA
	Operating frequency		—	—	—	900	MHz
	C/N ratio		Offset frequency = 25 kHz, BW = 16 kHz	—	83	—	dB
	S/N ratio		BW = 0.3 to 3 kHz, 3 kHz/Dev	—	49	—	dB
	Output power		—	—	–2	—	dBm
	Conversion gain		—	—	5	—	MHz/V
Mixer	Power supply voltage		—	2.7	3.0	3.3	V
	Current consumption		—	—	12	—	mA
	Operating frequency	IF	—	—	800	—	MHz
		L_O	P_{LO} = –10 dBm	—	110	—	MHz
		RF	$f_{RF} = f_{LO} + f_{IF}$	—	910	—	MHz
	Gain		—	—	4	—	dB
	Maximum output voltage		—	—	–9	—	dBm
	1dB compression point		Output level	—	–11	—	dBm
	intercept point		Input level	—	–1	—	dBm
	NF		DSB value	—	12	—	dB
Amplifier	Power supply voltage		—	2.7	3.0	3.3	V
	Current consumption		—	—	6	—	mA
	Operating frequency		—	—	900	—	MHz
	Gain		f = 900 MHz (–30 dBm in)	—	14	—	dB
	Maximum output voltage		f = 900 MHz	—	–3	—	dBm
	1dB compression point		f = 900 MHz, Output level	—	–7	—	dBm
	Intercept point		f = 900 MHz, 900.1MHz input level	—	–13	—	dBm
	NF		f = 900 MHz	—	1.9	—	dB

(Continued)

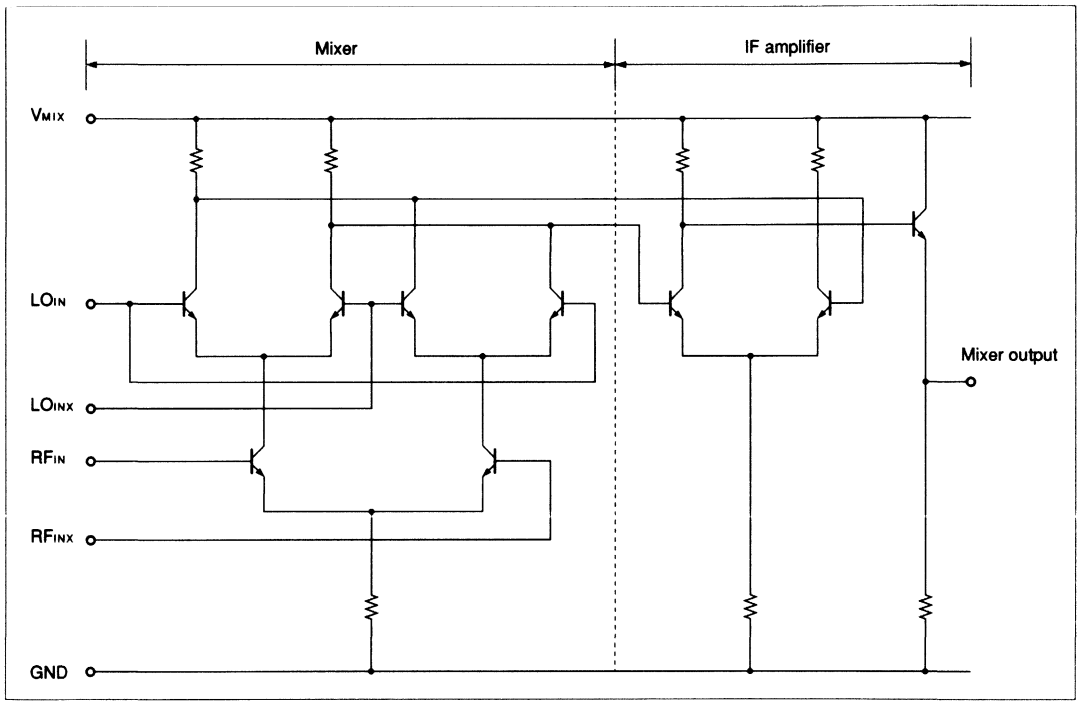
(Continued)

Circuit	Parameter		Conditions	Value			Unit
				Min.	Typ.	Max.	
Quadrature modulator	Power supply voltage		—	2.7	3.0	3.3	V
	Current consumption		—	—	25	—	mA
	Operating frequency	L_{O1}	P_{LO1} = –15 dBm	—	480	—	MHz
		L_{O2}	P_{LO2} = –5 dBm	—	1660	—	MHz
		RF	$f_{RF} = f_{LO2} + f_{LO1}/2$	—	1900	—	MHz
	Output level		Including up-converter	—	–12	—	dBm
	Modulation accuracy	Amplitude error	RMS Magnitude Error	—	1.1	—	%
		Phase error	RMS Phase Error	—	0.73	—	deg
		Vector error	RMS Vector Error	—	1.7	—	%
	Carrier suppression		External offset, no offset adjustment	—	–40	–30	dBc

■ BASIC EQUIVALENT CIRCUITS FOR THE ANALOG CIRCUITS

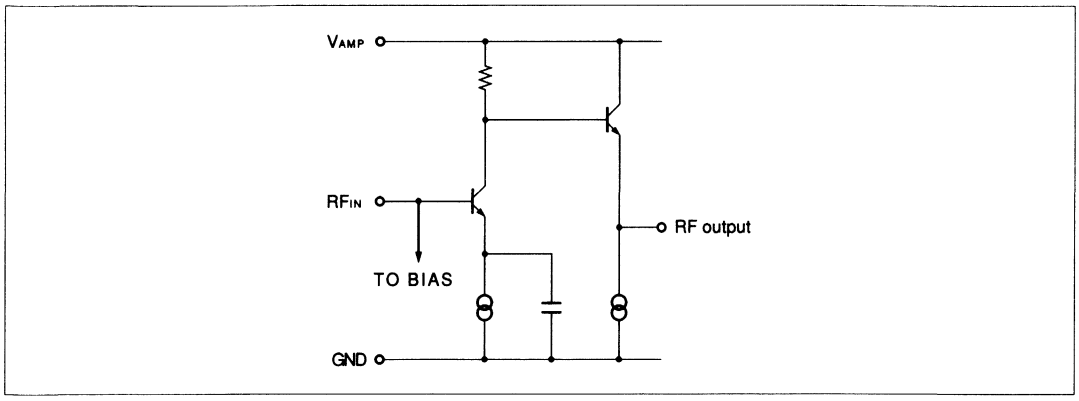
1. Mixer, IF Amplifier

The mixer is an active, double-balanced mixer. The LO and RF outputs can be connected to an internal bias circuit. The mixer output has an internal load resistor connected to its power supply and connects to the IF amplifier in the next stage. The IF amplifier consists of a differential amplifier with an emitter-follower output.



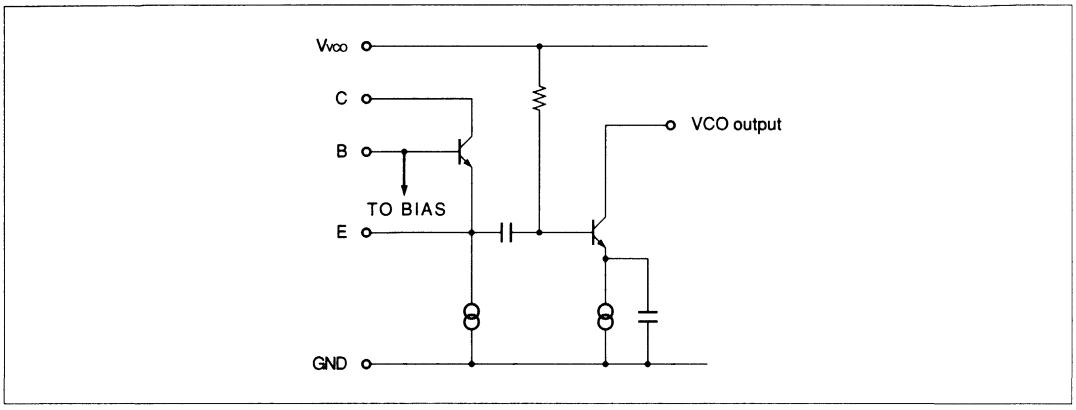
2. RF Amplifier

The output signal of a grounded-emitter circuit is output via an emitter-follower circuit. The RF input can be connected to the internal bias circuit.



3. VCO

Consists of the oscillator transistor of a grounded-base Colpitts oscillator circuit and an output buffer transistor. Use with an external varicap, resonator, or similar.



■ DEVELOPMENT PROCESSES

The following describes the ASTRO MASTER III development process. The process starts with materials provided by the customer.

1. Product Viability Study

(1) Study of product specifications and development process

Fujitsu evaluates the technical and economic viability of the product by performing simulations and other analysis based on the data provided by the customer.

- Product data

  Function data: Function description, I/O signal description, block diagram
  Characteristics data: Prescaler, VCO, mixer, amplifiers, quadrature modulator, etc.

- Development data

  Schedule data: Development schedule, development workload plan
  Cost estimate data: Number of items to be purchased, development costs, target price

(2) Product viability study

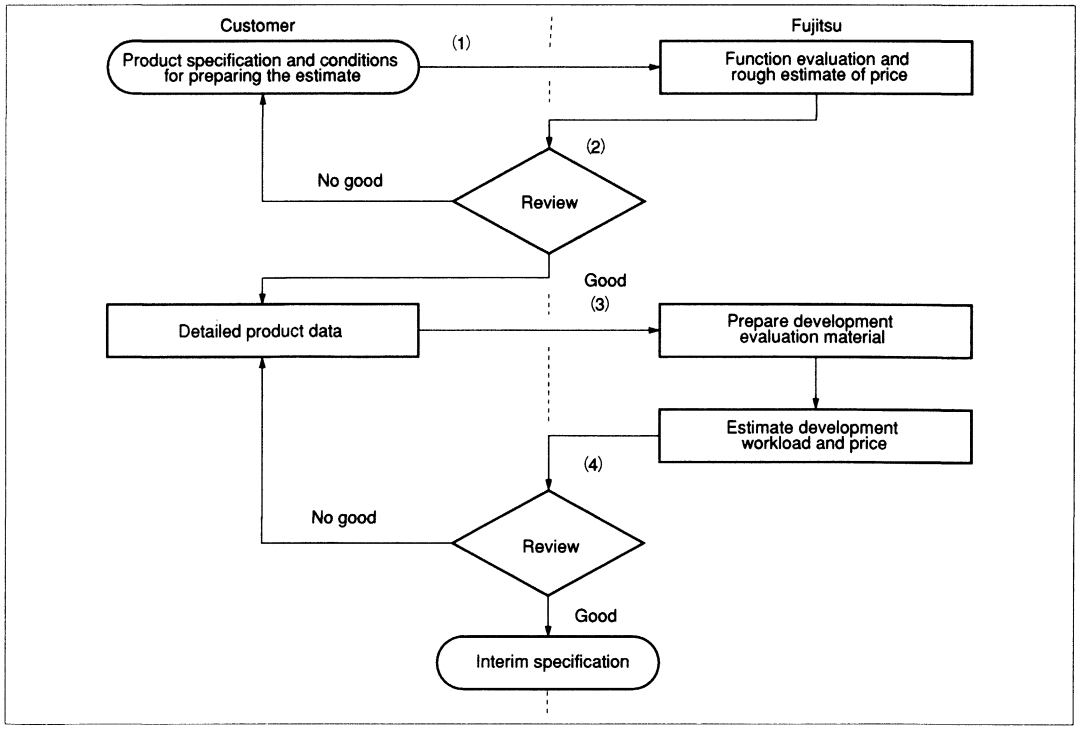
The customer and Fujitsu study whether the product is viable based on the evaluation results.

(3) Specification preparation

Circuit functions and circuit characteristics are studied in detail. Circuit specifications and test specifications are studied. A final estimate of the development workload, development period, development cost, and product price is made after the specification is confirmed.

(4) Confirm interim specification

After deciding whether or not to proceed with product development, the customer and Fujitsu exchange an interim specification.



2. LSI Development

(1) LSI design and prototyping

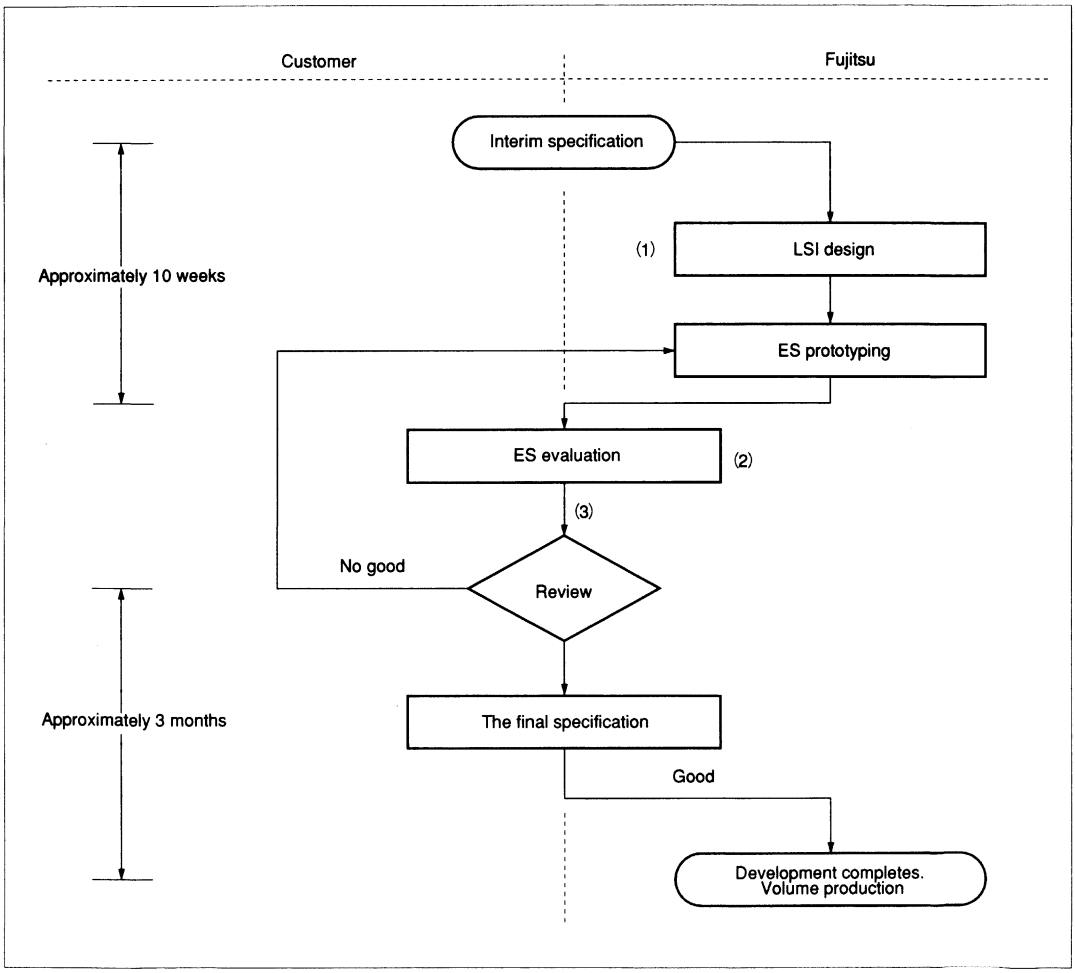
The LSI design and prototypes are prepared based on the interim specification exchanged between the customer and Fujitsu. The typical time required to produce engineering samples is approximately ten weeks after the interim specification is confirmed.

(2) Engineering sample (ES) evaluation

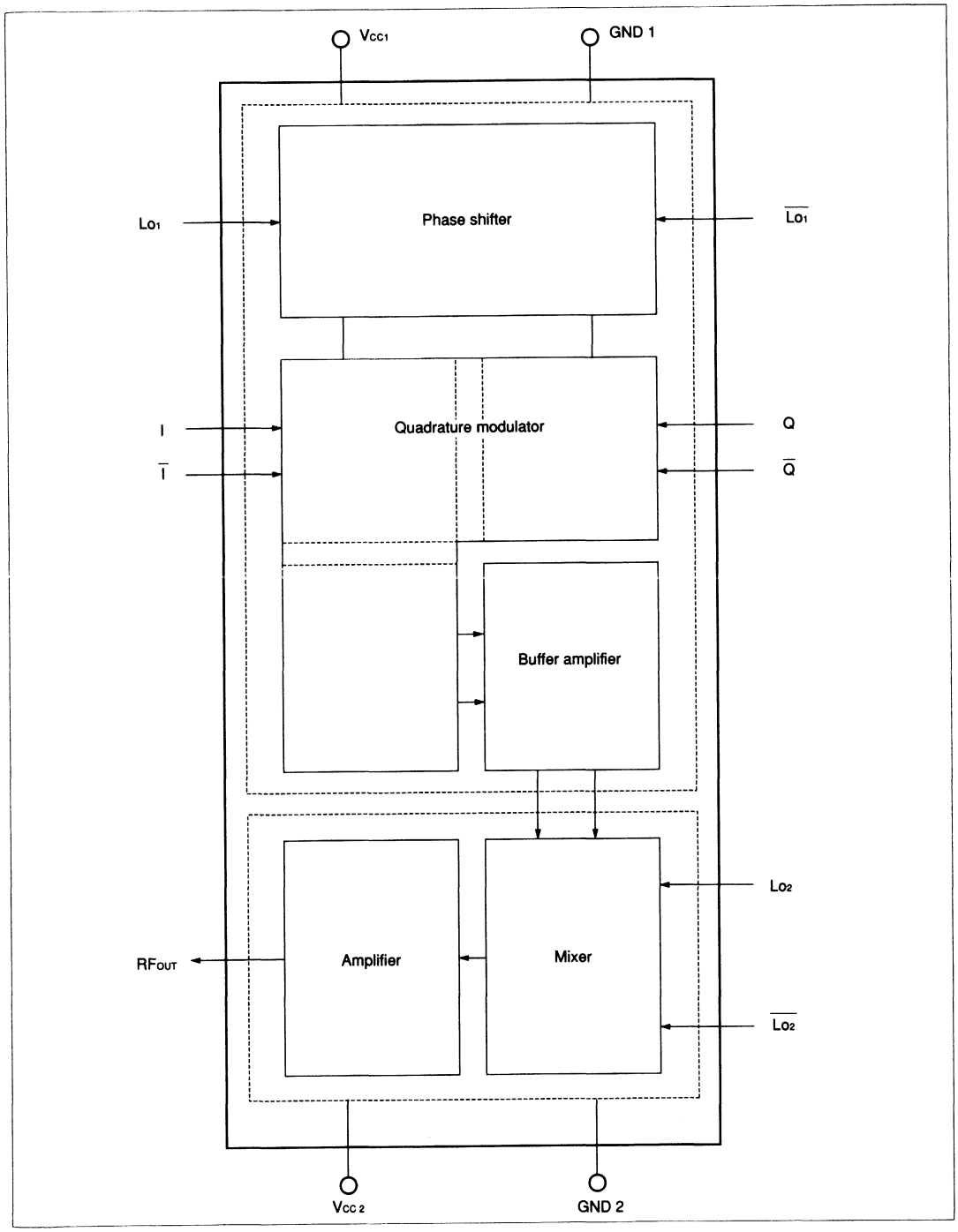
The customer and Fujitsu independently evaluate the engineering samples based on the interim specification.

(3) Final confirmation

If there are no problems with the evaluation results, the customer and Fujitsu exchange the final specification. This completes development. The next stage is volume production. The time required until volume production shipment is typically about three months.



■ APPLICATION EXAMPLE



■ ORDERING INFORMATION

Part number	Package	Remarks
MB546xx PFV	20-pin, Plastic SSOP (FPT-20P-M03)	
MB546xx PFV	34-pin, Plastic SSOP (FPT-34P-M03)	

FUJITSU SEMICONDUCTOR
DATA SHEET

DS06–70104–1E

Semicustom

Bi-CMOS

ASTRO MASTER IV Specification

(for PLL frequency synthesizers)

MB1560 Series

■ DESCRIPTION

The ASTRO MASTER IV is a master-slice type semi-custom LSI ideal for use in high-frequency front-end circuits in VCO, amplifier, mixer and orthogonal modulator devices.

The MB1560 series features an analog circuit unit that is a more highly integrated version of the ASTRO MASTER I series featuring two analog cell circuits, plus a digital circuit unit with a power-saving prescaler circuit and a PLL1 circuit with pulse-swallow capability.

The PLL, prescaler and high-frequency analog circuits can be designed to users' specifications using FUJITSU's standard macro cell technology.

This LSI series uses FUJITSU's latest wafer process technology for power-saving operation and master-slice semi-custom design to reduce lead times and lower costs. In addition, the ultra-compact flat package helps maintain circuit confidentiality, and contributes to lighter, more compact design by reducing the number of components.

The ASTRO MASTER IV is ideal for high-frequency applications, particularly mobile communication devices operating on digital specifications such as PCN, DECT, PHS and so on.

ASTRO: Advanced Semi-Custom Technology of Super PLL with RF System on LSI.

■ FEATURES

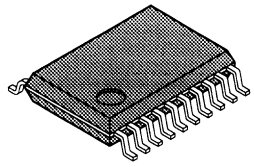
- PLL circuits can be customized for operating frequency, logical circuits, etc.
- High frequency analog circuits with adjustable resistance levels
- High speed operating capacity to 3.0 GHz
- On-chip low-current consumption and power-saving circuits
- On-chip high-speed lockup function
- Supply voltage: 2.7 V to 3.3 V (minimum operating voltage to 2.0 V min.)
- Development time (standard): approx. 10 weeks

■ LINEUP

Series	Prescaler	PLL	Analog circuits	Operating frequency	Package			Remarks
					SSOP	QFP	SQFP	
MB1560	1 circuit	1 circuit	2 circuits	3.0 GHz	20 34	—	—	For single PLL frequency synthesizers

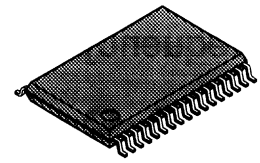
■ PACKAGE

20 pin Plastic SSOP



(FPT-20P-M03)

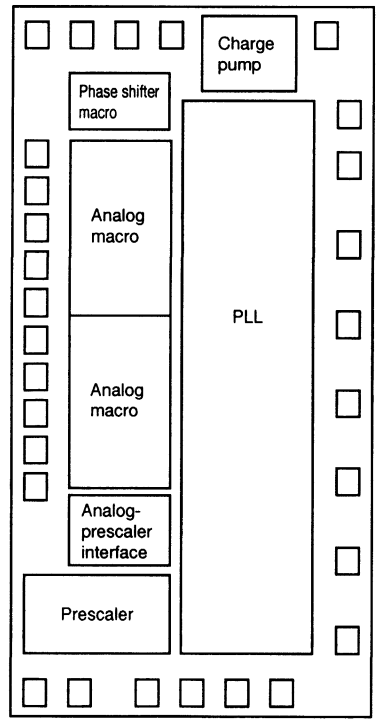
34 pin Plastic SSOP



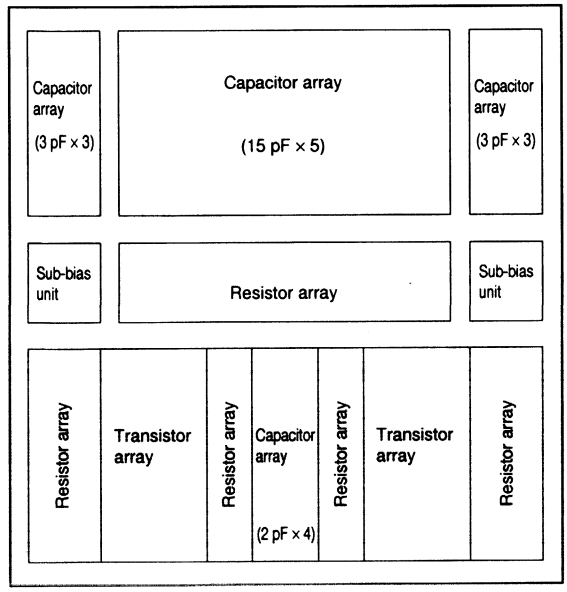
(FPT-34P-M03)

■ CHIP LAYOUT

- **MB1560 Series**



• **Analog Cell**


Capacitor array
(3 pF x 3)
Capacitor array
(15 pF x 5)
Capacitor array
(3 pF x 3)
Sub-bias unit
Resistor array
Sub-bias unit
Resistor array
Transistor array
Resistor array
Capacitor array
(2 pF x 4)
Resistor array
Transistor array
Resistor array

■ MACRO CELL DESCRIPTIONS

1. Prescaler

Divides the reference frequency by any given value and outputs the resulting frequency. Choice of two-modulus or fixed output mode.

2. PLL

- **Phase comparator**

The phase comparator has a phase detection range of -2π to $+2\pi$, and is designed to eliminate blind spots in phase comparison by output of a margin-of-error signal to the charge pump even when the phase difference is zero. Phase comparator characteristics can also be tuned to the polarity of VCO.

- **Counters**

The divide ratios of the comparator-side counter and reference-side counter can be either programmable or fixed.

- **Charge pump**

The "H" level output voltage from the charge pump is determined by power supply voltage. Charge pump characteristics for the sending and receiving systems can be optimized for each specific application.

For example, when FM modulation is applied directly to the VCO signal, charge pump characteristics can be adjusted for lower speeds in order to reduce the sensitivity of the synthesizer loop so that output does not track the modulation.

- **Analog switch**

When switching frequencies, the analog switch can be used to switch the capacitance of the low pass filter, to reduce the time constant in the filter and the load on the charge pump. This enables higher lock-up speed.

Switch control is synchronous with the LE signal, to that the analog switch is on when the LE signal is "high".

- **High speed lock-up circuit**

This circuit is specially designed for faster lock-up speeds.

- **Intermittent operation control circuit**

This on-chip power-saving function reduces circuit current flow in standby status, enabling devices to operate with less power demand. A special circuit is built in to prevent excessive error signal from increasing lock-up delay during the transition from power-saving mode to operating mode.

- **List of standard macro cells**

Type	Vcc	Icc	Operating frequency	Prescaler divide ratio (M)	Comparator counter divide ratio (N)	Swallow counter divide ratio (A)	Reference counter divide ratio (R)
PLL1	3 V	4 mA	1.1 GHz	64/65	16 to 2047	0 to 127	8 to 16383
PLL2		6 mA	2.0 GHz				

Crystal oscillator input frequency: Up to 32 MHz

Standby mode current demand: 100 μA

3. High Frequency Analog Cells

- **Mixer**

Active type double-balanced mixer

- **IF amplifier**

The IF amplifier is configured from a differential amplifier plus an NPN transistor using emitter-follower output from the differential amplifier.

- **RF amplifier**

Provides emitter-follower output of the output signal from the emitter-ground circuit. The RF input side can be connected to an internal bias circuit.

- **VCO**

Configured from an oscillator transistor in a base-ground Colpitts type oscillator circuit, plus a transistor acting as output buffer. Can be connected to external devices such as varicap or resonator.

- **Orthogonal modulator**

An orthogonal modulator is used for IF frequency modulation. In addition, a flip-flop type 90° phase shift circuit can be included in the configuration.

Note: Circuit format and other details can be adjusted to meet customer requirements.

■ CIRCUIT OPERATING DESCRIPTIONS

1. Intermittent Operation Control Circuit

The intermittent operation control circuit operates the LSI circuits during communication operations and at all other times places the chip in standby status to reduce power demand.

(1) Circuit operation in operating mode

All circuits are in operating status, and the chip performs normal PLL operations.

(2) Circuit operation in standby mode

All circuits that can be stopped without interfering with operation are shut down, and the chip goes into low-power operating mode.

Latch data:	Saves immediately preceding data
Shift register:	Data input enabled
Charge pump output:	High impedance
VCO input voltage:	Saves voltage level stored in low-pass filter during the last operating mode

<Caution> The digital system power supply must still be applied in standby mode.

2. Phase Lock Detection Circuit

To detect phase lock condition from the LD signal pin output, the T-bit should be selected. When the phase difference is greater than tw, the LD pin will output an L level signal, and when the difference is less than tw for 3 or more cycles, the output will change to H level. The length of the tw time interval can be set in the range of 625 ns to 1250 ns by connection to the crystal oscillator.

- **LD Signal operating status**

Operating status	PLL circuit	LD output
Standby mode	Standby	H
Operating mode	Un-lock	L
	Lock	H

3. High Speed Tuning Circuit

The following high speed tuning circuits are available for use according to specific applications.

- **High speed tuning circuits for ASTRO MASTER IV**

Function	Operation	Optimum applications
Analog switch	Circuit temporarily reduces LPF time constant at lock-up.	Analog portable phone devices (receiving system)
Turbo circuits	For broad-band steps, circuit forcibly switches charge pump on/off	PHS devices
Supercharger circuit	Circuit increases charge pump drive capacity	PHS devices
Hypercharger circuit	Circuit further enhances the drive capacity of the supercharger circuit	PDC, GSM etc.

■ SERIAL DATA

1. Data Bit Configuration

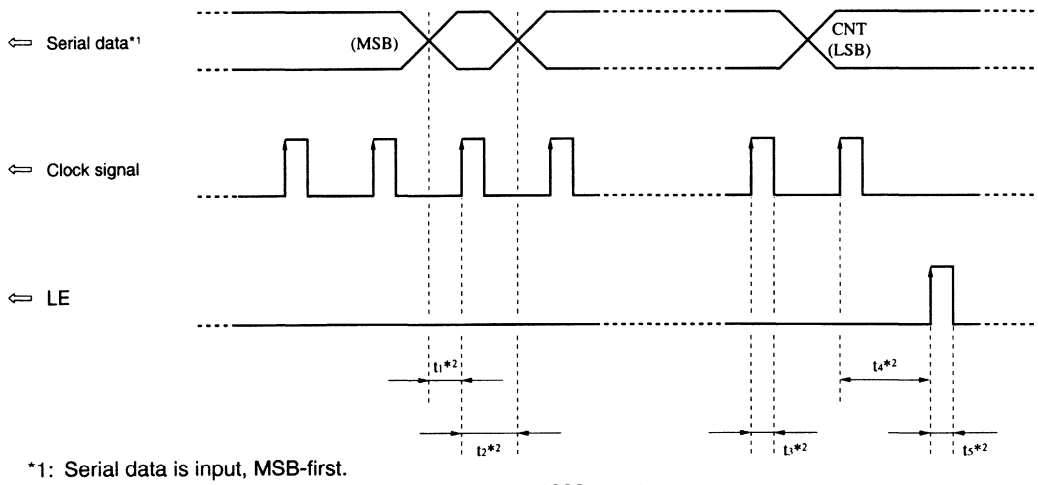
PLL operating settings are made through serial data input. The standard serial data format is shown in the table below. Serial data is entered MSB-first, and the data length is in the range of 22 to 37 bits.

- **Standard format for serial data**

Bit name (abbreviation)		Functional description	Standard bit count
Control bit (CNT bit)		Selects transfer destination (sending or receiving system)	1 to 2
LD select bit (T-bit)		Selects LD output	1 to 2
FC bit (F-bit)		Switches the phase of phase comparator	1
Programmable counter bit (N-bit)		Sets the programmable counter's divide ratio	11
Swallow counter bit (A-bit)		Sets the swallow counter's divide ratio	7
Reference counter bit (R-bit)	Fixed	Sets the reference counter's divide ratio	1 to 2
	Programmable		14

2. Serial Data Input Timing

After the serial data is stored in the shift register, it can be transferred to the latch circuit by means of the LE signal.



*1: Serial data is input, MSB-first.
*2: 100 ns ≤ t_1, t_4 300 ns ≤ t_3 800 ns ≤ t_5 1000 ns ≤ t_2

Notes:
- Data input utilizes the serial data, clock and LE signals at supply voltage or lower levels
- Shift register data is updated sequentially each time the clock signal is input. Data is synchronized with the rising edge of the clock signal, and is read sequentially into the shift register, MSB-first.
- After LSB input, the LE signal is changed from L level to H level.
- Shift register data is transferred to the latch circuit while the LE signal is at H level.
- Each input signal pin has a Schmitt trigger circuit to protect against abnormal operation due to noise.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min.	Max.	
Supply voltage*	V_{CC}	−0.5	+4.0	V
Input voltage*	V_{IN}	−0.5	V_{CC} + 0.5	V
Output current	I_{OUT}	−10	10	mA
Storage temperature	Tstg	−55	+125	°C

*: Voltage values are based on GND = 0 V.

Note: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Supply voltage*1	V_{CC}	2.7*2	—	3.3	V
	GND	—	0	—	V
Operating temperature	Ta	−40	—	+85	°C

*1: Voltage values are based on GND = 0 V
*2: Operation is assured to the minimum operating voltage level of 2.0 V min.

■ ANALOG CIRCUIT CHARACTERISTICS

Circuit	Parameter		Conditions	Value (typ.)	Unit
VCO	Supply voltage		—	3.0	V
	Current demand		—	11	mA
	Operating frequency		—	900	MHz
	C/N ratio		Offset frequency = 25 kHz, Band Width = 16 kHz	77	dB
	S/N ratio		BW = 0.3 to 3 kHz, 3 kHz/Dev	44	dB
	Output power		—	−2	dBm
	Conversion gain		—	6	MHz/V
Mixer	Supply voltage		—	3.0	V
	Current demand		—	12	mA
	Operating frequency	IF	—	800	MHz
		LO	P_{LO} = −10 dBm	110	MHz
		RF	$f_{RF} = f_{LO} + f_{IF}$	910	MHz
	Conversion gain		—	6	dB
	Maximum output power		—	−11	dBm
	1 dB compression point		Output level	−15	dBm
	Intercept point		Input level	−8	dBm
	NF		DSB measurement	12	dB
Amplifier	Supply voltage		—	3.0	V
	Current demand		—	6	mA
	Operating frequency		—	900	MHz
	Gain		f = 900 MHz (−30 dBm in)	14	dB
	Maximum output power		f = 900 MHz	−3	dBm
	1 dB compression point		f = 900 MHz, output level	−8	dBm
	Intercept point		f = 900 MHz, 900.1 MHz, input level	−12	dBm
	NF		f = 900 MHz	2.2	dB

(Continued)

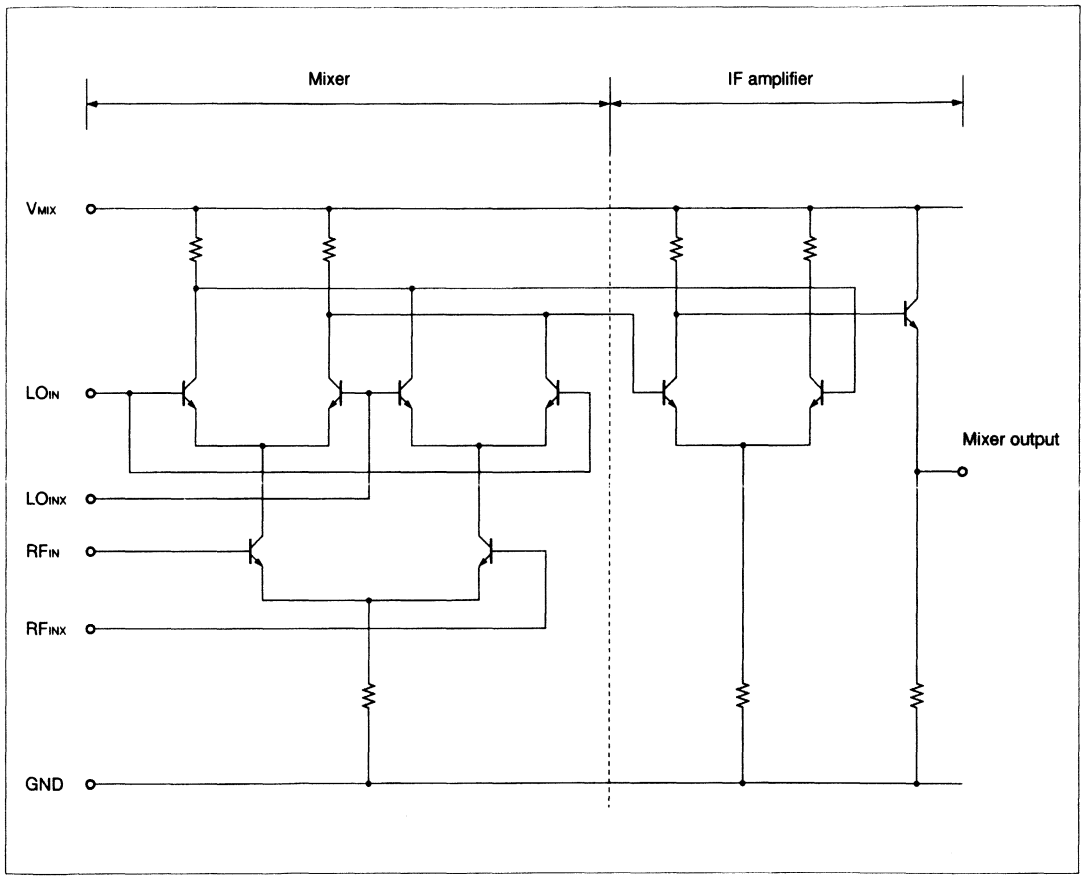
(Continued)

Circuit	Parameter		Conditions	Value (typ.)	Unit
Orthogonal modulator	Supply voltage		—	3.0	V
	Current demand		—	25	mA
	Operating frequency	LO1	P_{LO1} = −5 dBm	500	MHz
		LO2	P_{LO2} = −5 dBm	1650	MHz
		RF	$f_{RF} = f_{LO2} + f_{LO1}/2$	1900	MHz
	Output level		—	−14	dBm
	Modulator precision	Amplitude deviation	RMS Magnitude Error	1.9	%
		Phase deviation	RMS Phase Error	0.9	deg.
		Vector error	RMS Vector Error	2.4	%
	Carrier leak		—	−31	dBc

■ ANALOG SYSTEM: BASIC EQUIVALENT CIRCUITS

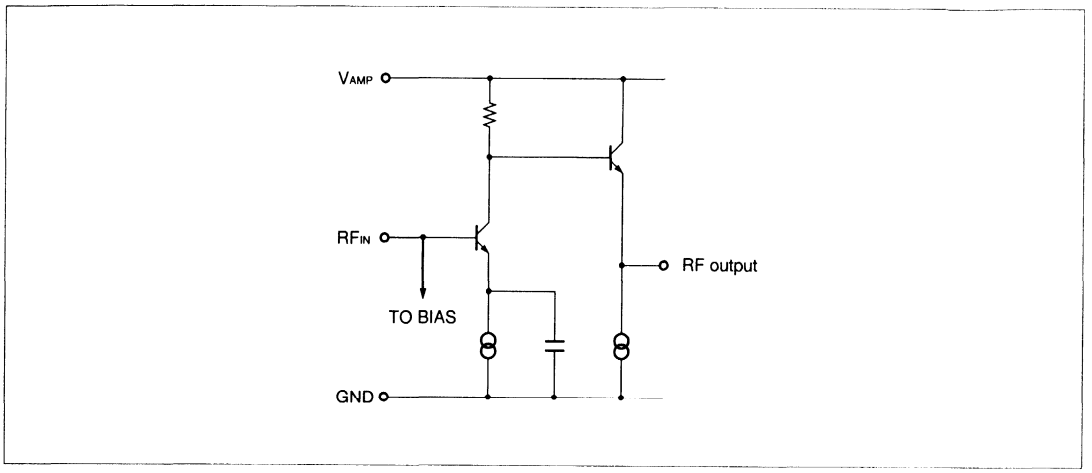
1. Mixer, IF Amplifier

The MB1560 series features an active-type double-balanced mixer. The LO and RF output can be connected to an internal bias circuit. The mixer output is connected through on-chip load resistor to the chip's power supply, and then to the next-stage IF amplifier. The IF amplifier is configured from a differential amplifier and NPN transistor, and provides emitter-follower differential amplifier output.



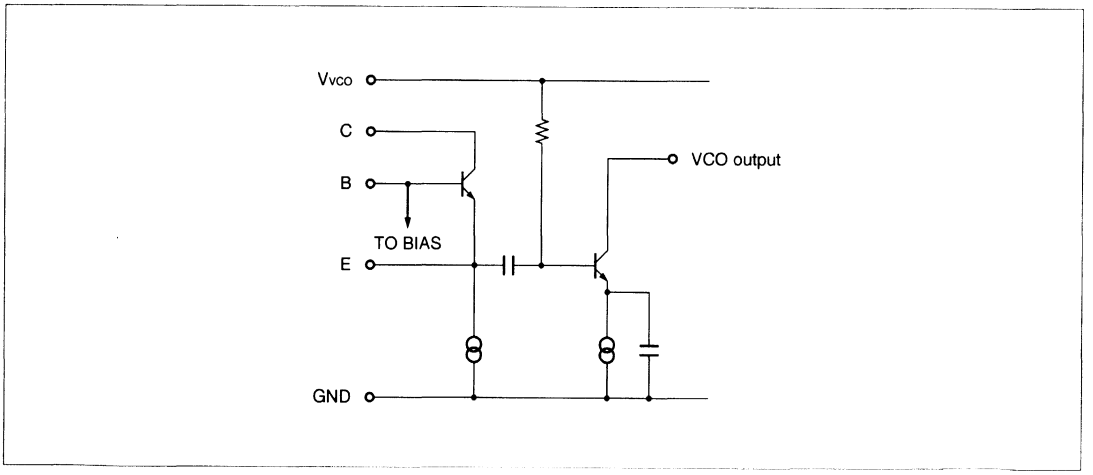
2. RF Amplifier

The emitter-ground circuit output signal is output as an emitter-follower signal. The RF input can be grounded to an internal bias circuit.



3. VCO Amplifier

The VCO amplifier is configured from an oscillator transistor in a base-ground Colpitts type oscillator circuit, plus a transistor acting as output buffer. The VCO amplifier can be connected to external devices such as varicap or resonator.



■ DEVELOPMENT PROCESSES

Each product in the ASTRO MASTER IV series is developed through the following processes, based on requirements and specifications supplied by the customer.

1. Feasibility Study

(1) Product specifications and development process study

FUJITSU conducts simulations based on documentation provided by the customer, in order to evaluate the technical and economic feasibility of each proposed design.

Product Documentation
- Technical documentation: Functional descriptions, I/O signal descriptions, block diagrams.
- Characteristics documentation: For prescalers, PLL, VCO, mixers, amplifiers, etc.

Development Documentation
- Delivery schedule documentation: Development schedule, division of responsibilities, etc.
- Cost estimates: Volume requirements, development costs, target prices

(2) Product feasibility evaluation

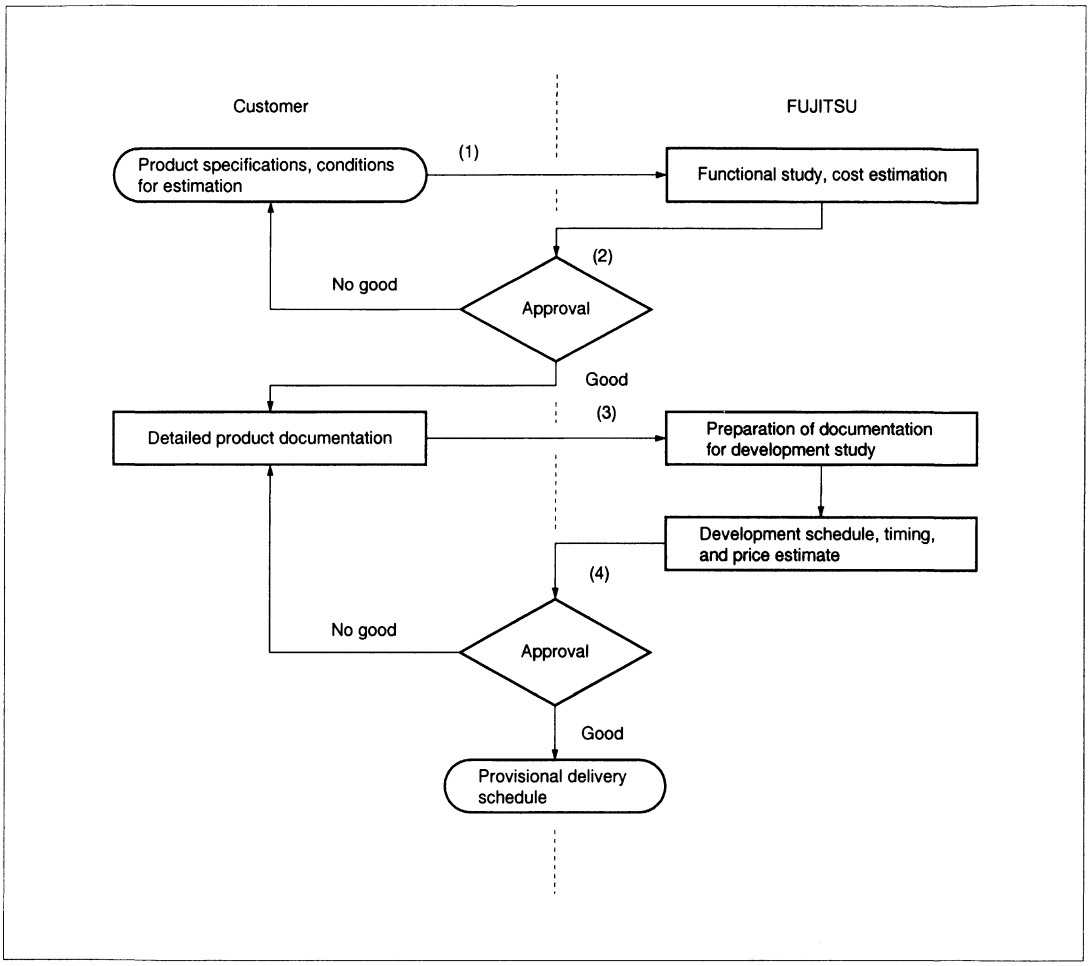
Based on the foregoing studies, FUJITSU and the customer meet to evaluate feasibility.

(3) Development of planned specifications

Circuit functions and characteristics are studied in detail, and circuit specifications and testing specifications are developed. After specifications have been determined, final estimates of the development schedule, timing and cost, and the product price can be produced.

(4) Approval of provisional delivery specifications

After FUJITSU and the customer have determined the feasibility of product development, a provisional delivery schedule is agreed upon.


Customer
FUJITSU
Product specifications, conditions for estimation
(1)
Functional study, cost estimation
(2)
No good
Approval
Good
Detailed product documentation
(3)
Preparation of documentation for development study
Development schedule, timing, and price estimate
(4)
No good
Approval
Good
Provisional delivery schedule

2. LSI Development

(1) LSI design, prototype development

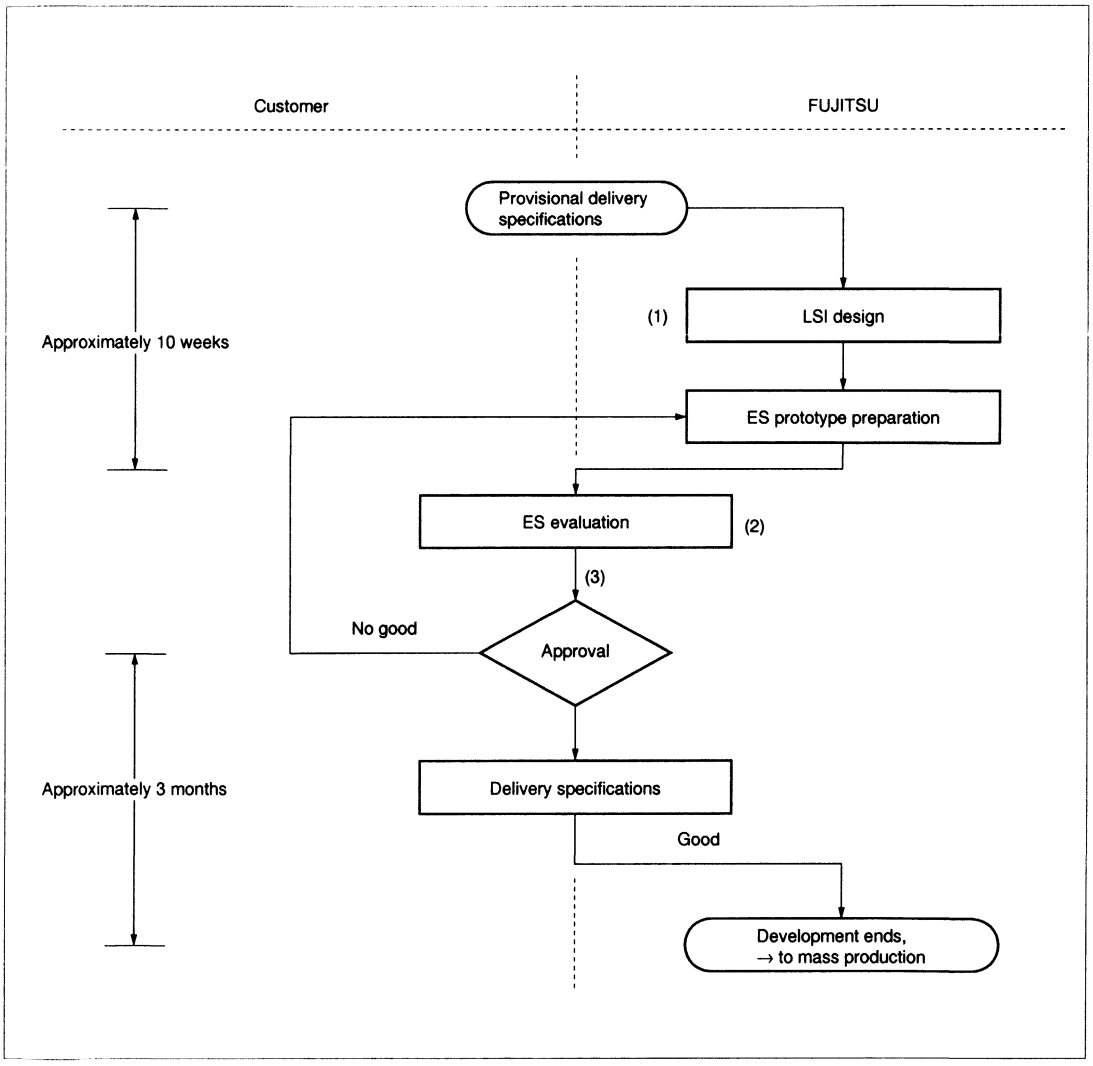
Based on the provisional delivery specifications agreed by the customer and FUJITSU, chip design and prototype work begins. The standard time required for an ES prototype is approximately 10 weeks from the approval of provisional delivery specifications.

(2) ES (engineering sample) evaluation

Both the customer and FUJITSU evaluate the ES prototype based on the provisional delivery specifications.

(3) Final approval

If there are no problems with the evaluation, FUJITSU and the customer agree on final delivery specifications and end development, moving to the mass production stage. The standard lead time for delivery of mass production products is approximately three months.



■ ORDERING INFORMATION

Part number	Package	Remarks
MB156XPFV	20 pin Plastic SSOP (FPT-20P-M03)	
MB156XPFV	34 pin Plastic SSOP (FPT-34P-M03)	

FUJITSU SEMICONDUCTOR
DATA SHEET

DS06-80101-1E

ASSP
IF Band PLL Frequency Synthesizer

MB15S00 Series

■ DESCRIPTION

The Fujitsu MB15S series is an exclusive Intermediate Frequency (IF) band Phase Locked Loop (PLL) frequency synthesizer with pulse swallow operation. It can operate maximum at 300MHz.

The reference divider and comparison divider have fixed divide ratios, so that it is not required to set the divide ratios by a µcontroller externally. Because the dividers are designed by means of **MASK ROM** method, a customer can chose them optionally. SOP and **SSOP 8-pin** plastic packages are available.

All of the above features help a system designer for **easier** as well as **compact** layout work.

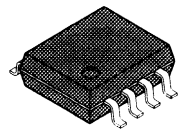
It operates with a supply voltage of 3.0V typ. and dissipates 3.5 mA typ. current realized through the use of Fujitsu's Bi-CMOS technology.

■ FEATURES

- Operating frequency : 300MHz max.
- Low power supply current: I_{CC} (total) = 3.5 mA typ. (V_{CC} = 3V)
- Pulse swallow function;
  300MHz Prescaler: 16/17 or 32/33
- MASK ROM optional the comparison and reference dividers:
  - Main counter ; 5 to 4,095
  - Swallow counter ; 0 to 31
  - Reference counter ; 5 to 4,095
- Charge pump options:
  - Analog cellular phones ; Low sensitivity charge pump for direct modulation.
  - Digital cellular phones ; Super charger circuit for High speed tuning.
- Low power supply voltage: V_{CC} = 2.7 to 3.6V
- Wide operating temperature: Ta = –40 to 85°C
- Plastic 8-pin SOP and 8-pin SSOP packages

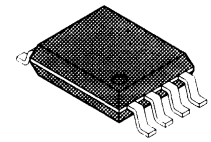
■ PACKAGES

8-pin, Plastic SOP



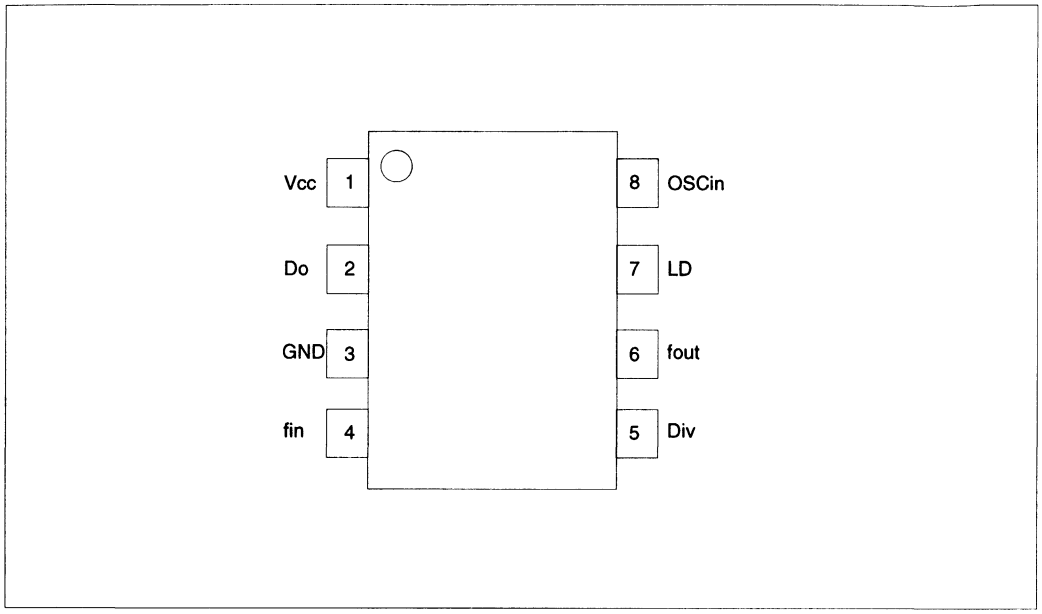
(FPT-8P-M01)

8-pin, Plastic SSOP



(FPT-8P-M03)

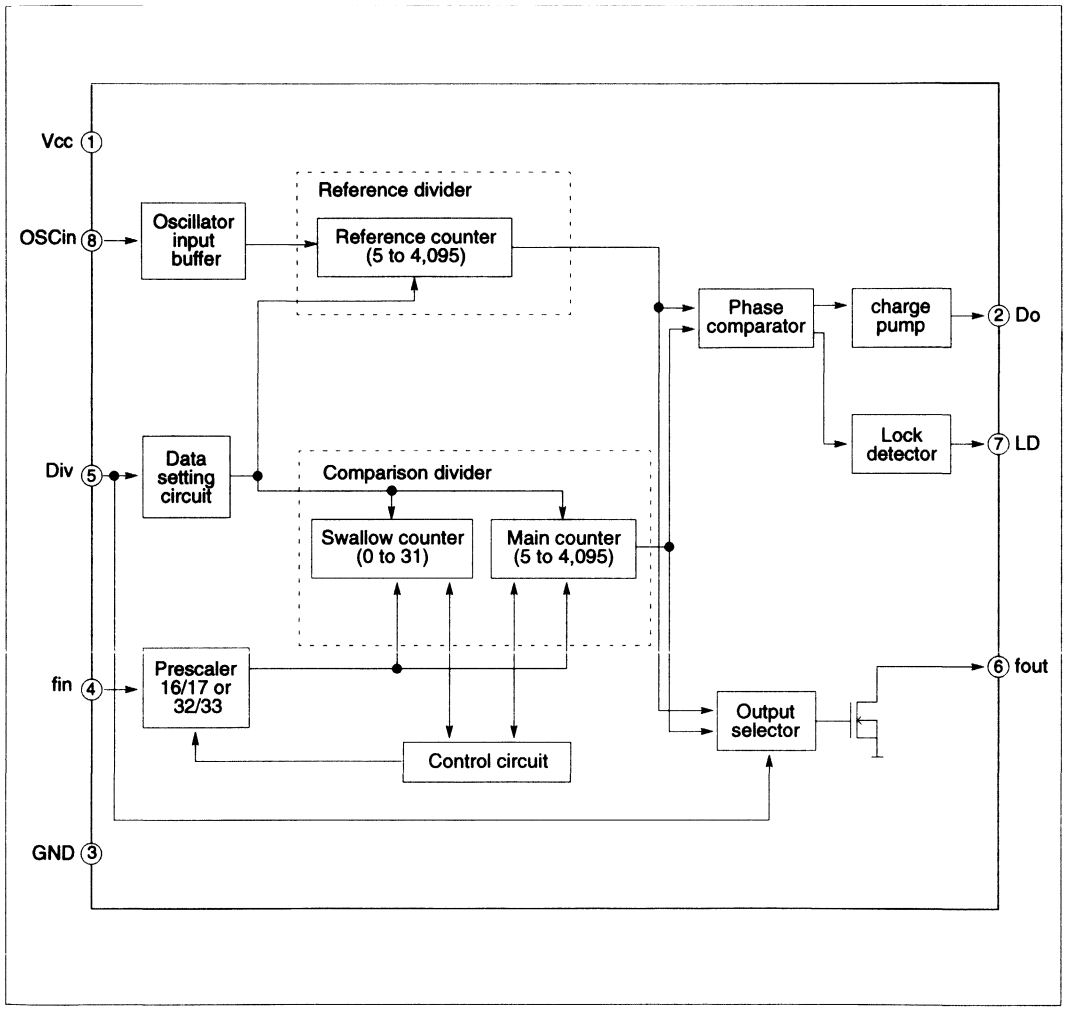
■ PIN ASSIGNMENT



■ PIN DESCRIPTIONS

Pin No.	Pin name	Description
1	Vcc	Power supply voltage input.
2	Do	Charge pump output.
3	GND	Ground.
4	fin	Prescaler input. Connection should be with AC coupling.
5	Div	Divide ratio switching input. Two kinds of divide ratios are selectable by Div input "H" or "L".
6	fout	Test purpose output. This pin is an open drain output so that should be left open usually.
7	LD	Lock detector output.
8	OSCin	Reference counter input. Connection should be with AC coupling.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{CC}	–0.5 to +5.0	V
Inputt voltage	V_I	–0.5 to V_{CC} + 0.5	V
Output voltage	V_{OUT}	–0.5 to V_{CC} +0.5	V
Output current	I_{OUT}	0 to 5	mA
Storage tempareture	T_{STG}	–55 to +125	°C

Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Note
		Min	Typ	Max		
Power supply voltage	V_{CC}	2.7	3.0	3.6	V	
Input voltage	V_{IN}	GND	–	V_{CC}	V	
Operating temperature	Ta	–40	–	+85	°C	

Handling Precautions

- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover workbenches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

■ ELECTRICAL CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Power supply current	I_{CC}	PLL is locked. Vcc = 3.0V, Ta = 25°C	–	3.5	5.0	mA
Operating frequency	fin	AC coupling by 1000pF capacitor	50	–	300	MHz
Oscillator input frequency	fosc	AC coupling by 1000pF capacitor	–	12	23	MHz
Input sensitivity	Vin	AC coupling by 1000pF capacitor	–10	–	+2	dBm
Oscillator input sensivity	OSCin	AC coupling by 1000pF capacitor	0.5	–	–	Vpp
Input voltage (Div)	V_{IH}		$V_{CC} \times 0.7$	–	–	V
	V_{IL}		–	–	$V_{CC} \times 0.3$	V
Input current (Div)	I_{IH}		–	–	1.0	µA
	I_{IL}		–1.0	–	–	µA
Input current (OSCin)	I_{OSC}		–100		100	µA
Output voltage	V_{OH}	V_{CC} = 3.0V	2.6	–	–	V
	V_{OL}	V_{CC} = 3.0V	–	–	0.4	V
High impedance cut off current (Do)	I_{OFF}	$V_{DO} \leq 3.3V$	–	–	1.1	µA

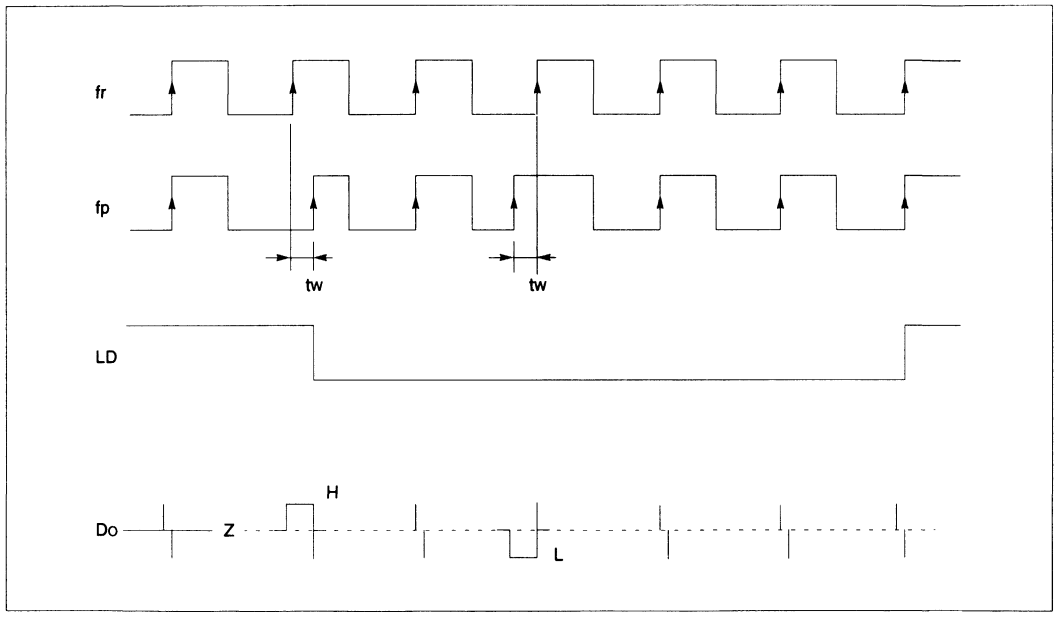
■ FUNCTIONAL DESCRIPTIONS

Divide ratios of the internal counters can be set optionally according to customer requirements. Two different frequencies can be selected by Div input "H" or "L".
The divide ratio can be calculated using the following equation:

$f_{VCO} = \{(P \times N) + A\} \times f_{OSC} \div R \quad (A < N)$

f_{VCO}: Output frequency of external voltage controlled ocillator (VCO: up to 300MHz)
P: Preset divide ratio of dual modulus prescaler (16/17 or 32/33)
N: Divide ratio of the main counter (5 to 4,095)
A: Divide ratio of the swallow counter (0 to 31)
f_{OSC}: Reference oscillation frequency (up to 23MHz)
R: Divide ratio of the reference counter (5 to 4,095)

■ PHASE DETECTOR TIME CHART

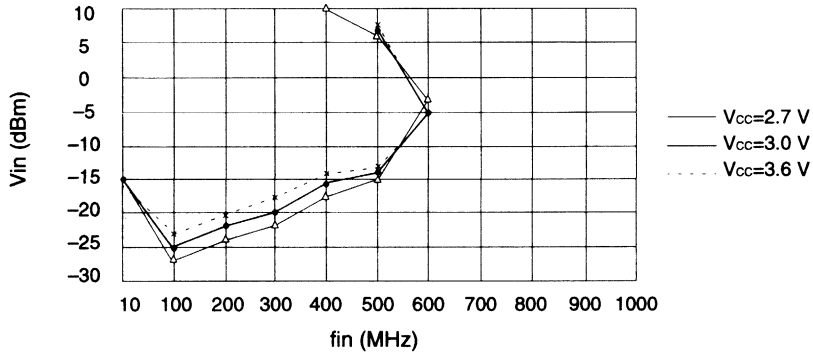


Note: • Phase defference detection range = -2π to $+ 2\pi$
• Spikes on Do pulse during locking state are output to prevent dead zone.
• LD output becomes low when phase difference is tw or more.
• LD output becomes high when phase difference is tw or less and continues to be so for three cycles or more.
• tw depends on OSCin input frequency.
(e.g. tW635ns to 1250ns when foscin = 12.8 MHz)

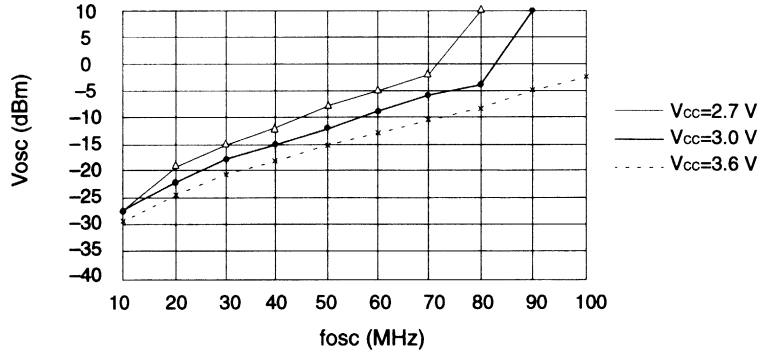
■ TYPICAL CHARACTERISTICS

Prescaler Input Sensitivity Characteristics

• **fin Pin**



• **OSCin Pin**



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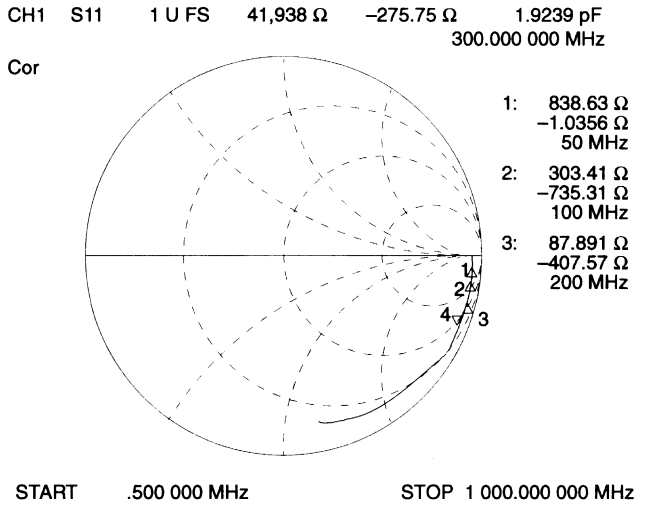
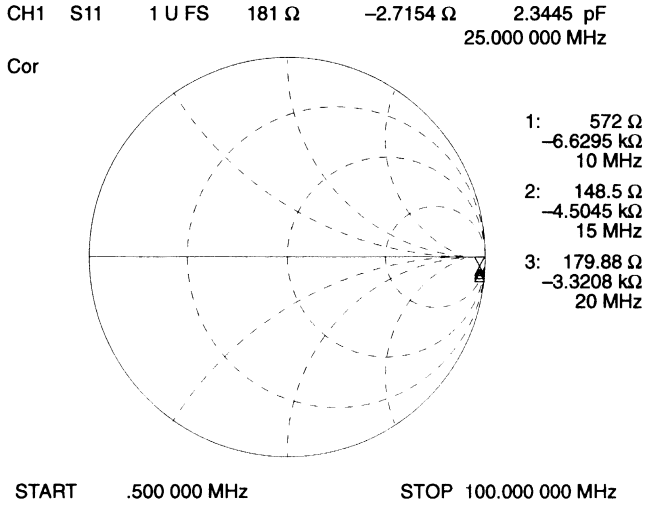
Input/Output Impedance Characteristics

- **fin Pin**



- **OSCin Pin**



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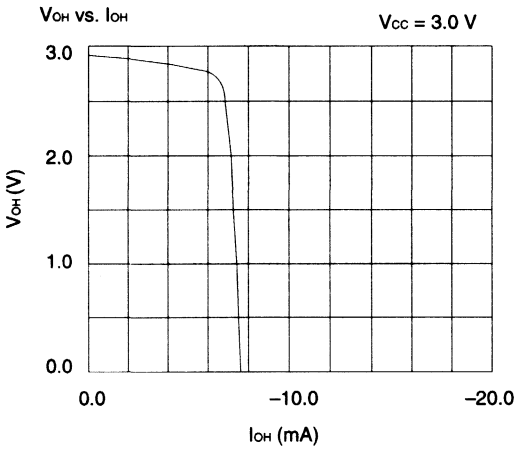
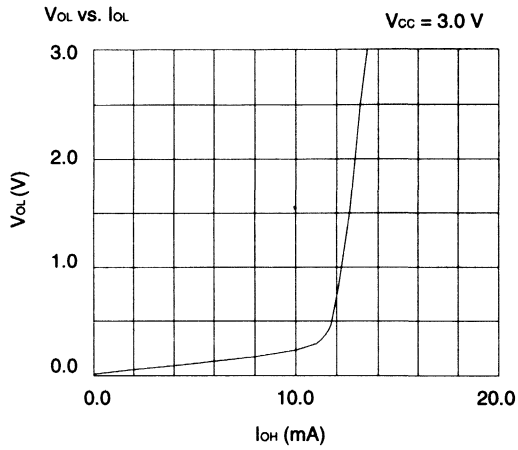
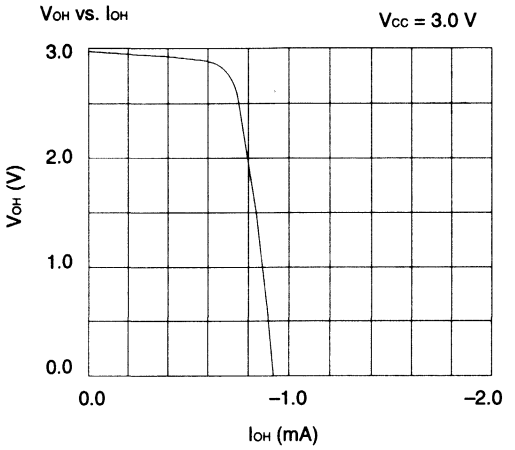
Charge Pump Characteristics

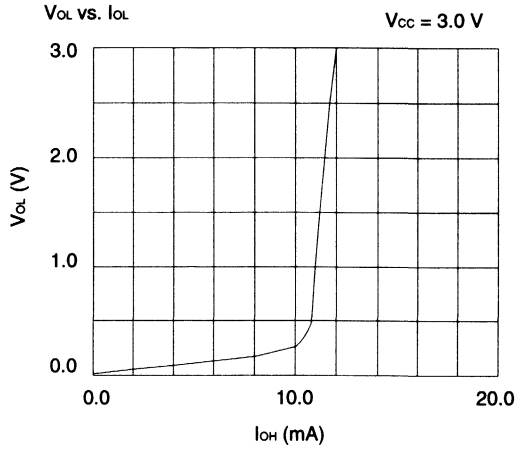
• Super charger





• Low sensitivity type



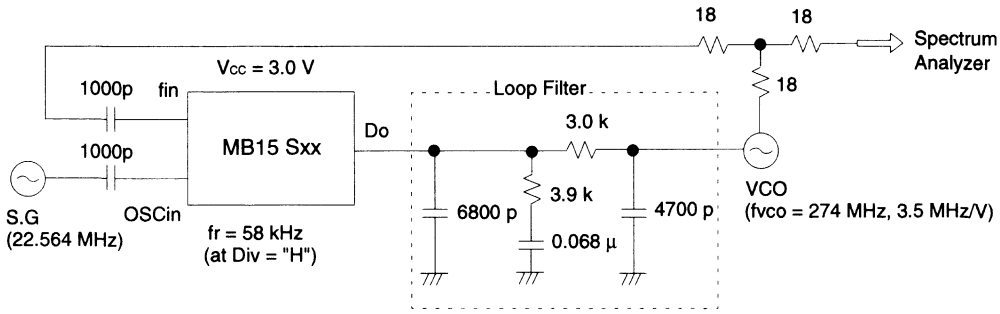


(Continued)

PLL Loop Characteristics (Super Charger)

Parameter	Results
Hoppint time +/– 1 kHz Unlock → Lock Power on → Lock	1.80 ms < 4.50 ms
Suprious Δ f = 58 kHz	–87.0 dBc
Phase noise C/N peak in BW	–82.0 dBc/Hz
Vcc (V)	3.0V
VCO	Discrete VCO (Kv = 3.5 MHz/V) Lock frequency = 274.0 MHz (fr = 58 kHz)

Measurement Circuit



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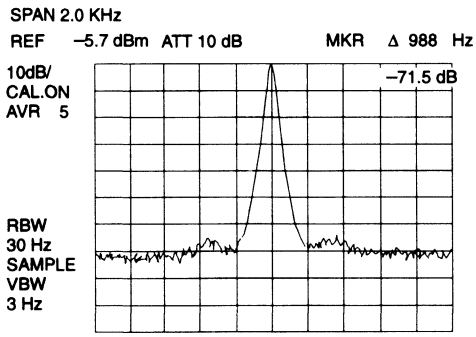
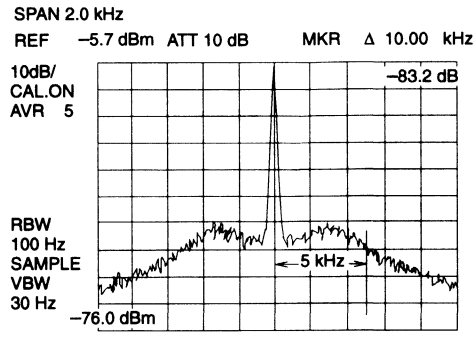
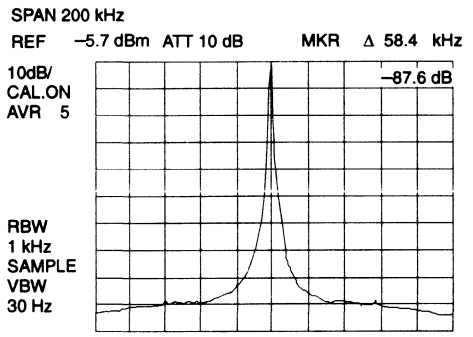
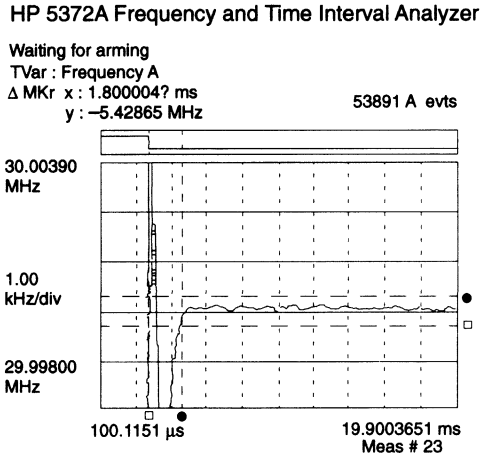
PLL Phase Noise/Suprious







PLL Lock-up Time (unlock→ lock)



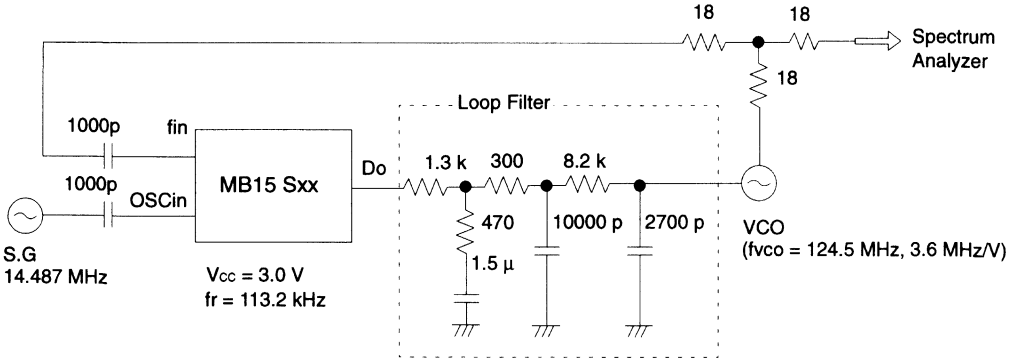
(Continued)

(Continued)

PLL Loop Characteristics (Low Sensitivity Type)

Parameter	Results
Hoppint time +/– 1 kHz Power on → Lock	8.6 ms
Suprious (Δ f = 113.2 kHz)	–86.7 dBc
Phase noise (Δ f = 1 kHz)	–79.0 dBc/Hz
V_{CC} (V)	3.0 v
VCO	Discrete VCO (Kv = 3.6 MHz/V) Lock frequency = 124.5 MHz (fr = 113.2 kHz)

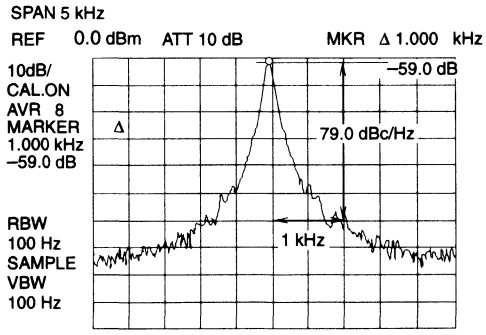
Measurement Circuit

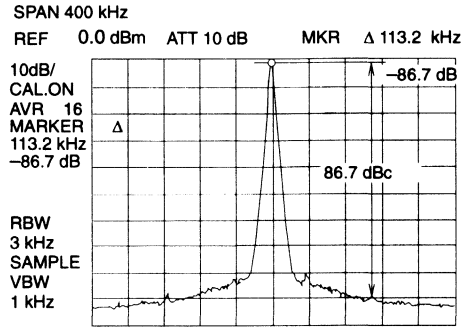


(Continued)

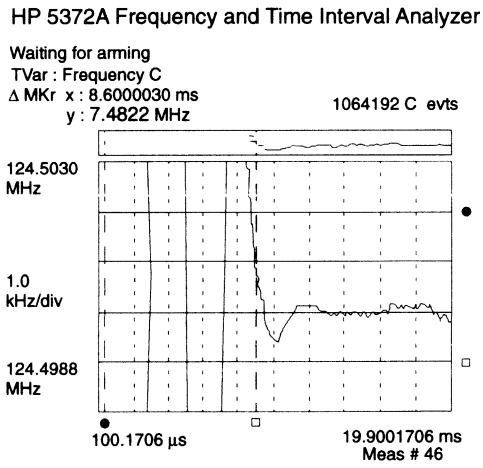
(Continued)

PLL Phase Noise/Suprious

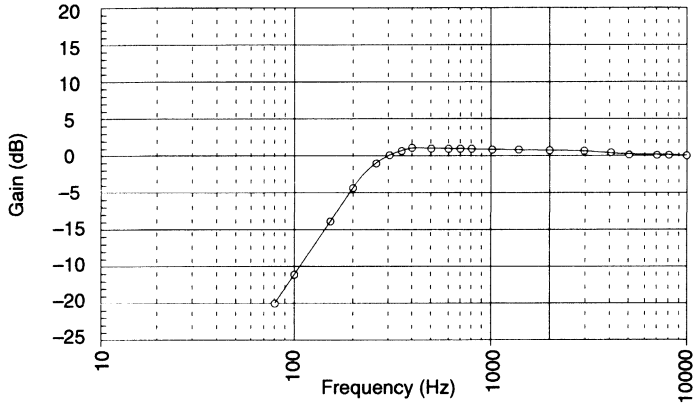




PLL Lock-up Time

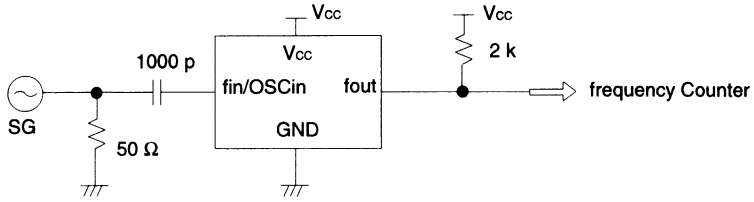


Modulation Characteristics



■ TEST CIRCUIT EXAMPLE (fin/OSCin Input Sensitivity Measurement)

Measurement Circuit



■ CUSTOMER REQUESTING SPECIFICATIONS

Prameter			Option	Requirements
fvco		VCO output frequency	~ 300MHz fvco = {(P x N) + A} x fr	
fosc		Reference oscillation frequency	~ 23MHz fosc = R x fr	
Comparison divider	N	Main counter divide ratio	5 to 4,095	
	A	Swallow counter divide ratio	0 to 31	
Reference divider	R	Reference counter divide ratio	5 to 4,095	
	fr	Reference frequency	Option	
P		Prescaler divide ratio	16/17 or 32/33	
Charge pump type			Low sensitivity type or super charger	
Package			SSOP 8-pin or SOP 8-pin	
ES request date/qty.			Typically 6 weeks from spec. fix to the first ES.	
CS request date/qty.			–	
MP request date/qty.			–	
Target price			–	
Customer comments				

MEMO

FUJITSU SEMICONDUCTOR
DATA SHEET

DS04–21703–3E

ASSP

Piezo Electric VCO

M2 Series (D110)

VOLTAGE CONTROLLED OSCILLATOR (4 to 30 MHz)

DESCRIPTION

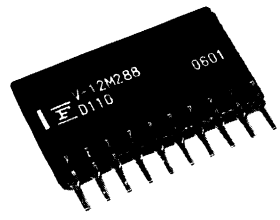
The M2 series (D110) Voltage Controlled Oscillators (VCO) directly oscillate in the frequency range of 4 to 30 MHz. The M2 series VCO use a piezoelectric single crystal with high electromechanical coupling coefficient (LiTaO3: lithium tantalate) for stable and wide variable frequency width.

Excellent S/N and jitter characteristic due to high Q of lithium tantalate can realize high quality playback sound and picture, especially in PLL circuit of digital audio and video equipments.

FEATURES

- Wider variable frequency width than quarts crystals: ±0.2% or more
- High stability (100 times more stable than LC or TTL-IC VCO)
- Excellent S/N and jitter characteristic due to high Q of lithium tantalate for high quality playback sound and picture.
- Excellent temperature characteristic: −300~500ppm (−10~+70°C)
- 10-pin SIP ready for high-density mounting.

PACKAGE

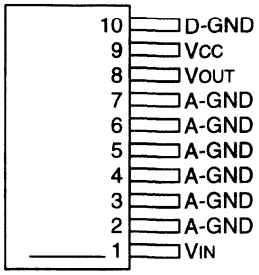


TERMINAL ASSIGNMENT

Terminal No.	Terminal Name	Description
1	VIN	Control voltage input terminal
2,3,4,5,6,7	A-GND	Analog grounding terminal
8	VOUT	Output terminal
9	VCC	Power supply terminal
10	D-GND	Digital grounding terminal

Note: The GND terminals are not connected inside the module. Be sure to route them on the PC board.

(Front view)



MAXIMUM RATINGS

Item	Symbol	Rated value	Unit
Power supply voltage	VCC	–0.5~+7.0	V
Input control voltage	VIN	–0.5~+10.0	
Power consumption	PD	100	mW
Operating temperature	Ta	–10~+70	°C
Storage temperature	Tstg	–30~+100	
Oscillation frequency range	——	4~30	MHz

RECOMMENDED OPERATING CONDITIONS

Item	Symbol	Rated value	Unit
Power supply voltage	VCC	4.75~5.25	V
Input control voltage	VIN	0~5	
Operating temperature	Ta	–10~+60	°C

STANDARD FREQUENCIES

Frequencies	Uses	Part number	Frequencies	Uses	Part number
12.288 MHz	Audio	FAR–M2SC–12M288–D110	17.734 MHz	Video	FAR–M2SC–17M734–D110
13.500 MHz	Video	FAR–M2SC–13M500–D110	22.579 MHz	Audio	FAR–M2SC–22M579–D110
14.318 MHz	Video	FAR–M2SC–14M318–D110	24.576 MHz	Audio	FAR–M2SC–24M576–D110
16.934 MHz	Audio	FAR–M2SC–16M934–D110	28.636 MHz	Video	FAR–M2SC–28M636–D110

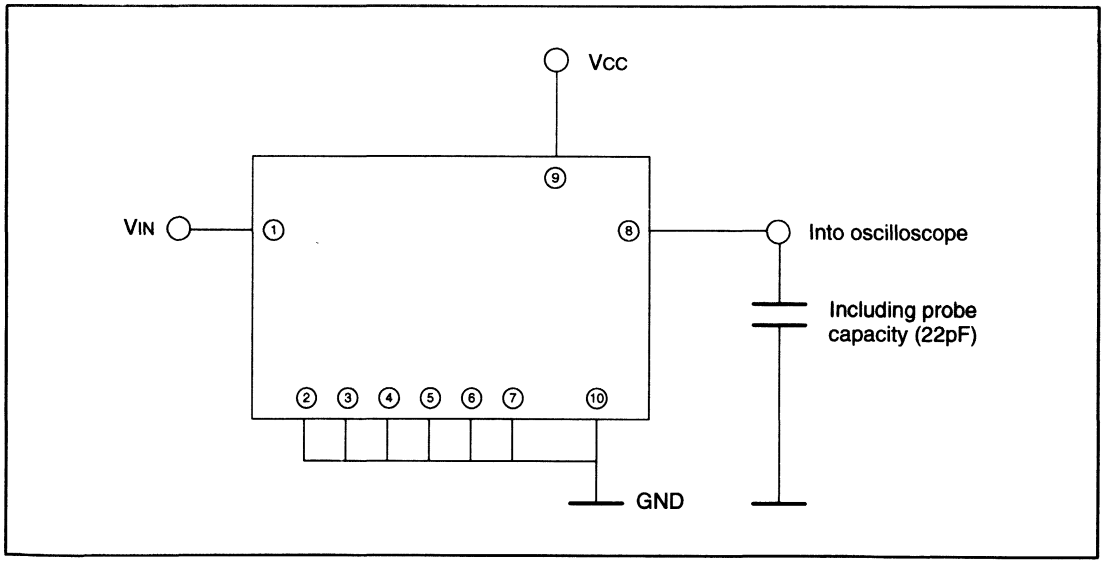
ELECTRICAL CHARACTERISTICS

(Vcc = 5.0V)

Item		Symbol	Condition	Rated value			Unit	
				minimum	standard	maximum		
Power supply current		Icc	Not loaded	–	10	15	mA	
Oscillation frequency		fH	VIN = 5.0V	+2000	–	–	ppm	
		f1	VIN = 0V	–	–	–2000		
Output voltage	H level	VOH	VIN = 2.5V	Vcc–0.5	5.0	–	V	
	L level	VOL	VIN = 2.5V	–	0	0.5		
Frequency voltage stability		Δf (Vcc)	Vcc = 4.75~5.25V	–100	–	+100	ppm	* 1
Frequency temperature stability		Δf (Ta)	VIN = 2.5V	–300	–	+500		* 2

* 1 : Vcc = 5.0V standard
* 2 : 25°C standard, Ta = –10~+70°C

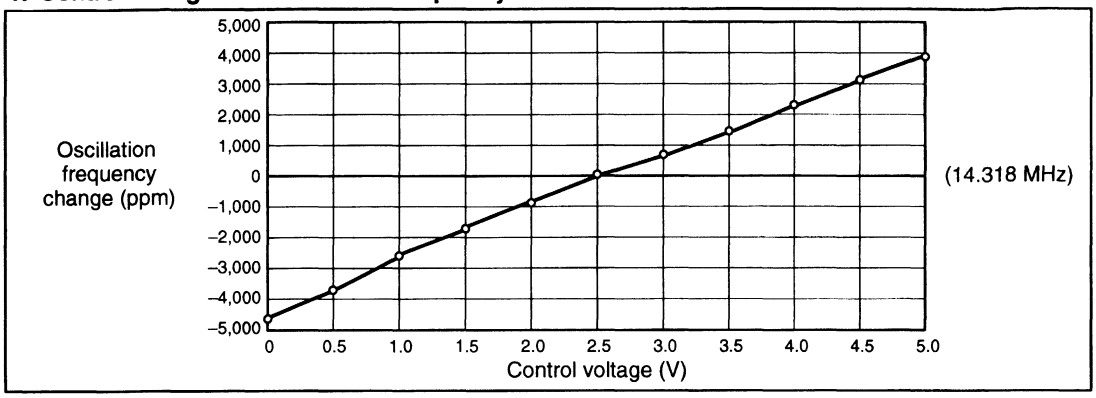
MEASURING CIRCUIT DIAGRAM



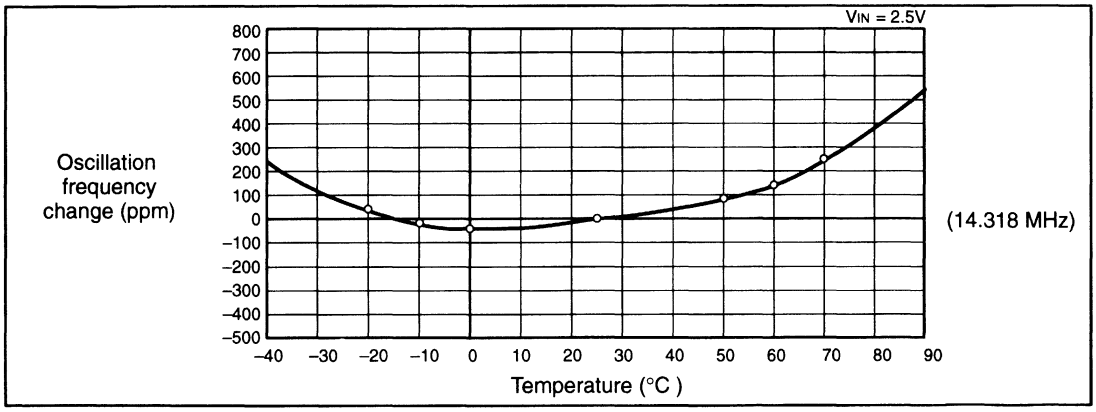
STANDARD CHARACTERISTICS

Part number : FAR–M2SC–14M318–D110

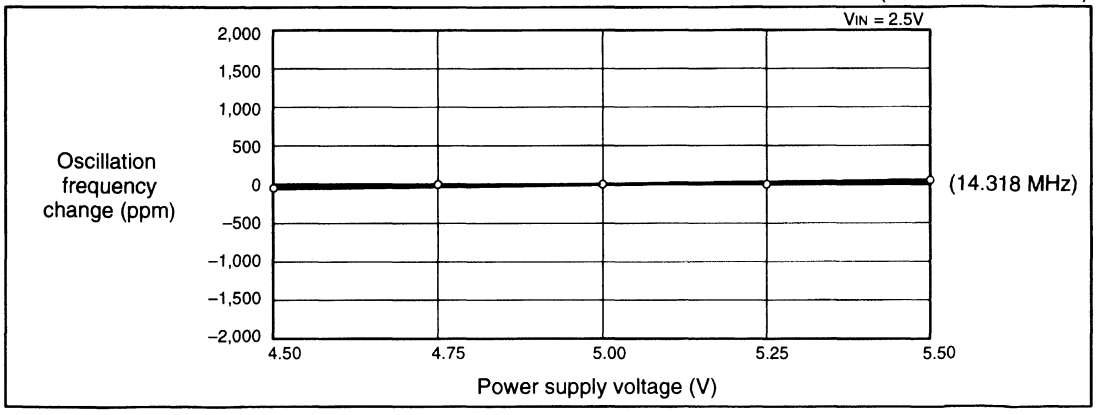
1. Control voltage and oscillation frequency



2. Temperature characteristics (25°C standard)



3. Power supply voltage characteristics (Vcc = 5.0V standard)



PART NUMBER SYSTEM

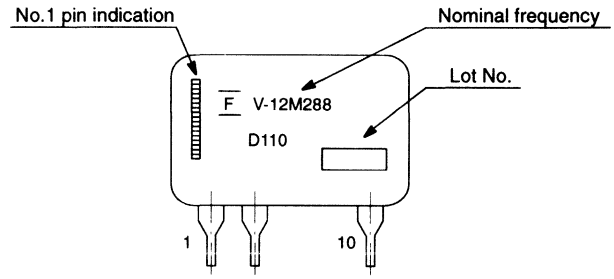
[Part number example]

FAR-M2SC- □□□□□□ -D □□□
① ②

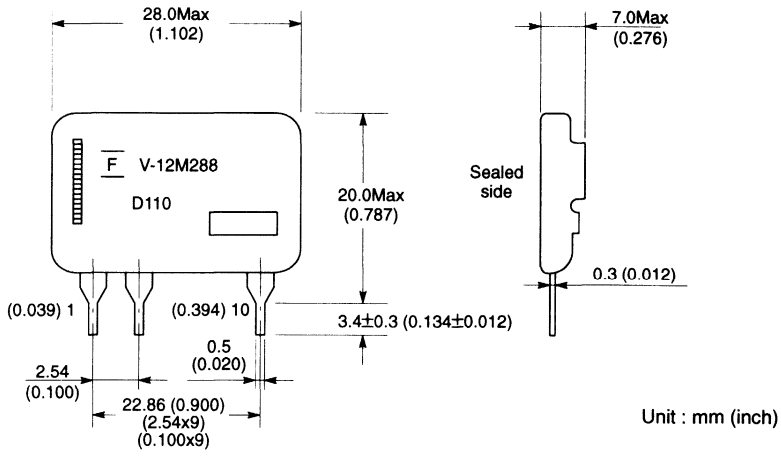
① Frequency designation : Nominal frequency in six alphanumeric characters.
M indicates the decimal point in MHz.
(Example) 14.318 MHz 14M318

② Serial No. : 110~119 (standard : 110)

MARKING



DIMENSION



MEMO

FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-23900-3E

ASSP

PIEZOELECTRIC SAW FILTERS

F5 SERIES

SAW BANDPASS FILTER (700 to 1000 MHz)

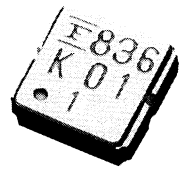
DESCRIPTION

The F5 series are wideband bandpass filters for use in the 700MHz to 1000MHz range. The F5 series uses a single lithium tantalate piezoelectric crystal ($LiTaO_3$) that has large electromechanical coupling coefficient. That prorides wide bandwidths and exceptional stability. Our exclusive mounting technique makes the F5 series very compact and surface mountable. The F5 series is most suitable for use in handheld phones.

FEATURES

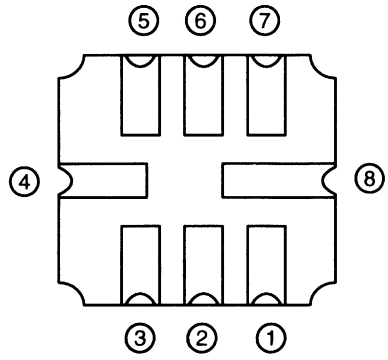
- Considerably smaller and lighter than the dielectric filter (Volume and weight are reduced by 1/30.)
- Surface mount package (SMT)
- Wide variety of bandwidths for world wide system (AMPS, ADC, ETACS, NMT, GSM, NTT, NTACS)
- Low insertion loss
- High power rating: 0.2 W guaranteed

PACKAGE



PIN ASSIGNMENT

(BOTTOM VIEW)



Pin no.	Pin name	Description
1	GND	Ground pin
2	IN	Input pin
3	GND	Ground pin
4	GND	Ground pin
5	GND	Ground pin
6	OUT	Output pin
7	GND	Ground pin
8	GND	Ground pin

MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Operating temperature	T_a	–30 to 70	°C
Storage temperature	T_{stg}	–40 to 100	°C
Maximum input level	P_{in}	200	mW
Frequency range		700 to 1000	MHz

RECOMMENDED OPERATING CONDITIONS

Item	Symbol	Rating	Unit
Operating temperature	T_a	–30 to 70	°C

PART NUMBERS

Tx : For Transmitter
Rx : For Receiver

No.	Part Number	System	Use	Center Frequency (MHz)	Bandwidth (MHz)	Remarks
1	FAR–F5CB–836M50–G201	AMPS/ADC	Tx	836.5	25	
2	FAR–F5CB–881M50–G201	AMPS/ADC	Rx	881.5	25	
3	FAR–F5CB–888M50–G201	ETACS	Tx	888.5	33	
4	FAR–F5CB–933M50–G202	ETACS	Rx	933.5	33	
5	FAR–F5CB–902M50–G201	NMT/GSM	Tx	902.5	25	
6	FAR–F5CB–947M50–G201	NMT/GSM	Rx	947.5	25	
7	FAR–F5CB–911M50–G201	NTACS	Tx	911.5	27	
8	FAR–F5CB–856M50–G201	NTACS	Rx	856.5	27	
9	FAR–F5CB–933M50–G201	NTT	Tx	933.5	17	
10	FAR–F5CB–878M50–G201	NTT	Rx	878.5	17	

ELECTRIC CHARACTERISTICS

1. AMPS/ADC type (Tx)

Part number: FAR-F5CB-836M50-G201 T_a=–3 to 70°C

Item	Symbol	Condition	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	824 to 849MHz	—	3.5	4.2	dB	
In-band ripple		824 to 849MHz	—	1.0	1.5	dB	
Stopband attenuation		DC to 800MHz	20	25	—	dB	
		869 to 894MHz	20	25	—	dB	
		894 to 3000MHz	15	20	—	dB	
In-band VSWR		824 to 849MHz	—	1.7	2.0		
Matching constants	C_1			7		pF	
	L_1			9		nH	
	C_2			6		pF	
	L_2			11		nH	

2. AMPS/ADC type (Rx)

Part number: FAR-F5CB-881M50-G201 T_a=–30 to 70°C

Item	Symbol	Condition	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	869 to 894MHz	—	—	4.5	dB	
In-band ripple		824 to 849MHz	—	—	1.5	dB	
Stopband attenuation		DC to 849MHz	20	—	—	dB	
		914 to 939MHz	18	—	—	dB	
		947 to 1049MHz	30	—	—	dB	
		1049 to 3000MHz	15	—	—	dB	
In-band VSWR		869 to 894MHz	—	1.8	2.0		
Matching constants	C_1			6		pF	
	L_1			7		nH	
	C_2			7		pF	
	L_2			9		nH	

*: To be determined

3. ETACS type (Tx)

Part number: FAR-F5CB-888M50-G201

T_a=–30 to 70°C

Item	Symbol	Condition	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	872 to 900MHz	—	4.5	5.0	dB	
		900 to 905MHz	—	5.5	6.5	dB	
In-band ripple		872 to 905MHz	—	—	2.5	dB	
Stopband attenuation		DC to 847MHz	20	25	—	dB	
		847 to 860MHz	8	12	—	dB	
		917 to 920MHz	10	13	—	dB	
		920 to 922MHz	13	15	—	dB	
		922 to 950MHz	20	23	—	dB	
		962 to 995MHz	30	33	—	dB	
		995 to 3000MHz	15	20	—	dB	
In-band VSWR		872 to 905MHz	—	2.0	2.5		
Matching constants	C_1			7		pF	
	L_1			7		nH	
	C_2			6		pF	
	L_2			9		nH	

4. ETACS type (Rx)

Part number: FAR-F5CB-933M50-G202

T_a=–30 to 70°C

Item	Symbol	Condition	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	917 to 947MHz	—	4.5	5.0	dB	
		947 to 950MHz	—	5.5	6.5	dB	
In-band ripple		917 to 950MHz	—	1.0	2.5	dB	
Stopband attenuation		DC to 872MHz	20	25	—	dB	
		872 to 900MHz	15	18	—	dB	
		900 to 902MHz	13	15	—	dB	
		902 to 905MHz	8	13	—	dB	
		962 to 965MHz	10	15	—	dB	
		965 to 970MHz	15	18	—	dB	
		970 to 995MHz	20	25	—	dB	
		1005 to 1040MHz	30	33	—	dB	
		1040 to 3000MHz	15	20	—	dB	
In-band VSWR		917 to 950MHz	—	2.3	2.5		
Matching constants	C_1			6		pF	
	L_1			6		nH	
	C_2			7		pF	
	L_2			8		nH	

5. NMT type (Tx)

Part number: FAR-F5CB-902M50-G201

T_a=–30 to 70°C

Item	Symbol	Condition	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	890 to 915MHz	—	4.0	4.5	dB	
In-band ripple		890 to 915MHz	—	1.3	2.0	dB	
Stopband attenuation		DC to 850MHz	20	25	—	dB	
		850 to 870MHz	15	22	—	dB	
		935 to 960MHz	20	28	—	dB	
		1012 to 1058MHz	30	33	—	dB	
		1058 to 3000MHz	15	20	—	dB	
In-band VSWR		890 to 915MHz	—	1.5	2.0		
Matching constants	C_1			5		pF	
	L_1			6		nH	
	C_2			6		pF	
	L_2			9		nH	

6. NMT type (Rx)

Part number: FAR-F5CB-947M50-G201

T_a=–30 to 70°C

Item	Symbol	Condition	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	935 to 960MHz	—	4.0	4.5	dB	
In-band ripple		935 to 960MHz	—	1.3	2.0	dB	
Stopband attenuation		DC to 890MHz	20	25	—	dB	
		890 to 915MHz	18	22	—	dB	
		980 to 1005MHz	18	30	—	dB	
		1012 to 1058MHz	28	32	—	dB	
		1089 to 1115MHz	30	32	—	dB	
		1115 to 3000MHz	15	20	—	dB	
In-band VSWR		935 to 960MHz	—	1.5	2.0		
Matching constants	C_1			5		pF	
	L_1			6		nH	
	C_2			6		pF	
	L_2			9		nH	

7. NTACS type (Tx)

Part number: FAR-F5CB-911M50-G201

T_a=–30 to 70°C

Item	Symbol	Condition	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	898 to 925MHz	—	4.0	4.5	dB	
In-band ripple		898 to 925MHz	—	1.5	2.0	dB	
Stopband attenuation		DC to 815MHz	25	27	—	dB	
		815 to 870MHz	22	25	—	dB	
		1008 to 1100MHz	30	33	—	dB	
		1100 to 3000MHz	15	20	—	dB	
In-band VSWR		898 to 925MHz	—	1.8	2.0		
Matching constants	C_1			6		pF	
	L_1			7		nH	
	C_2			5		pF	
	L_2			10		nH	

8. NTACS type (Rx)

Part number: FAR-F5CB-856M50-G201

T_a=–30 to 70°C

Item	Symbol	Condition	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	843 to 870MHz	—	4.0	4.5	dB	
In-band ripple		843 to 870MHz	—	1.5	2.0	dB	
Stopband attenuation		DC to 814MHz	22	25	—	dB	
		898 to 935MHz	22	25	—	dB	
		935 to 1100MHz	30	33	—	dB	
		1100 to 3000MHz	15	20	—	dB	
In-band VSWR		843 to 870MHz	—	1.8	2.0		
Matching constants	C_1			7		pF	
	L_1			8		nH	
	C_2			7		pF	
	L_2			9		nH	

9. NTT type (Tx)

Part number: FAR-F5CB-933M50-G201

T_a=–30 to 70°C

Item	Symbol	Condition	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	925 to 942MHz	—	3.5	4.2	dB	
In-band ripple		925 to 942MHz	—	1.0	1.5	dB	
Stopband attenuation		DC to 780MHz	20	25	—	dB	
		780 to 797MHz	25	30	—	dB	
		797 to 870MHz	20	25	—	dB	
		870 to 887MHz	25	28	—	dB	
		970 to 1070MHz	20	30	—	dB	
		1070 to 1087MHz	25	30	—	dB	
		1087 to 3000MHz	15	20	—	dB	
In-band VSWR		925 to 942MHz	—	1.8	2.0		
Matching constants	C_1			5		pF	
	L_1			7		nH	
	C_2			—			
	L_2			—			

10. NTT type (Rx)

Part number: FAR-F5CB-878M50-G201

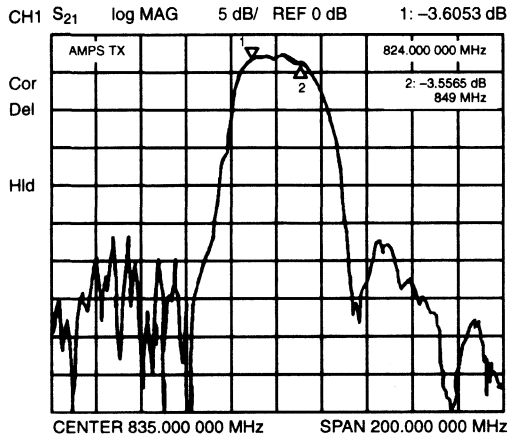
T_a=–30 to 70°C

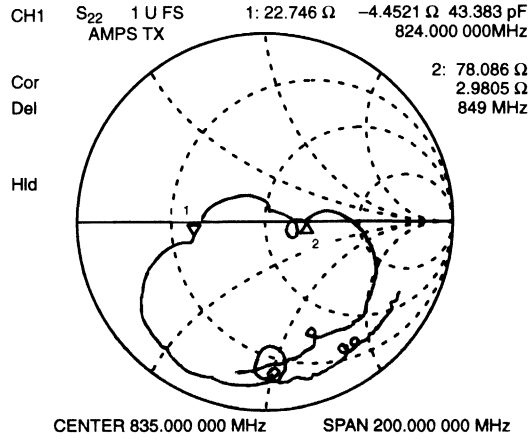
Item	Symbol	Condition	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	870 to 887MHz	—	3.5	4.2	dB	
In-band ripple		870 to 887MHz	—	1.0	1.5	dB	
Stopband attenuation		DC to 690MHz	20	25	—	dB	
		690 to 707MHz	30	33	—	dB	
		707 to 846MHz	20	25	—	dB	
		925 to 942MHz	25	28	—	dB	
		942 to 3000MHz	15	20	—	dB	
In-band VSWR		870 to 887MHz	—	1.8	2.0		
Matching constants	C_1			5		pF	
	L_1			8		nH	
	C_2			7		pF	
	L_2			10		nH	

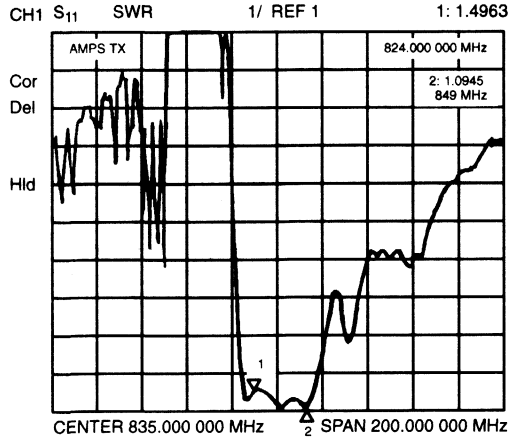
CHARACTERISTIC DATA EXAMPLE

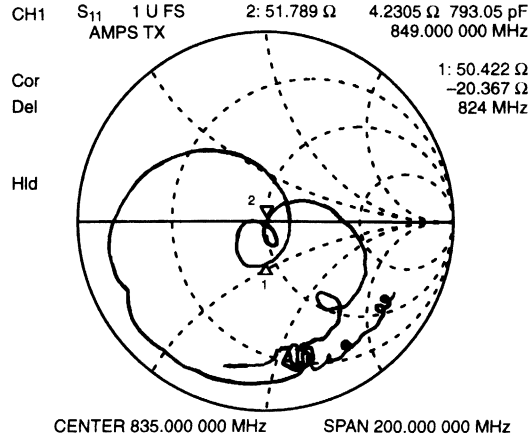
1. AMPS/ADC type (Tx)

Part number: FAR-F5CB-836M50-G201



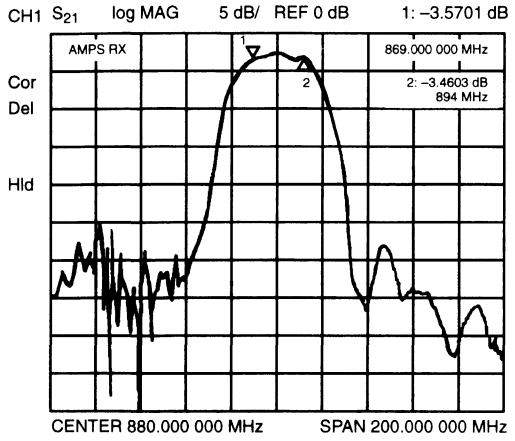


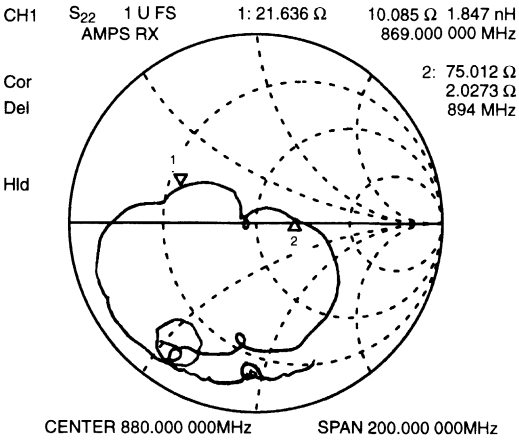


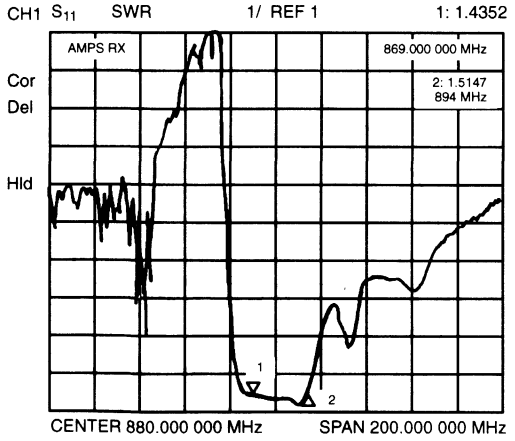


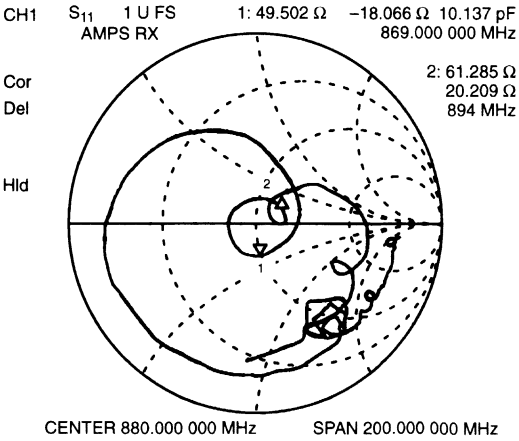
2. AMPS/ADC type (Rx)

Part number: FAR-F5CB-881M50-G201



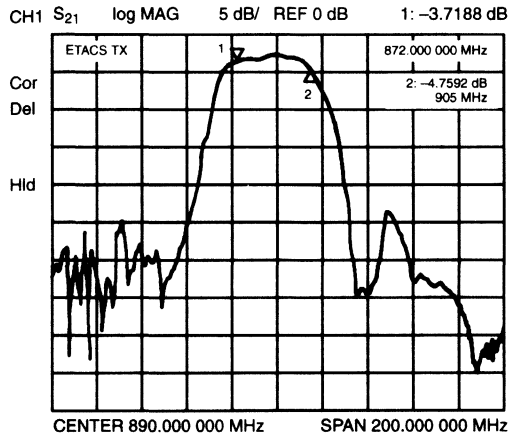


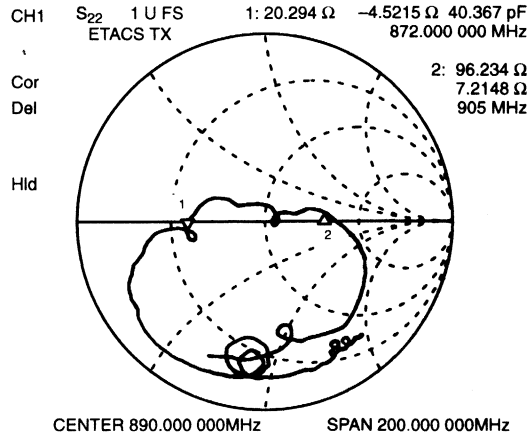


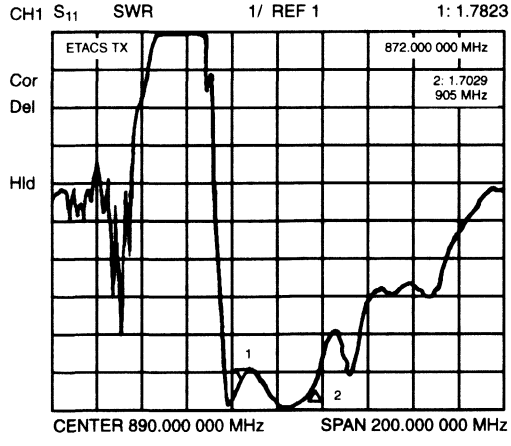


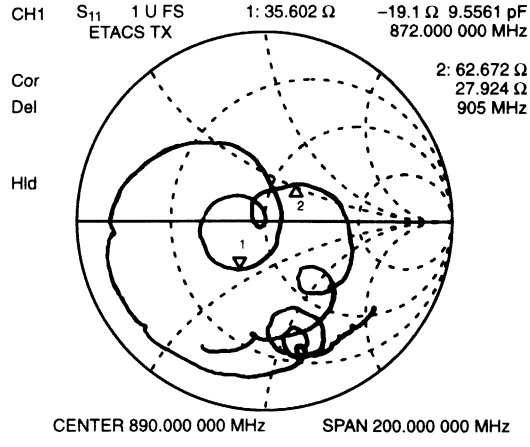
3. ETACS type (Tx)

Part number: FAR-F5CB-888M50-G201



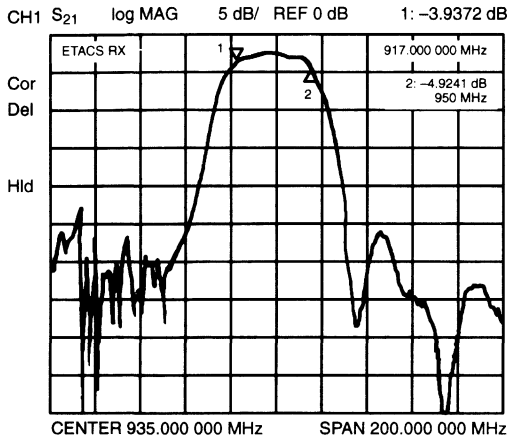


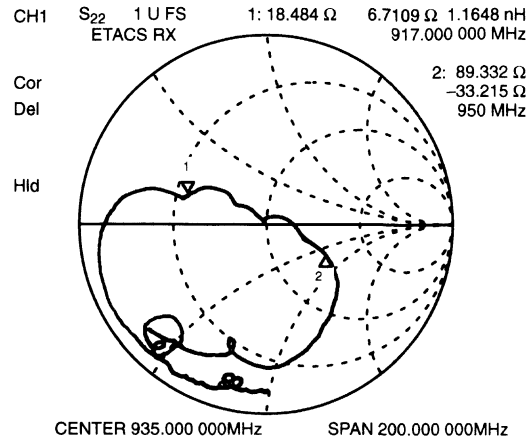


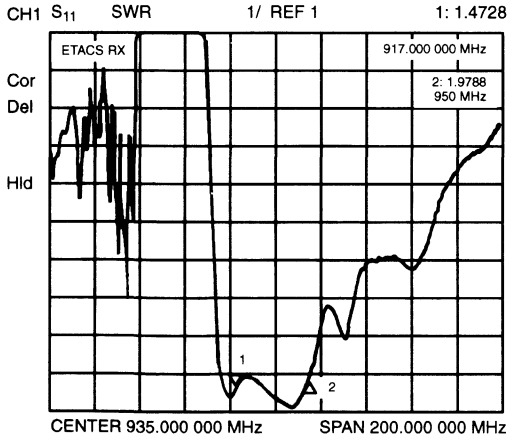


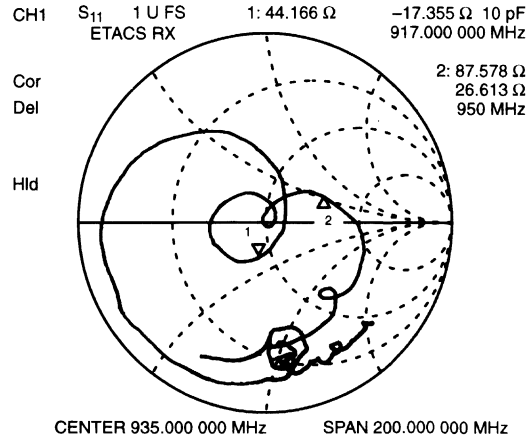
4. ETACS type (Rx)

Part number: FAR-F5CB-933M50-G202



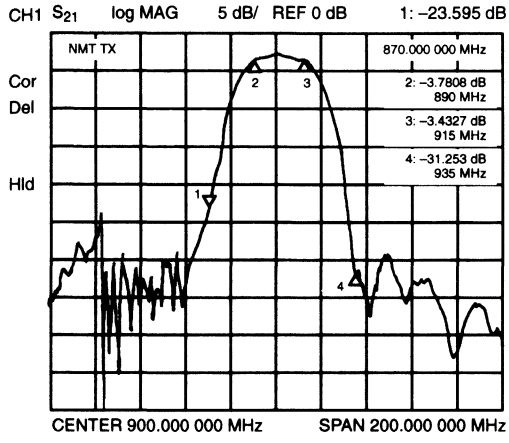


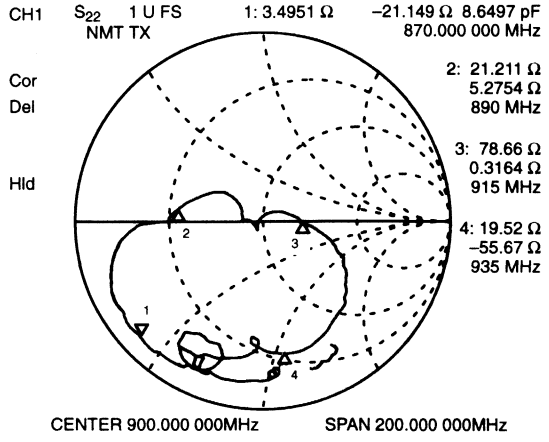


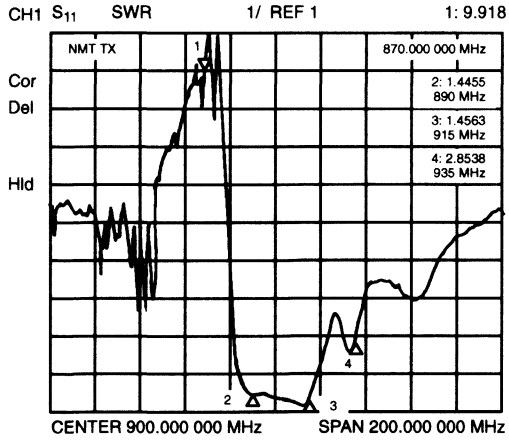


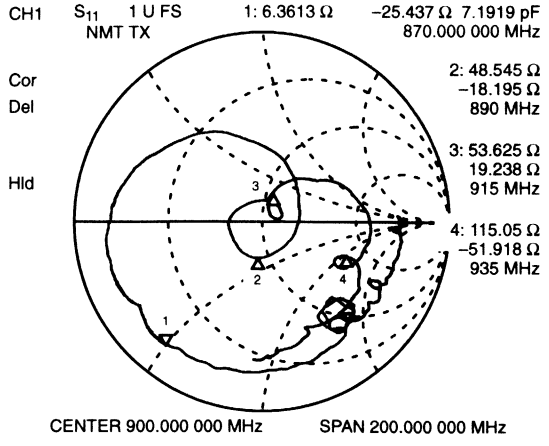
5. NMT/GSM type (Tx)

Part number: FAR-F5CB-902M50-G201



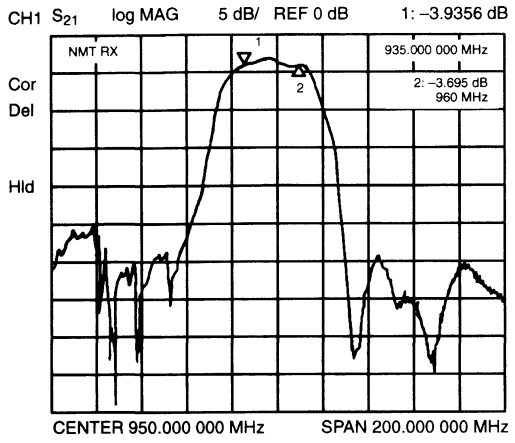


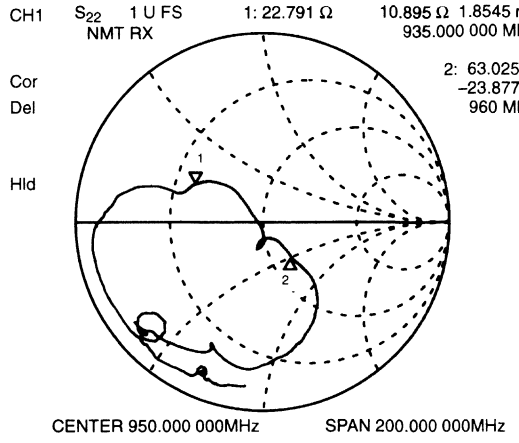


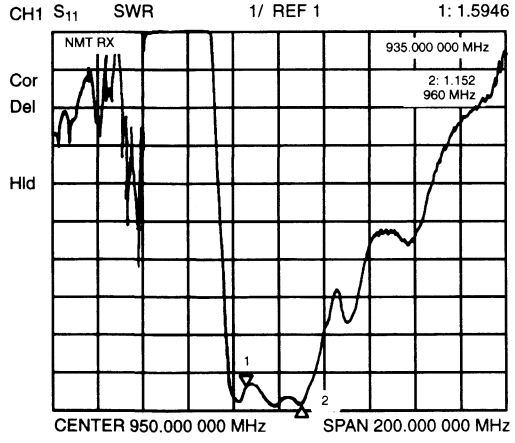


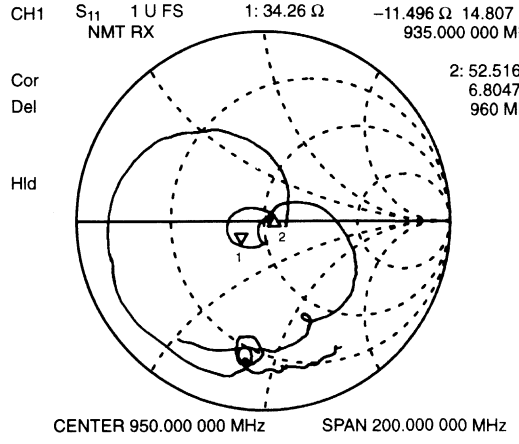
6. NMT/GSM type (Rx)

Part number: FAR-F5CB-947M50-G201

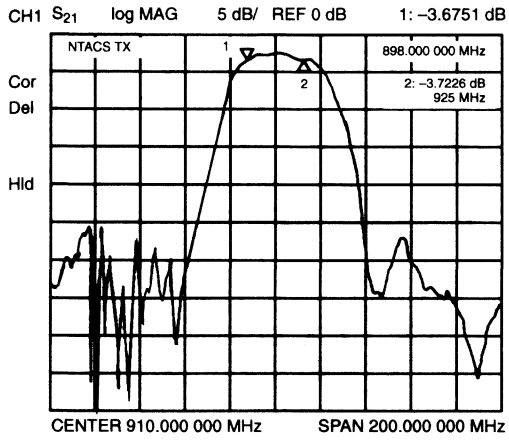


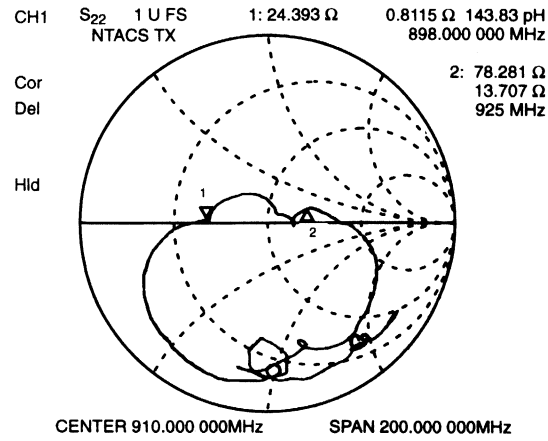


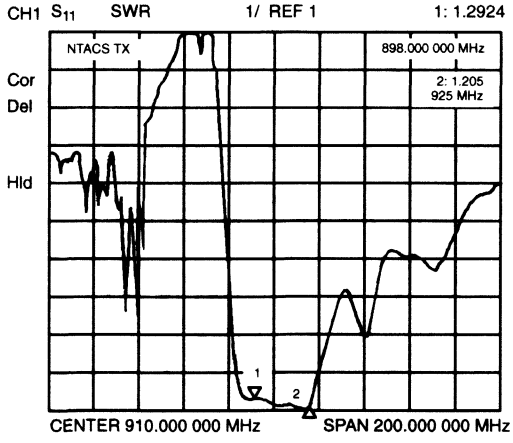


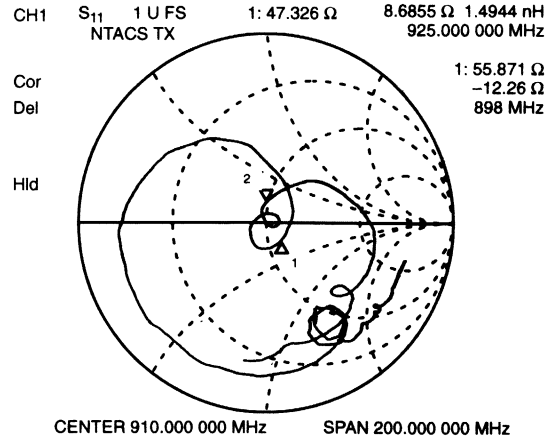


7. NTACS type (Tx)
Part number: FAR-F5CB-911M50-G201



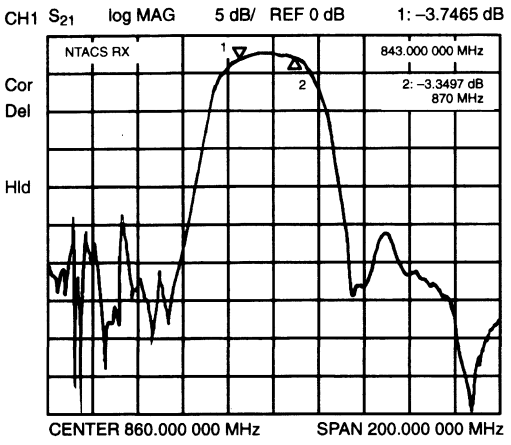


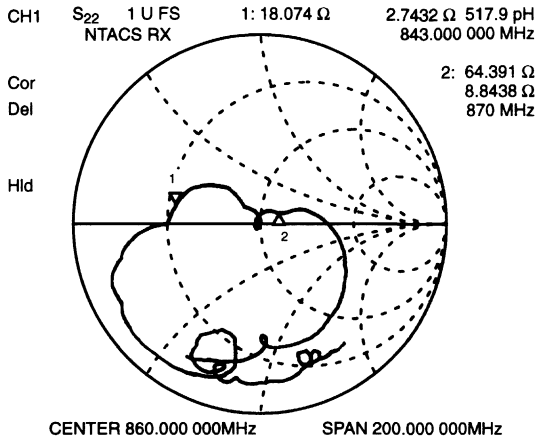


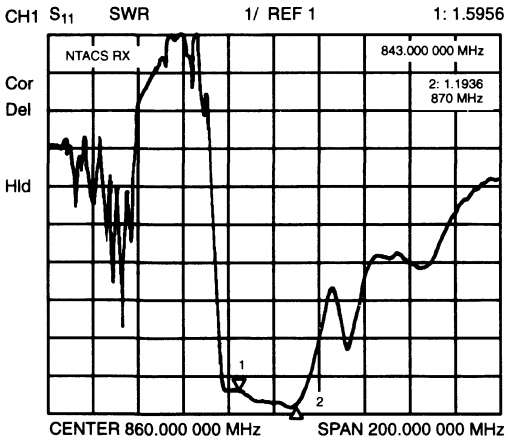


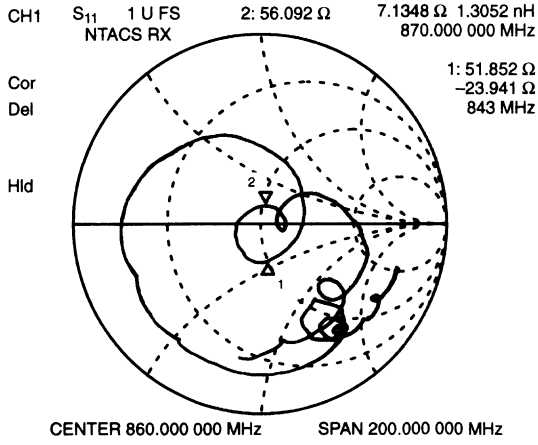
8. NTACS type (Rx)

Part number: FAR-F5CB-856M50-G201



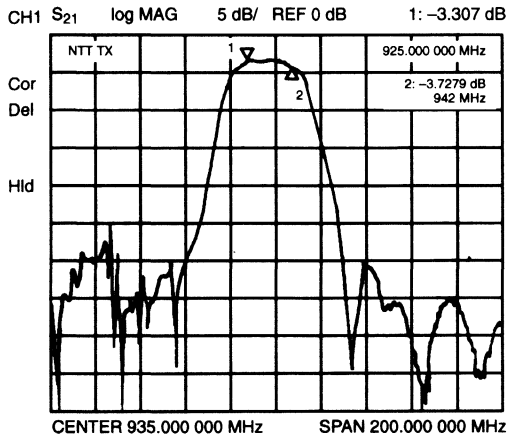


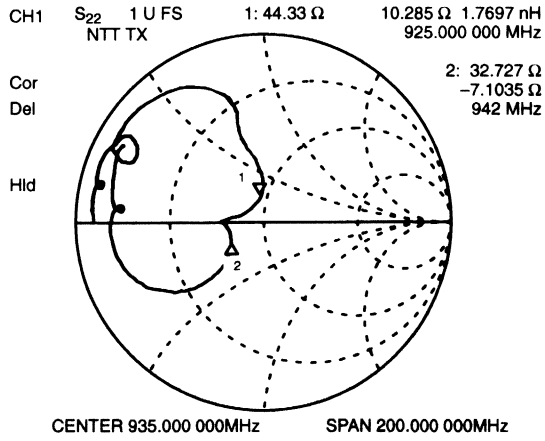


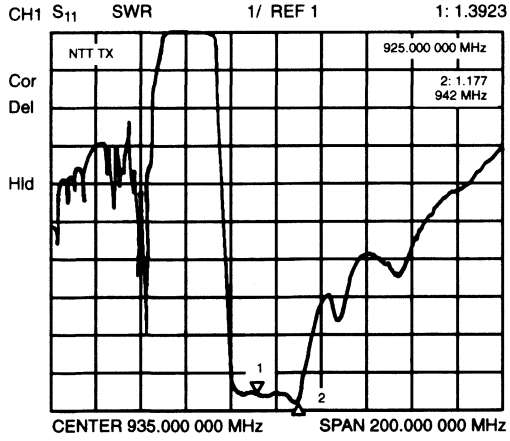


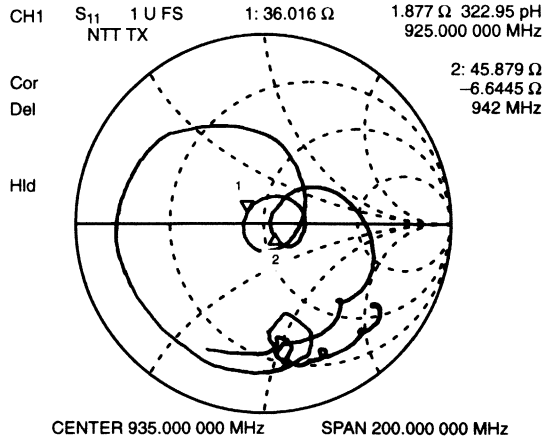
9. NTT type (Tx)

Part number: FAR-F5CB-933M50-G201



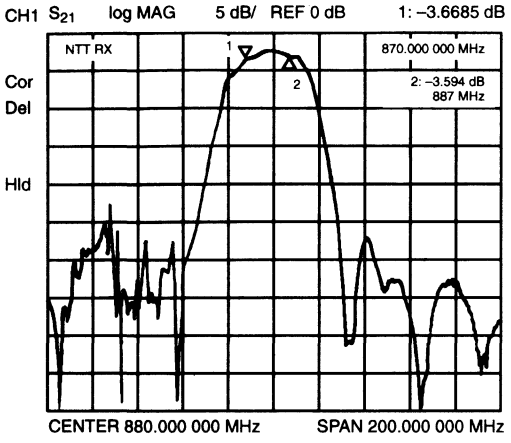


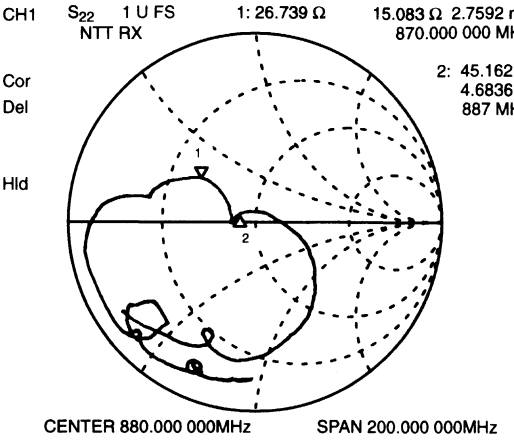


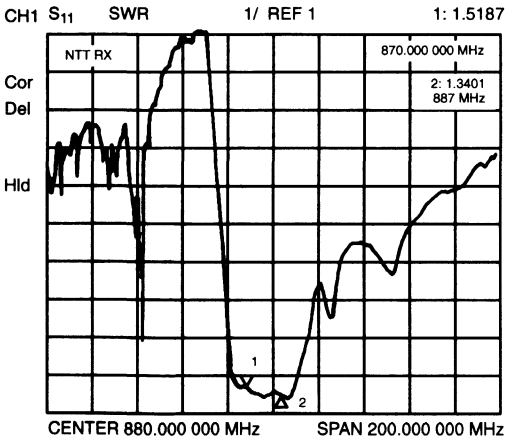


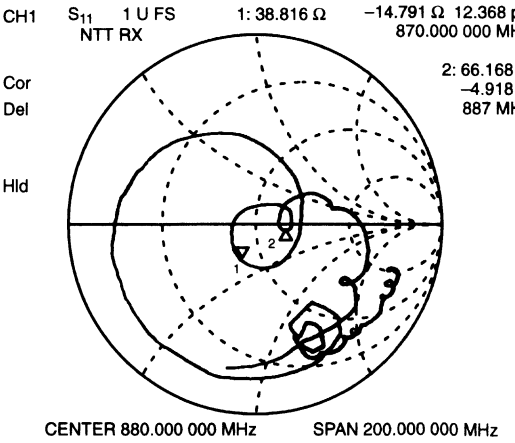
10. NTT type (Rx)

Part number: FAR-F5CB-878M50-G201

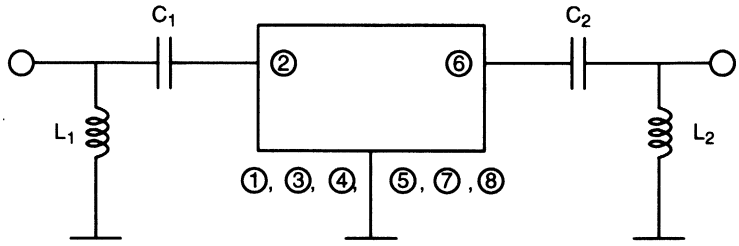








TEST CIRCUIT



* Each value is changed according to specification

PART NUMBER DESIGNATION

Designation example

FAR–F5CB– □□□□□□ –G□□□ – □
① ② ③

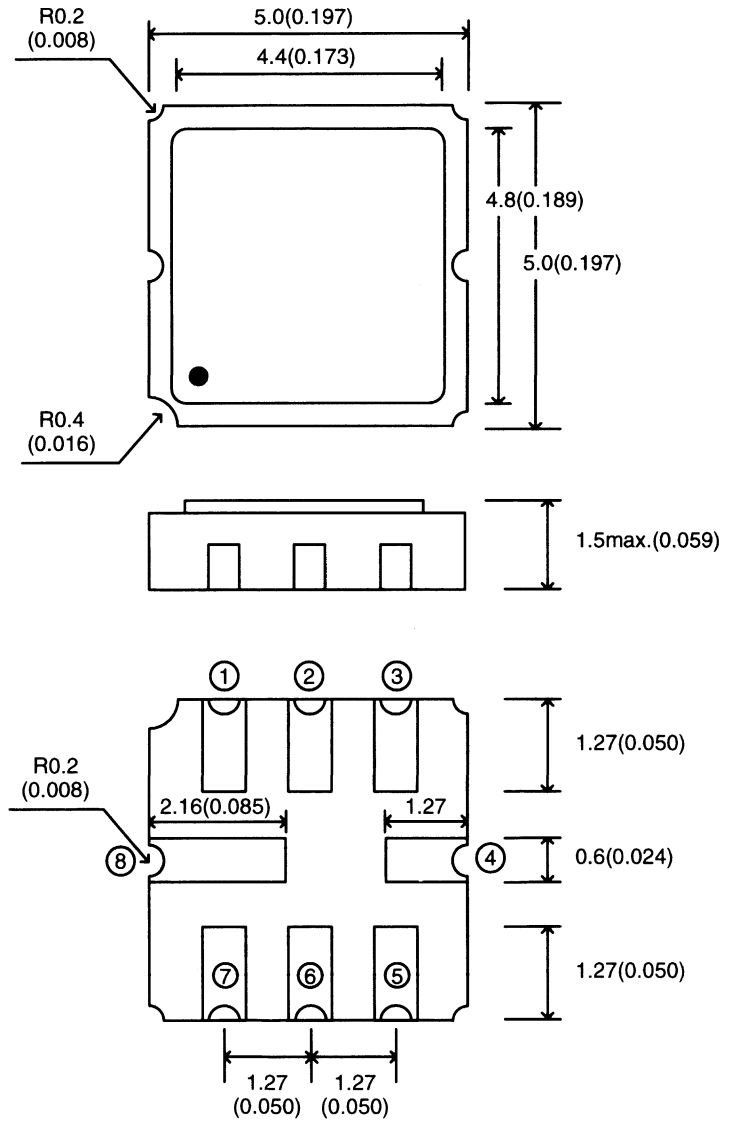
① Frequency designation : Specify the nominal frequency in six alphanumeric characters. Enter M (for MHz) at the decimal point. Refer to "PART NUMBERS".
Example: For an 836.5MHz device, designate as 836M50.

② Serial number : Specify a number from 201 to 299

③ Packaging (Reeled tape) :

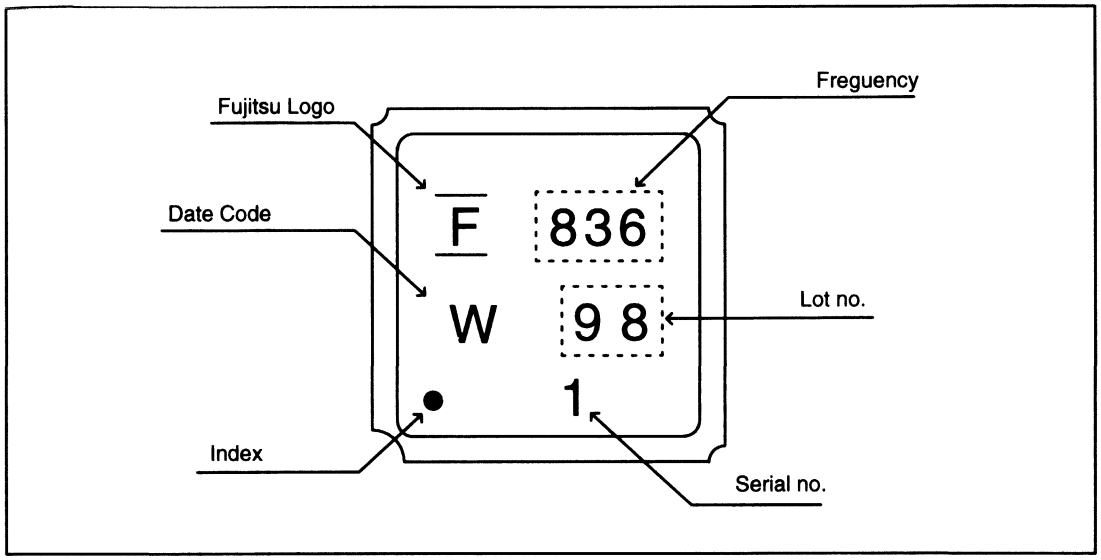
Designation	Contents
T	1Kpcs/reel
R	3Kpcs/reel

DIMENSIONS



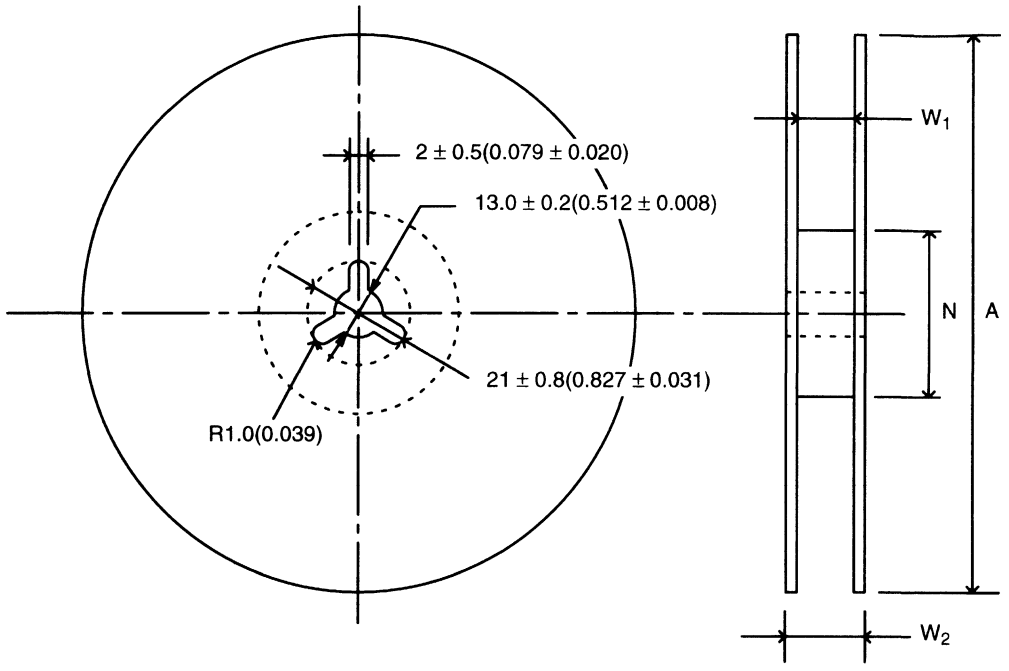
Unit: mm(in.)

MARKING


Fujitsu Logo
Freguency
Date Code
F
836
W
98
Lot no.
1
Index
Serial no.

PACKAGING: Reel type

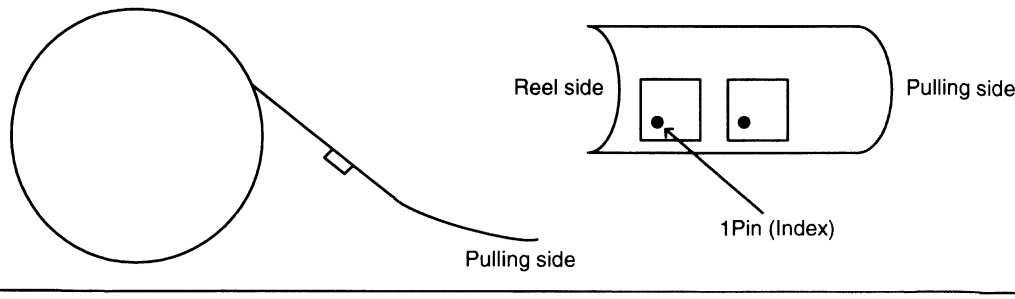
1. Reel dimension



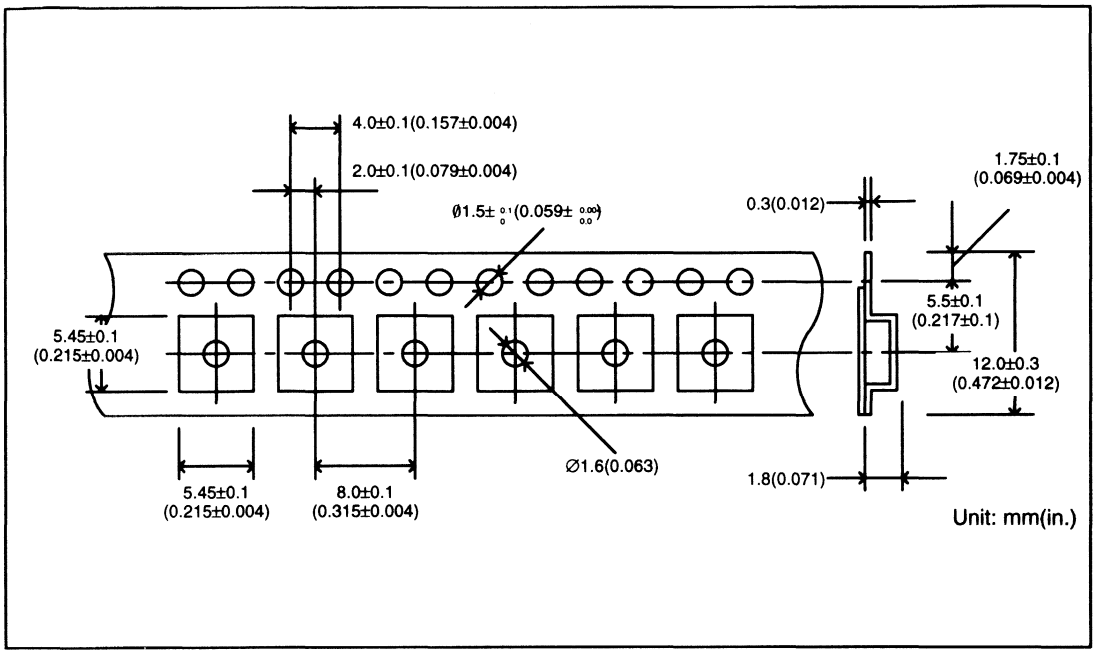
Designation	A	N	W_1	W_2
–T	250 (9.843)	80 (3.150)	$12.4^{+2.0}_{0.0}$ ($0.488^{+0.079}_{0.0}$)	18.4 or less(0.724)
–R	330 (12.972)	80 (3.150)	$12.4^{+2.0}_{0.0}$ ($0.488^{+0.079}_{0.0}$)	18.4 or less(0.724)

Unit: mm(in.)

2. Package style



3. Tape dimension



MEMO

FUJITSU SEMICONDUCTOR
DATA SHEET

DS04–23107–2E

ASSP

PIEZOELECTRIC SAW FILTERS

F5 SERIES(G210)

SAW-BPF, 700MHz to 1000MHz

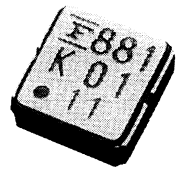
DESCRIPTION

The F5 series are wideband bandpass filters for use in the 700MHz to 1000MHz range. The F5 series uses a single lithium tantalate piezoelectric crystal ($LiTaO_3$) that has large electromechanical coupling coefficient. That prorides wide bandwidths and exceptional stability. Our exclusive mounting technique makes the F5 series very compact and surface mountable. The F5 series is most suitable for use in handheld phones.

FEATURES

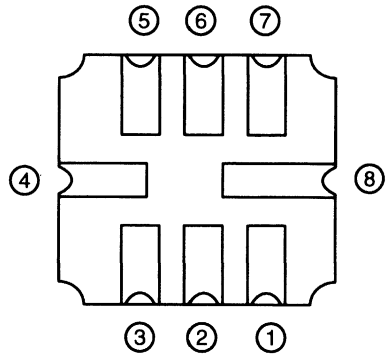
- Considerably smaller and lighter than the dielectric filter (Volume and weight are reduced by 1/30.)
- Surface mount package (SMT)
- Low insertion loss
- High power rating: 0.2 W guaranteed
- High stopband attenuation type available for AMPS/ADC, ETACS, NMT/GSM–Rx

PACKAGE



PIN ASSIGNMENT

(BOTTOM VIEW)



Pin no.	Pin name	Description
1	GND	Ground pin
2	IN	Input pin
3	GND	Ground pin
4	GND	Ground pin
5	GND	Ground pin
6	OUT	Output pin
7	GND	Ground pin
8	GND	Ground pin

MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Operating temperature	T_a	–30 to 70	°C
Storage temperature	T_{stg}	–40 to 100	°C
Maximum input level	P_{in}	200	mW
Frequency range		700 to 1000	MHz

RECOMMENDED OPERATING CONDITIONS

Item	Symbol	Rating	Unit
Operating temperature	T_a	–30 to 70	°C

PART NUMBERS

Rx : For Receiver

No.	Part Number	System	Use	Center Frequency (MHz)	Bandwidth (MHz)	Remarks
1	FAR–F5CB–881M50–G211	AMPS/ADC	Rx	881.5	25	High stopband attenuation
2	FAR–F5CB–933M50–G212	ETACS	Rx	933.5	33	High stopband attenuation
3	FAR–F5CB–947M50–G211	NMT/GSM	Rx	947.5	25	High stopband attenuation

ELECTRIC CHARACTERISTICS

1. AMPS/ADC type (Rx)

Part number: FAR-F5CB-881M50-G211

T_a=–30 to 70°C

Item	Symbol	Condition	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	869 to 894MHz	—	4.8	5.3	dB	
In-band ripple		869 to 894MHz	—	1.7	2.0	dB	
Stopband attenuation		DC to 824MHz	35	38	—	dB	
		824 to 849MHz	29	35	—	dB	
		914 to 939MHz	20	25	—	dB	
		947 to 1049MHz	40	45	—	dB	
		1049 to 3000MHz	15	—	—	dB	
In-band VSWR		869 to 894MHz	—	1.6	2.0		
Matching constants	C_1			6		pF	
	L_1			8		nH	
	C_2			6		pF	
	L_2			8		nH	

2. ETACS type (Rx)

Part number: FAR-F5CB-933M50-G212

T_a=–30 to 70°C

Item	Symbol	Condition	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	917 to 950MHz	—	5.5	6.0	dB	
In-band ripple		917 to 950MHz	—	2.0	2.5	dB	
Stopband attenuation		DC to 872MHz	35	40	—	dB	
		872 to 894MHz	35	38	—	dB	
		894 to 905MHz	15	20	—	dB	
		964 to 970MHz	15	20	—	dB	
		970 to 997MHz	20	25	—	dB	
		1005 to 1150MHz	40	45	—	dB	
		1150 to 3000MHz	15	—	—	dB	
In-band VSWR		917 to 950MHz	—	2.3	2.5		
Matching constants	C_1			6		pF	
	L_1			8		nH	
	C_2			6		pF	
	L_2			8		nH	

3. NMT type (Rx)

Part number: FAR-F5CB-947M50-G211

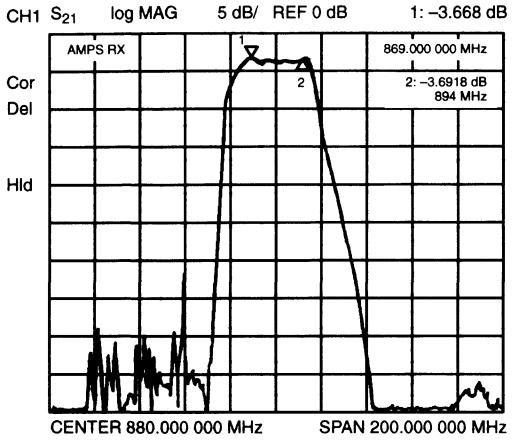
T_a=–30 to 70°C

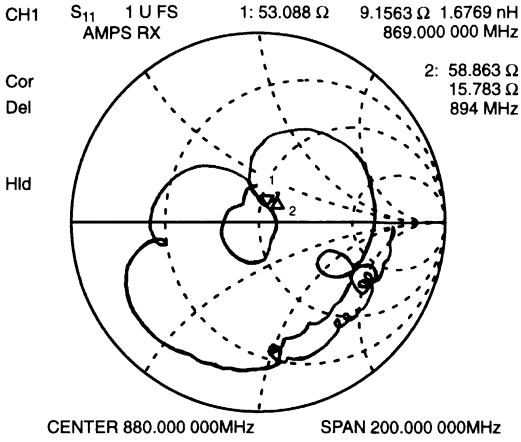
Item	Symbol	Condition	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	935 to 960MHz	—	4.7	5.0	dB	
In-band ripple		935 to 960MHz	—	1.5	2.0	dB	
Stopband attenuation		DC to 815MHz	40	45	—	dB	
		815 to 830MHz	35	37	—	dB	
		830 to 845MHz	40	45	—	dB	
		845 to 890MHz	30	35	—	dB	
		890 to 915MHz	30	33	—	dB	
		976 to 980MHz	15	20	—	dB	
		980 to 1005MHz	20	23	—	dB	
		1012 to 1058MHz	40	45	—	dB	
		1089 to 1140MHz	40	45	—	dB	
		1140 to 3000MHz	15	—	—	dB	
In-band VSWR		935 to 960MHz	—	2.0	2.5		
Matching constants	C_1			6		pF	
	L_1			8		nH	
	C_2			6		pF	
	L_2			8		nH	

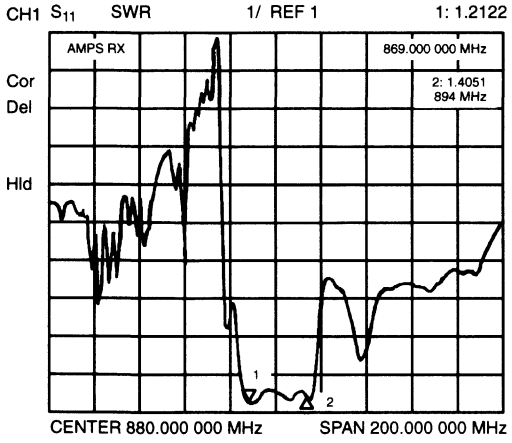
CHARACTERISTIC DATA EXAMPLE

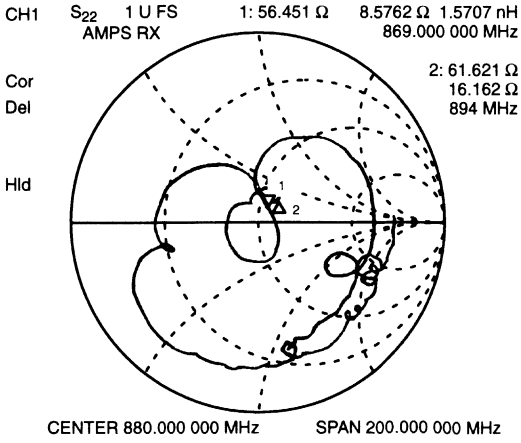
1. AMPS/ADC type (Rx)

Part number: FAR-F5CB-881M50-G211



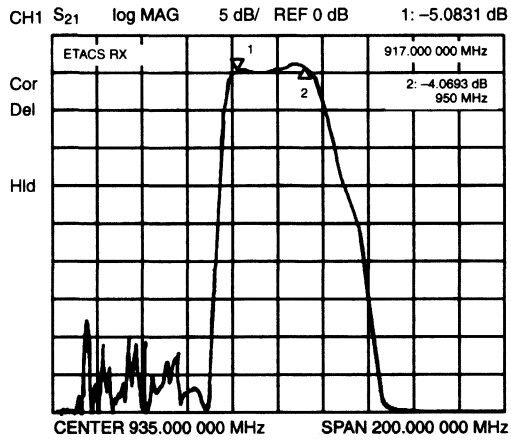


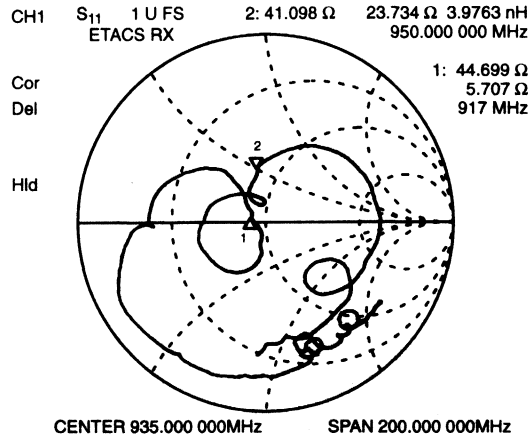


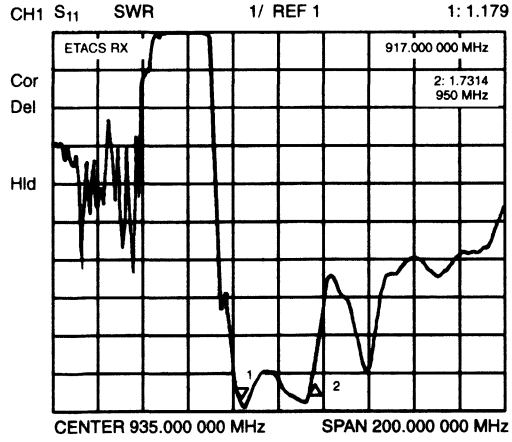


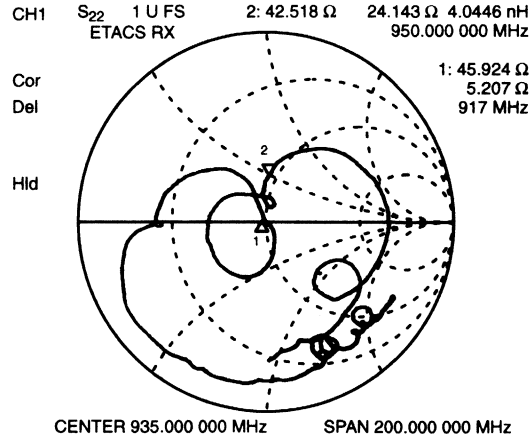
2. ETACS type (Rx)

Part number: FAR-F5CB-933M50-G212



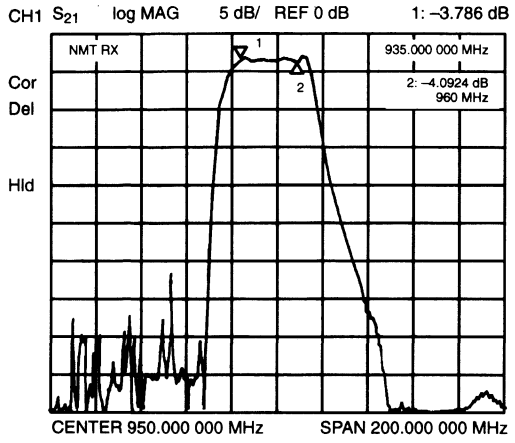


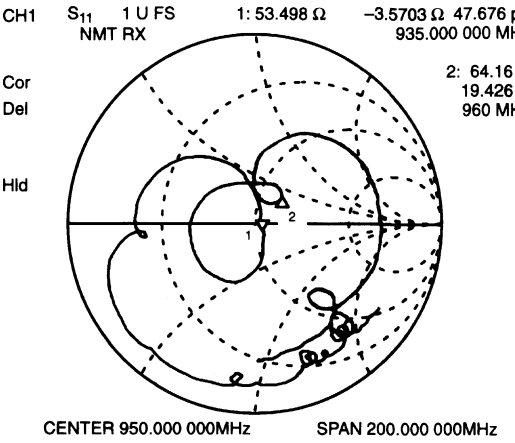


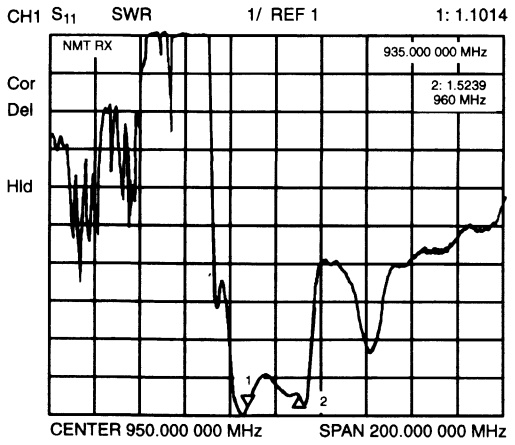


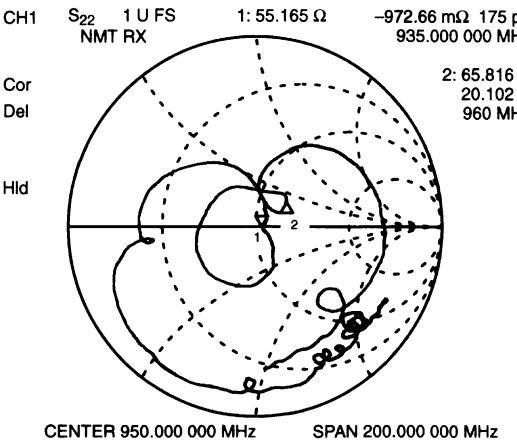
3. NMT/GSM type (Rx)

Part number: FAR-F5CB-947M50-G211

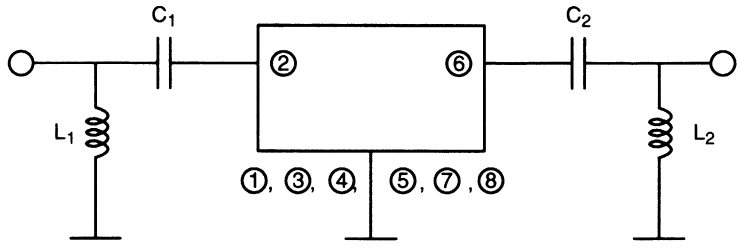








TEST CIRCUIT



* Each value is changed according to specification

PART NUMBER DESIGNATION

Designation example

FAR-F5CB-□□□□□□-G□□□-□
① ② ③

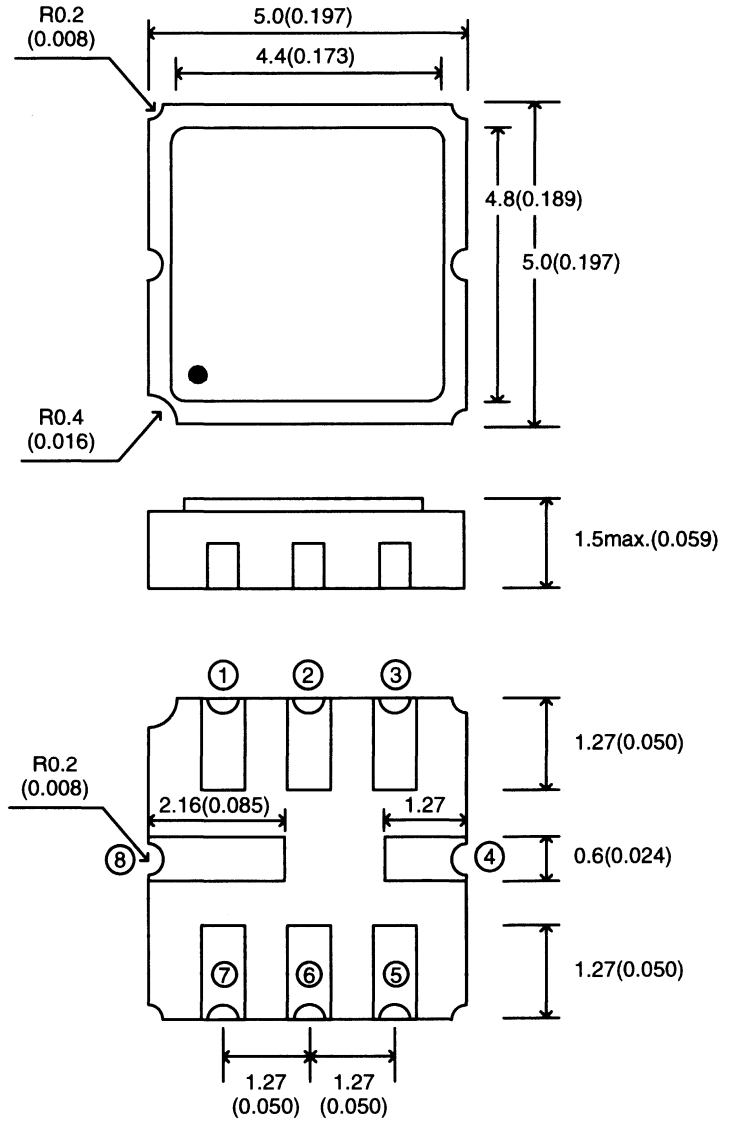
① Frequency designation : Specify the nominal frequency in six alphanumeric characters. Enter M (for MHz) at the decimal point. Refer to "PART NUMBERS".
Example: For an 836.5MHz device, designate as 836M50.

② Serial number : Specify a number from 201 to 299

③ Packaging (Reeled tape) :

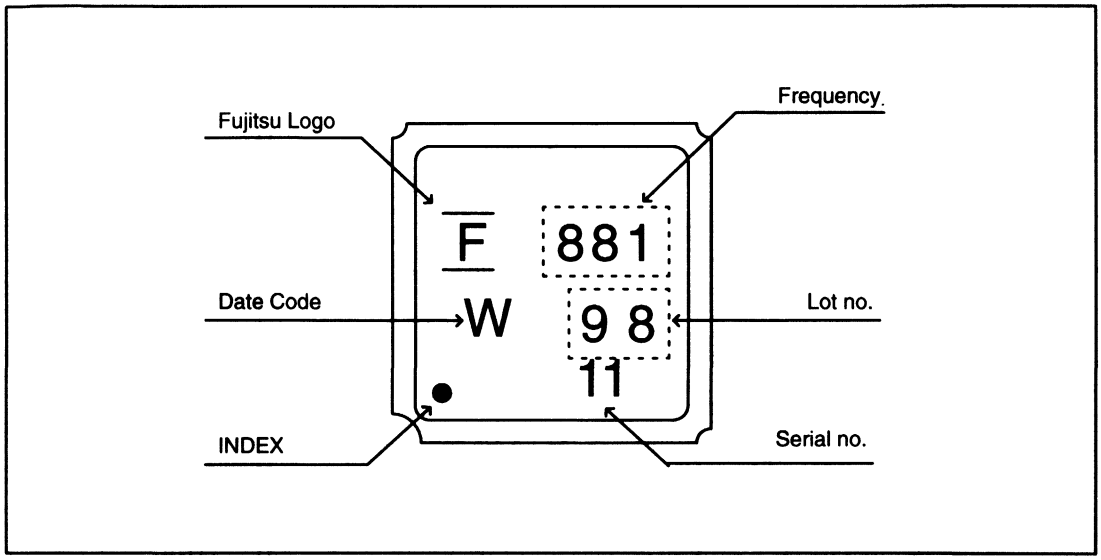
Designation	Contents
T	1Kpcs/reel
R	3Kpcs/reel

DIMENSIONS



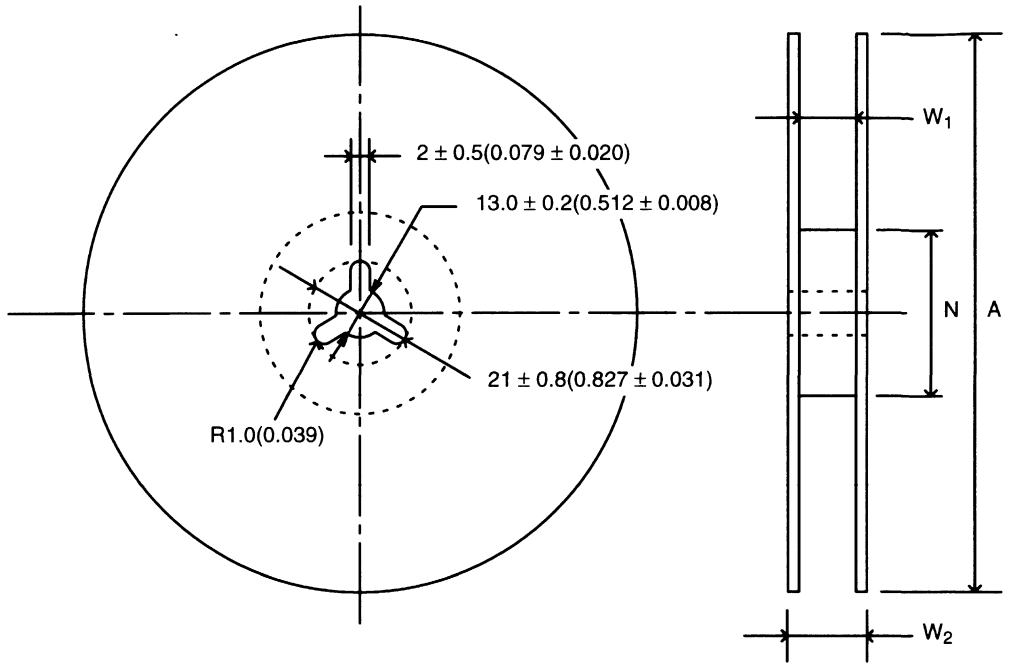
Unit: mm(in.)

MARKING


Fujitsu Logo
Frequency
F
881
Date Code
W
9 8
Lot no.
11
INDEX
Serial no.

PACKAGING: Reel type

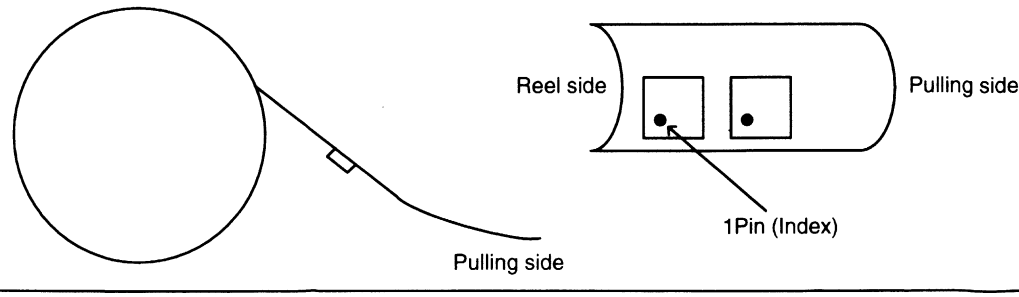
1. Reel dimension



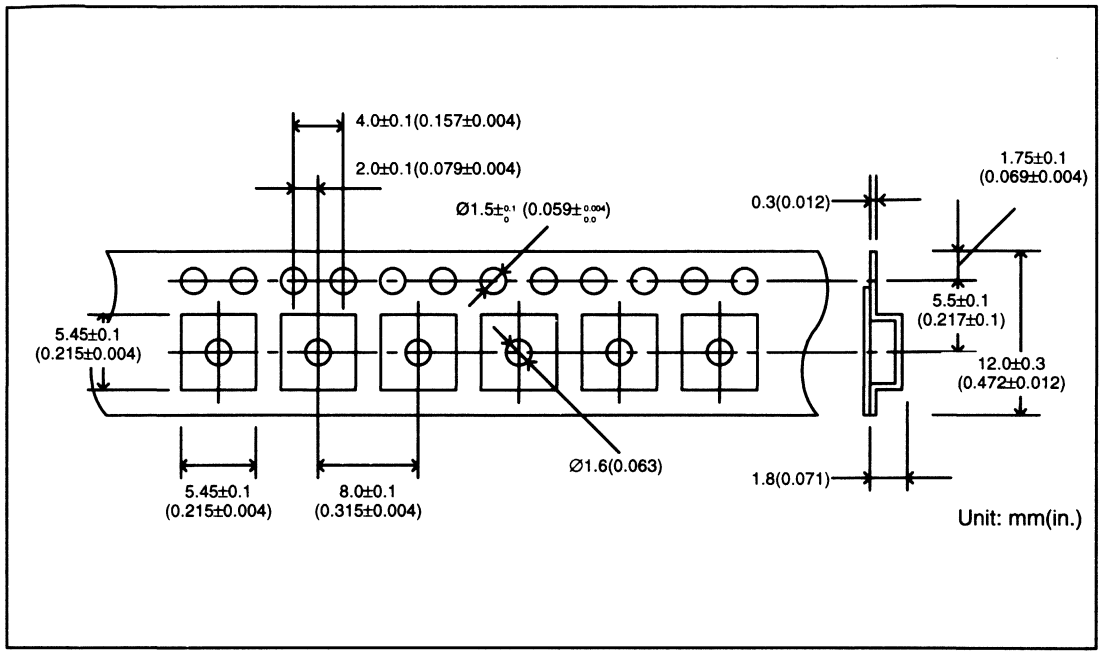
Designation	A	N	W_1	W_2
–T	250 (9.843)	80 (3.150)	$12.4^{+2.0}_{0.0}$ ($0.488^{+0.079}_{0.0}$)	18.4 or less(0.724)
–R	330 (12.972)	80 (3.150)	$12.4^{+2.0}_{0.0}$ ($0.488^{+0.079}_{0.0}$)	18.4 or less(0.724)

Unit: mm(in.)

2. Package style



3. Tape dimension



MEMO

FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-23108-3E

ASSP

PIEZOELECTRIC SAW BPF

F5 SERIES(L2 Type)

SAW BANDPASS FILTER (700 to 1000 MHz)

DESCRIPTION

F5 series are wideband bandpass filters for use in the 700MHz to 1000MHz of frequency range.

F5 series uses a single lithium tantalate piezoelectric crystal ($LiTaO_3$) that has large electromechanical coupling coefficient. This provides wide bandwidths and exceptional stability.

Our exclusive mounting technology makes F5 series very compact and surface mountable.

Standard L2 type is much lower Insertion Loss and High attenuation L2 type is much higher stopband attenuation than other filters. Further more, Impedance is realized at 50 Ω in passband.

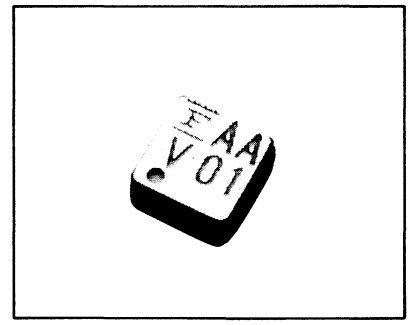
L2 type can be handled without outside matching circuit.

The F5 series is most suitable for use in handheld phones of both analog and digital systems.

FEATURES

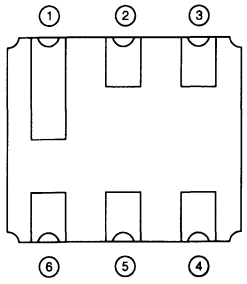
- Ultra compact and light (0.02 cc, 0.1 g)
- Outside matching circuit is unnecessary.
- Surface mount package (SMT)
- Wide variety of bandwidths for worldwide system (AMPS, ADC, ETACS, NMT, GSM, NTT, NTACS, PDC)
- Low insertion loss
- High power rating : 0.2 W garanteed

PACKAGE



PIN ASSIGNMENT

(Bottom view)



Pin No.	Pin name	Description
1	GND	Ground Pin
2	IN	Input Pin
3	GND	Ground Pin
4	GND	Ground Pin
5	OUT	Output Pin
6	GND	Ground Pin

MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Operating temperature	Ta	–30 to +70 *1	°C
Storage temperature	Tstg	–40 to +100	
Maximum input level	Pin	+200	mW
Frequency range	–	+700 to +1000	MHz

*1 This is also the Recommended Operating Conditions.

STANDARD FREQUENCIES

STANDARD VERSION

Center frequency (MHz)	Bandwidths (MHz)	System	Part Symbol	Part number
836.5	25	AMPS/ADC (Tx)	A A	FAR-F5CC-836M50-L2AA
881.5	25	AMPS/ADC (Rx)	A B	FAR-F5CC-881M50-L2AB
933.5	17	NTT (Tx)	B A	FAR-F5CC-933M50-L2BA
878.5	17	NTT (Rx)	B B	FAR-F5CC-878M50-L2BB
888.5	33	ETACS (Tx)	C A	FAR-F5CC-888M50-L2CA
933.5	33	ETACS (Rx)	C B	FAR-F5CC-933M50-L2CB
911.5	27	NTACS (Tx)	D A	FAR-F5CC-911M50-L2DA
856.5	27	NTACS (Rx)	D B	FAR-F5CC-856M50-L2DB
902.5	25	NMT/GSM (Tx)	E A	FAR-F5CC-902M50-L2EA
947.5	25	NMT/GSM (Rx)	E B	FAR-F5CC-947M50-L2EB
950.0	20	PDC (Tx)	F A	FAR-F5CC-950M00-L2FA
820.0	20	PDC (Rx)	F B	FAR-F5CC-820M00-L2FB

HIGH ATTENUATION VERSION

Center frequency (MHz)	Bandwidths (MHz)	System	Part Symbol	Part number
836.5	25	AMPS/ADC (Tx)	A Z	FAR-F5CC-836M50-L2AZ
881.5	25	AMPS/ADC (Rx)	A Y	FAR-F5CC-881M50-L2AY
902.5	25	NMT/GSM (Tx)	E Z	FAR-F5CC-902M50-L2EZ
947.5	25	NMT/GSM (Rx)	E Y	FAR-F5CC-947M50-L2EY

ELECTRICAL CHARACTERISTICS (STANDARD VERSION)

1. AMPS / ADC system (Tx) Part number : FAR-F5CC-836M50-L2AA

(Ta = –30 to 70°C)

Item	Symbol	Conditions	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	824 to 849 MHz	–	2.0	3.5	dB	
In-band ripple	–	824 to 849 MHz	–	0.6	2.0	dB	
Absolute stopband attenuation	–	–	–	–	–	dB	
	–	869 to 894 MHz	20	27	–	dB	
	–	–	–	–	–	dB	
In-band VSWR	–	824 to 849 MHz	–	1.8	2.0	–	

2. AMPS / ADC system (Rx) Part number : FAR-F5CC-881M50-L2AB

(Ta = –30 to 70°C)

Item	Symbol	Conditions	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	869 to 894 MHz	–	2.5	3.5	dB	
In-band ripple	–	869 to 894 MHz	–	0.6	2.0	dB	
Absolute stopband attenuation	–	DC to 824 MHz	20	23	–	dB	
	–	824 to 849 MHz	20	28	–	dB	
	–	914 to 939 MHz	20	27	–	dB	
	–	939 to 1049 MHz	25	28	–	dB	
	–	1049 to 2000 MHz	20	21	–	dB	
In-band VSWR	–	869 to 894 MHz	–	1.8	2.0	–	

ELECTRICAL CHARACTERISTICS (STANDARD VERSION)

3. ETACS system (Tx)

Part number : FAR–F5CC–888M50–L2CA

(Ta = –30 to 70°C)

Item	Symbol	Conditions	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	872 to 905 MHz	–	3.0	5.0	dB	
In–band ripple	–	872 to 905 MHz	–	1.5	–	dB	
Absolute stopband attenuation	–	–	–	–	–	dB	
	–	917 to 950 MHz	10	15	–	dB	
	–	–	–	–	–	dB	
In–band VSWR	–	872 to 905 MHz	–	2.1	2.5	–	

4. ETACS system (Rx)

Part number : FAR–F5CC–933M50–L2CB

(Ta = –30 to 70°C)

Item	Symbol	Conditions	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	917 to 950 MHz	–	3.5	5.5	dB	
In–band ripple	–	917 to 950 MHz	–	2.0	–	dB	
Absolute stopband attenuation	–	DC to 872 MHz	20	32	–	dB	
	–	872 to 900 MHz	25	32	–	dB	
	–	900 to 905 MHz	10	15	–	dB	
	–	1007 to 1040 MHz	30	38	–	dB	
	–	1040 to 2000 MHz	20	26	–	dB	
In–band VSWR	–	917 to 950 MHz	–	2.0	2.5	–	

ELECTRICAL CHARACTERISTICS (STANDARD VERSION)

5. NTACS system (Tx) Part number : FAR-F5CC-911M50-L2DA

(Ta = –30 to 70°C)

Item	Symbol	Conditions	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	898 to 925 MHz	–	2.5	3.5	dB	
In-band ripple	–	898 to 925 MHz	–	0.6	2.0	dB	
Absolute stopband attenuation	–	–	–	–	–	–	
	–	843 to 870 MHz	25	29	–	dB	
	–	–	–	–	–	–	
In-band VSWR	–	898 to 925 MHz	–	1.8	2.0	–	

6. NTACS system (Rx) Part number : FAR-F5CC-856M50-L2DB

(Ta = –30 to 70°C)

Item	Symbol	Conditions	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	843 to 870 MHz	–	2.5	3.5	dB	
In-band ripple	–	843 to 870 MHz	–	0.6	2.0	dB	
Absolute stopband attenuation	–	DC to 733 MHz	23	25	–	dB	
	–	733 to 760 MHz	35	40	–	dB	
	–	760 to 815 MHz	25	29	–	dB	
	–	898 to 953 MHz	25	35	–	dB	
	–	953 to 980 MHz	35	40	–	dB	
	–	980 to 1100 MHz	25	30	–	dB	
	–	1100 to 2000 MHz	20	21	–	dB	
In-band VSWR	–	843 to 870 MHz	–	1.9	2.5	–	

ELECTRICAL CHARACTERISTICS (STANDARD VERSION)

7. NMT / GSM system (Tx) Part number : FAR-F5CC-902M50-L2EA

(Ta = –30 to 70°C)

Item	Symbol	Conditions	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	890 to 915 MHz	–	2.0	3.5	dB	
In-band ripple	–	890 to 915 MHz	–	0.6	2.0	dB	
Absolute stopband attenuation	–	–	–	–	–	dB	
	–	835 to 960 MHz	20	27	–	dB	
	–	–	–	–	–	dB	
In-band VSWR	–	890 to 915 MHz	–	1.8	2.0	–	

8. NMT / GSM system (Rx) Part number : FAR-F5CC-947M50-L2EB

(Ta = –30 to 70°C)

Item	Symbol	Conditions	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	935 to 960 MHz	–	2.5	3.5	dB	
In-band ripple	–	935 to 960 MHz	–	0.6	2.0	dB	
Absolute stopband attenuation	–	DC to 800 MHz	20	25	–	dB	
	–	890 to 915 MHz	20	28	–	dB	
	–	980 to 1025 MHz	15	28	–	dB	
	–	1025 to 1070 MHz	35	40	–	dB	
	–	1070 to 1105 MHz	30	35	–	dB	
	–	1105 to 1600 MHz	20	25	–	dB	
	–	1600 to 2000 MHz	15	20	–	dB	
In-band VSWR	–	935 to 960 MHz	–	1.9	2.5	–	

ELECTRICAL CHARACTERISTICS (STANDARD VERSION)

9. PDC system (Tx) Part number : FAR–F5CC–950M00–L2FA

(Ta = –30 to 70°C)

Item	Symbol	Conditions	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	940 to 960 MHz	–	2.0	3.0	dB	
In–band ripple	–	940 to 960 MHz	–	0.6	1.5	dB	
Absolute stopband attenuation	–	–	–	–	–	dB	
	–	810 to 830 MHz	20	25	–	dB	
	–	–	–	–	–	dB	
In–band VSWR	–	940 to 960 MHz	–	1.8	2.0	–	

10. PDC system (Rx) Part number : FAR–F5CC–820M00–L2FB

(Ta = –30 to 70°C)

Item	Symbol	Conditions	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	810 to 830 MHz	–	3.0	4.0	dB	
In–band ripple	–	810 to 830 MHz	–	0.5	1.5	dB	
Absolute stopband attenuation	–	DC to 740 MHz	20	25	–	dB	
	–	940 to 960 MHz	25	28	–	dB	
	–	1040 to 1060 MHz	25	30	–	dB	
	–	1060 to 2000 MHz	20	26	–	dB	
In–band VSWR	–	810 to 830 MHz	–	1.8	2.0	–	

ELECTRICAL CHARACTERISTICS (HIGH ATTENUATION VERSION)

11. AMPS / ADC system (Tx) Part number : FAR–F5CC–836M50–L2AZ

(Ta = –30 to 70°C)

Item	Symbol	Conditions	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	824 to 849 MHz	–	3.0	4.0	dB	
In–band ripple	–	824 to 849 MHz	–	1.0	2.0	dB	
Absolute stopband attenuation	–	D.C. to 800MHz	25	28	–	dB	
	–	869 to 894 MHz	30	40	–	dB	
	–	894 to 1049 MHz	30	35	–	dB	
	–	1049 to 2000 MHz	20	26	–	dB	
In–band VSWR	–	824 to 849 MHz	–	2.0	2.5	–	

12. AMPS / ADC system (Rx) Part number : FAR–F5CC–881M50–L2AY

(Ta = –30 to 70°C)

Item	Symbol	Conditions	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	869 to 894 MHz	–	2.8	4.0	dB	
In–band ripple	–	869 to 894 MHz	–	1.0	2.0	dB	
Absolute stopband attenuation	–	DC to 779 MHz	25	31	–	dB	
	–	779 to 804 MHz	35	40	–	dB	
	–	804 to 824 MHz	25	31	–	dB	
	–	824 to 849 MHz	20	31	–	dB	
	–	914 to 939 MHz	20	30	–	dB	
	–	939 to 1049 MHz	35	40	–	dB	
	–	1049 to 2000 MHz	20	26	–	dB	
In–band VSWR	–	869 to 894 MHz	–	2.0	2.5	–	

ELECTRICAL CHARACTERISTICS (HIGH ATTENUATION VERSION)

13. NMT / GSM system (Tx) Part number : FAR-F5CC-902M50-L2EZ

(Ta = -30 to 70°C)

Item	Symbol	Conditions	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	890 to 915 MHz	–	3.2	4.0	dB	
In-band ripple	–	890 to 915 MHz	–	1.0	2.0	dB	
Absolute stopband attenuation	–	D.C. to 845MHz	32	36	–	dB	
	–	845 to 870 MHz	20	33	–	dB	
	–	935 to 980 MHz	20	40	–	dB	
	–	980 to 1200 MHz	30	32	–	–	
	–	1200 to 2000 MHz	15	25	–	–	
In-band VSWR	–	890 to 915 MHz	–	2.1	2.5	–	

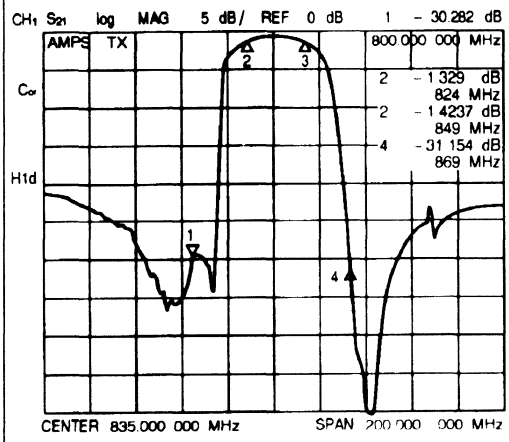
14. NMT / GSM system (Rx) Part number : FAR-F5CC-947M50-L2EY

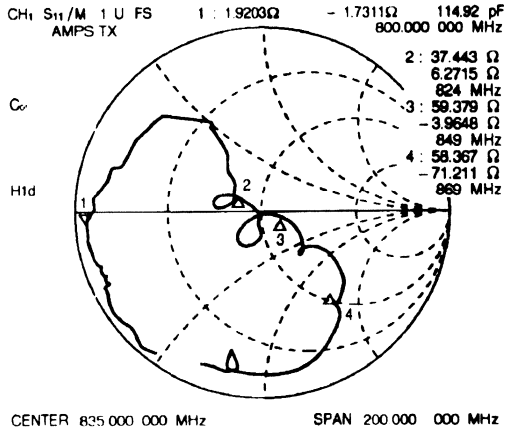
(Ta = -30 to 70°C)

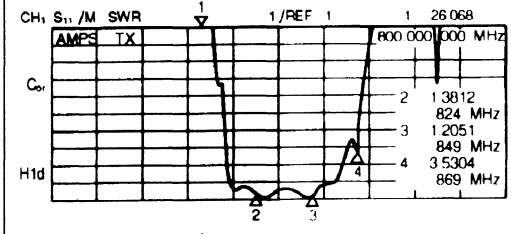
Item	Symbol	Conditions	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	935 to 960 MHz	–	3.2	4.0	dB	
In-band ripple	–	935 to 960 MHz	–	1.0	2.0	dB	
Absolute stopband attenuation	–	DC to 870 MHz	32	35	–	dB	
	–	890 to 915 MHz	20	30	–	dB	
	–	980 to 1025 MHz	15	40	–	dB	
	–	1025 to 1070 MHz	35	38	–	dB	
	–	1070 to 1105 MHz	30	35	–	dB	
	–	1105 to 2000 MHz	20	25	–	dB	
In-band VSWR	–	935 to 960 MHz	–	2.1	2.5	–	

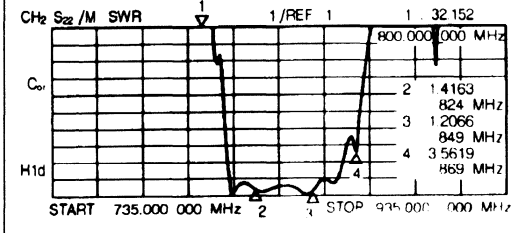
CHARACTERISTIC DATA EXAMPLES (STANDARD VERSION)

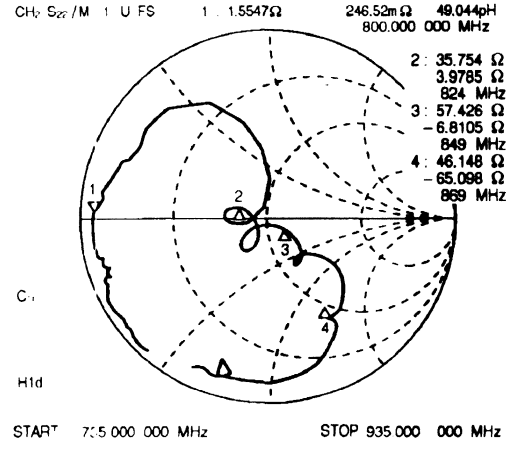
1. AMPS / ADC system (Tx) Part number : FAR-F5CC-836M50-L2AA





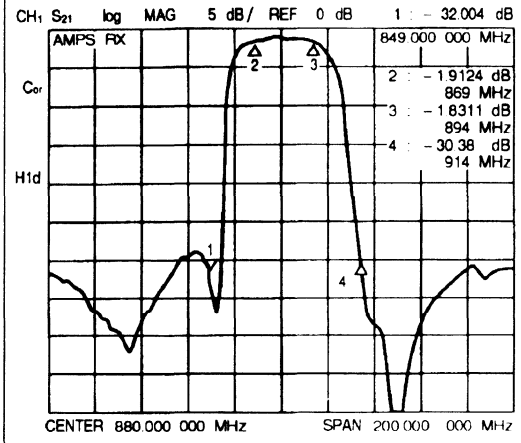


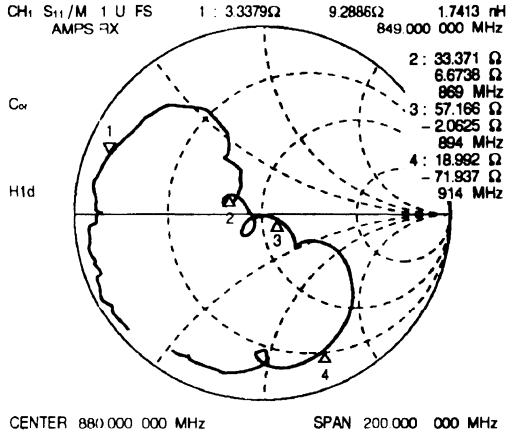


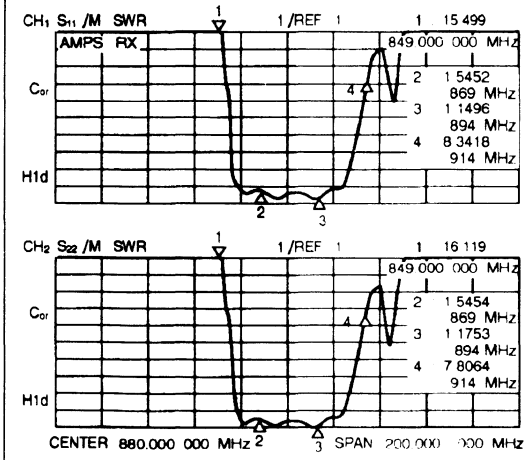


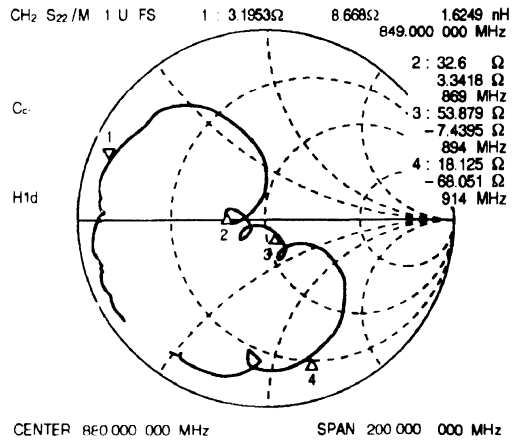
CHARACTERISTIC DATA EXAMPLES (STANDARD VERSION)

2. AMPS / ADC system (Rx) Part number : FAR-F5CC-881M50-L2AB



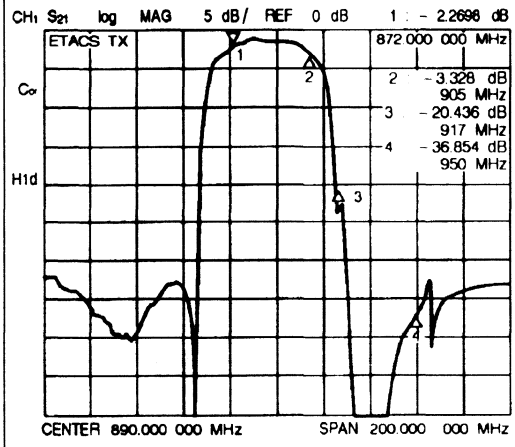


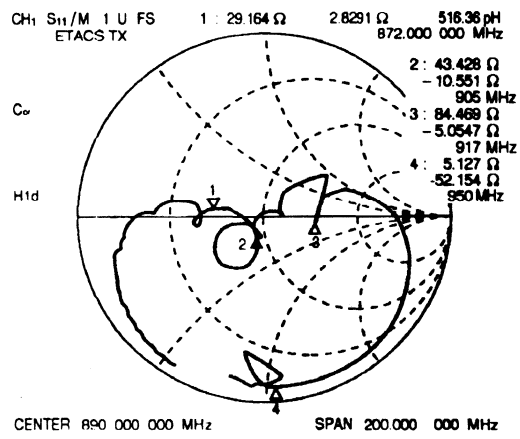


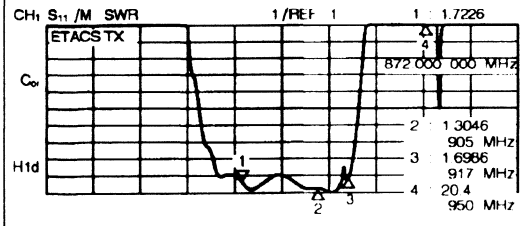


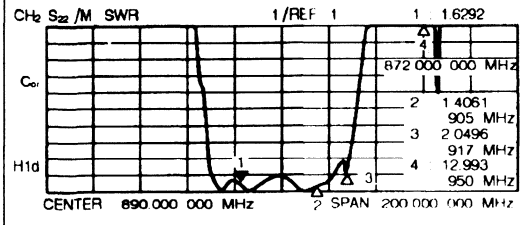
CHARACTERISTIC DATA EXAMPLES (STANDARD VERSION)

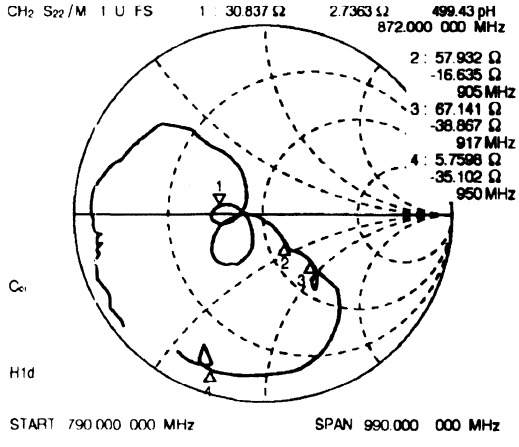
3. ETACS system (Tx) Part number : FAR-F5CC-888M50-L2CA





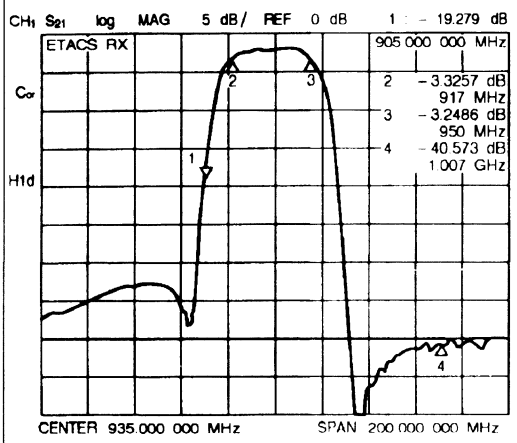


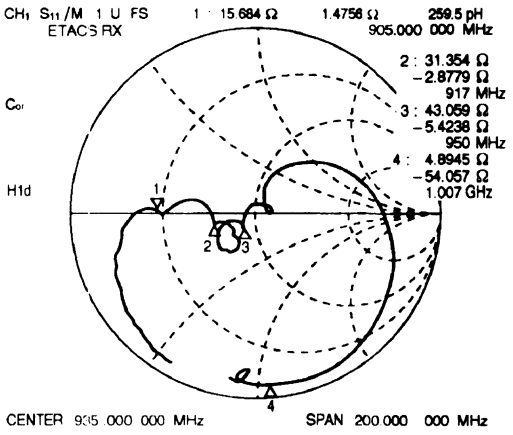


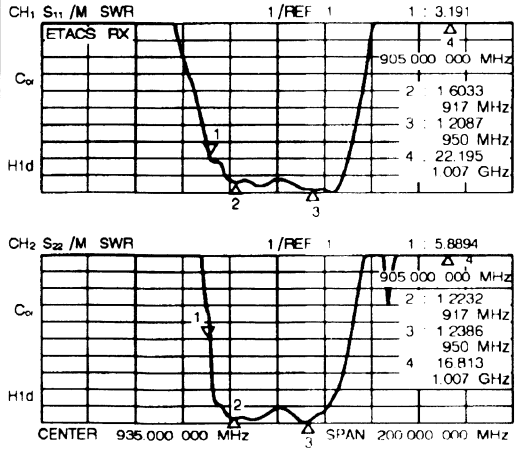


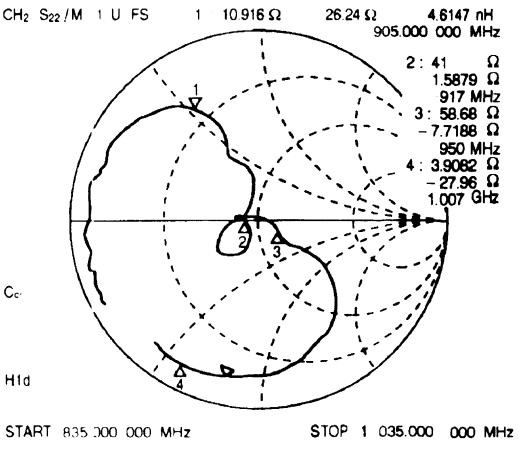
CHARACTERISTIC DATA EXAMPLES (STANDARD VERSION)

4. ETACS system (Rx) Part number : FAR–F5CC–933M50–L2CB



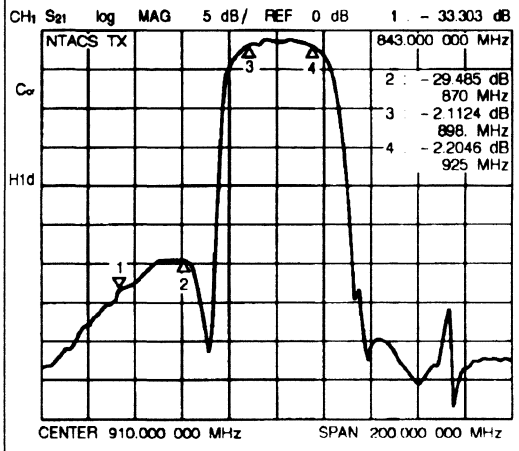


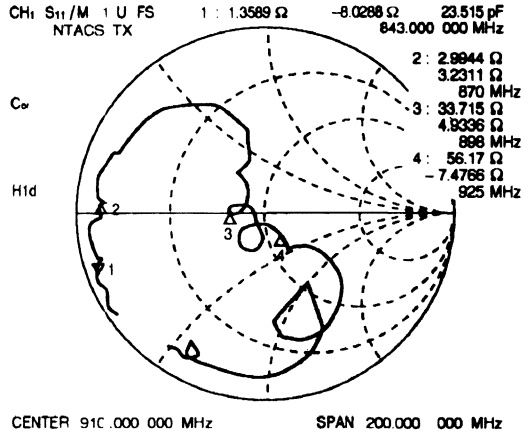


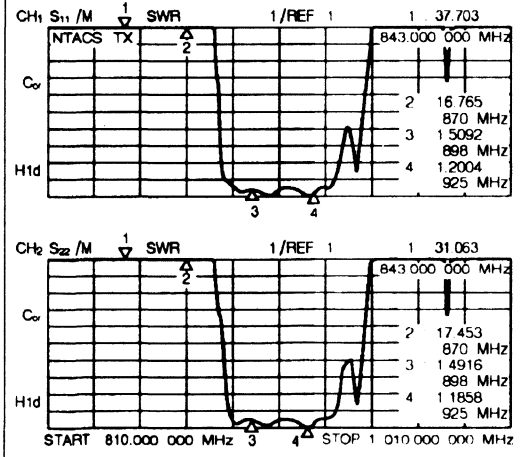


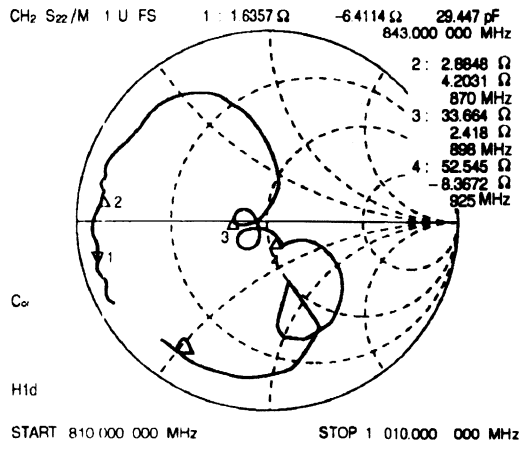
CHARACTERISTIC DATA EXAMPLES (STANDARD VERSION)

5. NTACS system (Tx) Part number : FAR-F5CC-911M50-L2DA



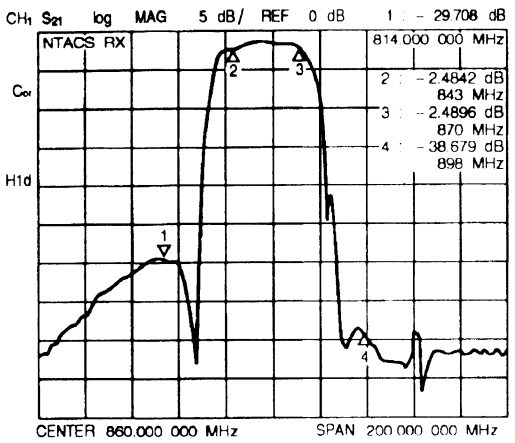


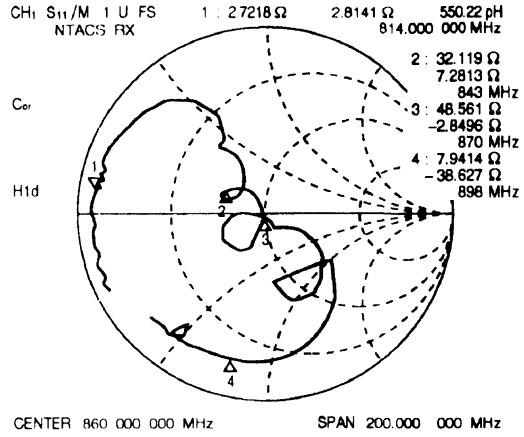


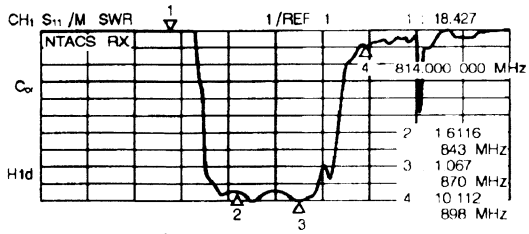


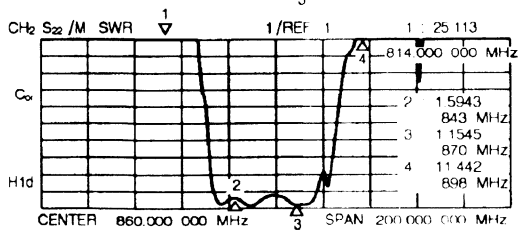
CHARACTERISTIC DATA EXAMPLES (STANDARD VERSION)

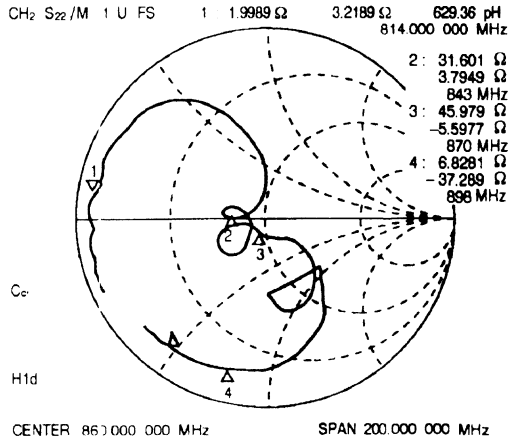
6. NTACS system (Rx) Part number : FAR–F5CC–856M50–L2DB





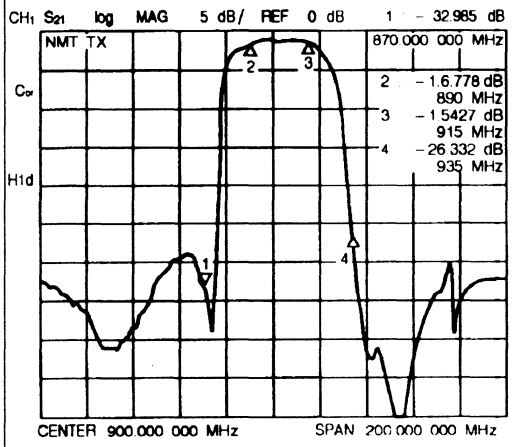


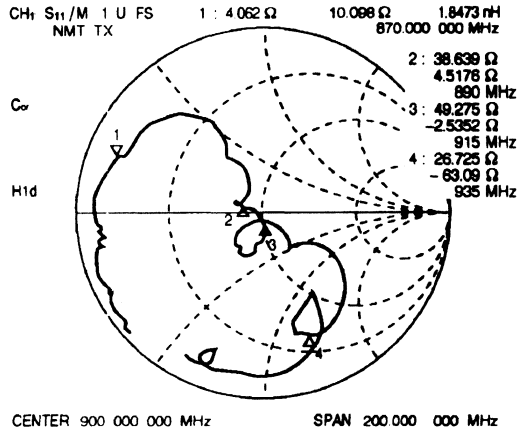


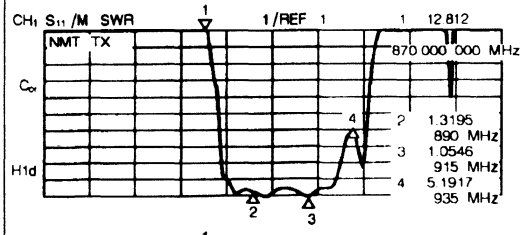


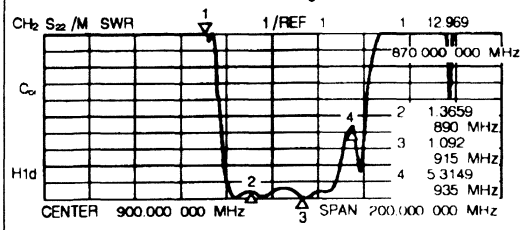
CHARACTERISTIC DATA EXAMPLES (STANDARD VERSION)

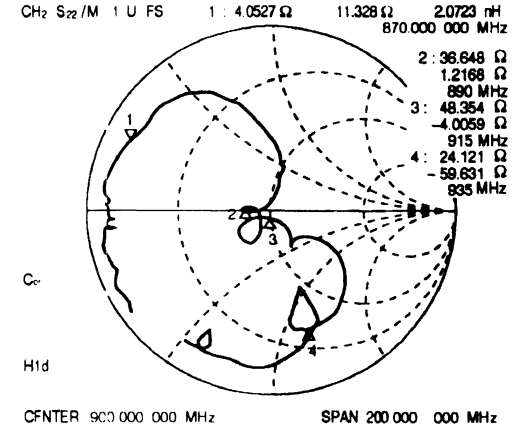
7. NMT / GSM system (Tx) Part number : FAR-F5CC-902M50-L2EA





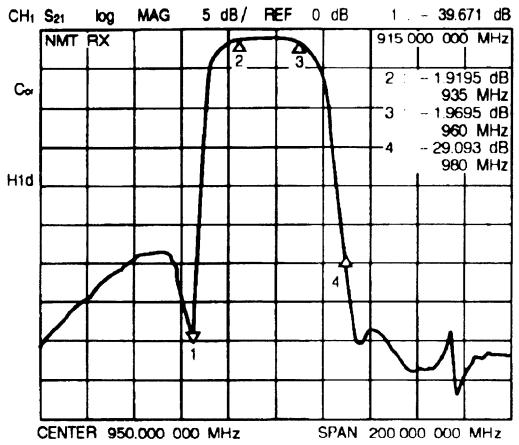


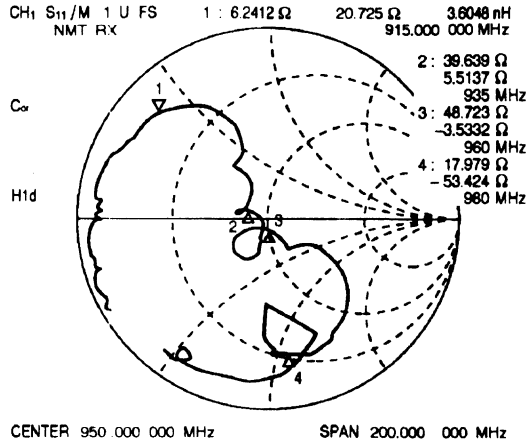


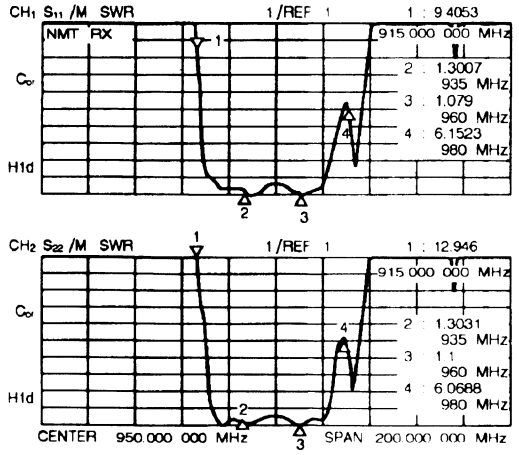


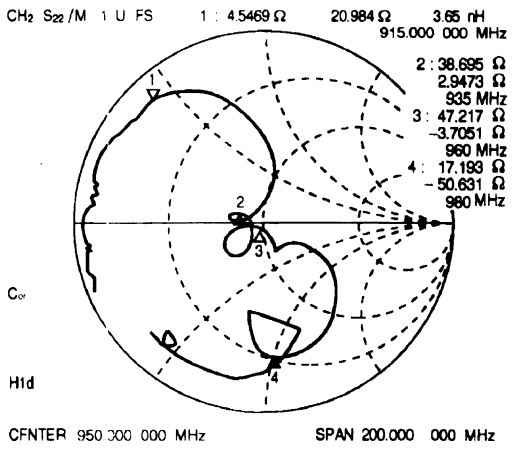
CHARACTERISTIC DATA EXAMPLES (STANDARD VERSION)

8. NMT / GSM system (Rx) Part number : FAR–F5CC–947M50–L2EB



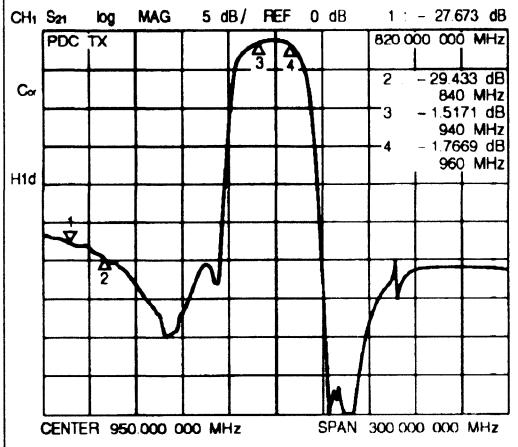


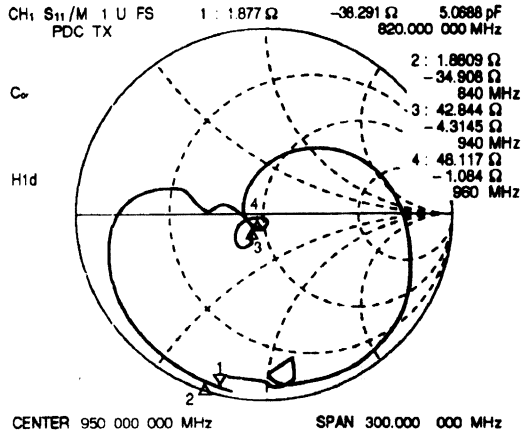


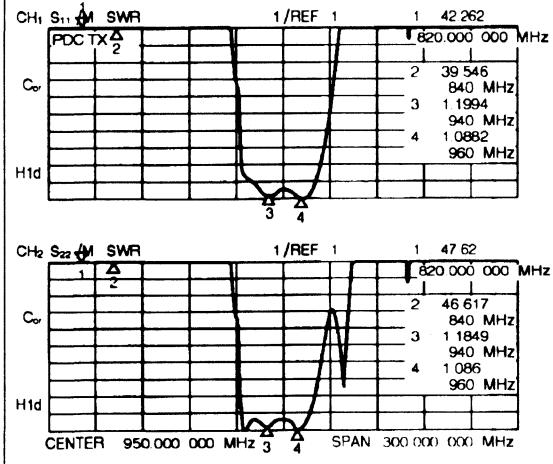


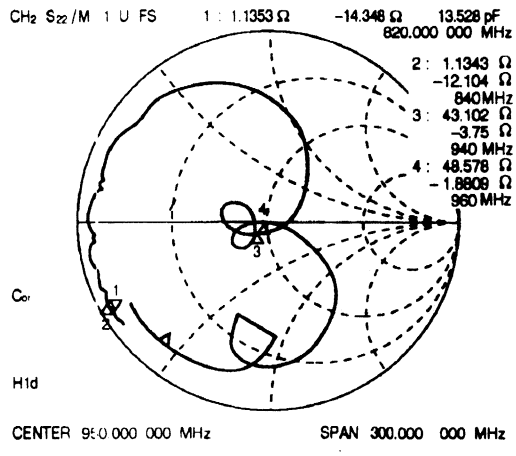
CHARACTERISTIC DATA EXAMPLES (STANDARD VERSION)

9. JDC system (Tx) Part number : FAR-F5CC-950M00-L2FA



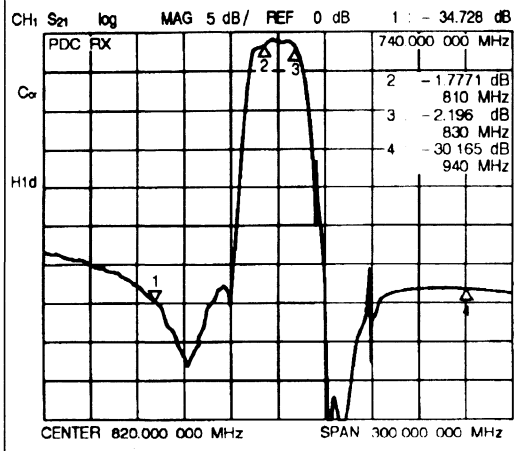


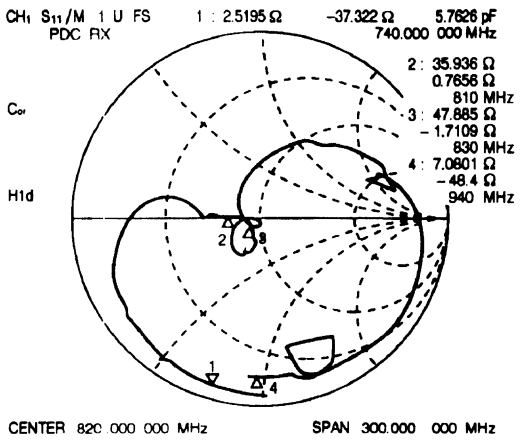


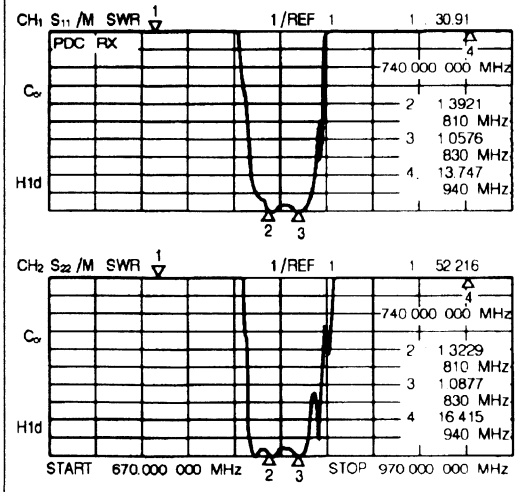


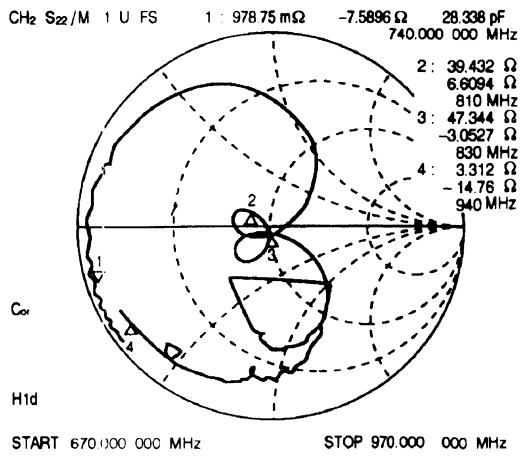
CHARACTERISTIC DATA EXAMPLES (STANDARD VERSION)

10. JDC system (Rx) Part number : FAR-F5CC-820M00-L2FB



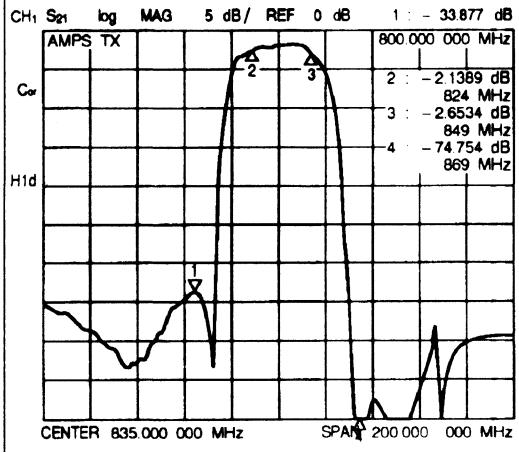


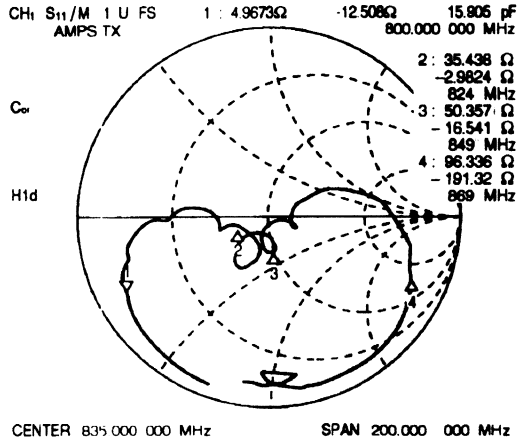


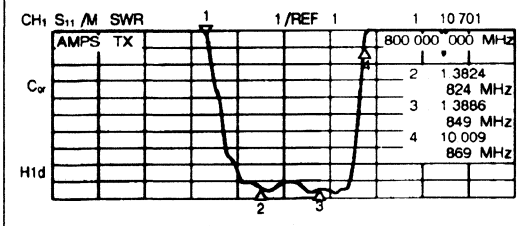


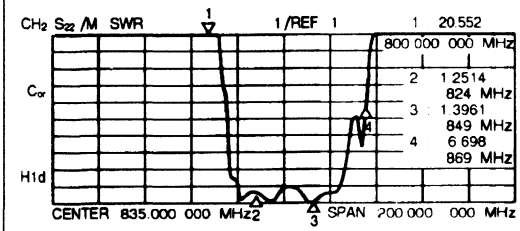
CHARACTERISTIC DATA EXAMPLES (HIGH ATTENUATION VERSION)

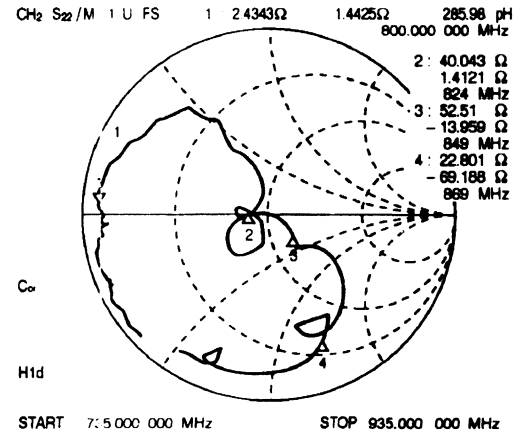
11. AMPS / ADC system (Tx) Part number : FAR-F5CC-836M50-L2AZ





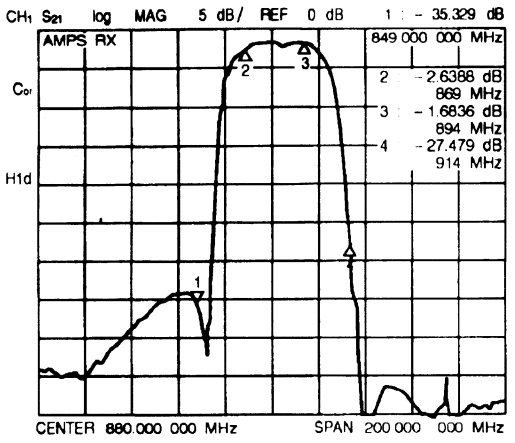


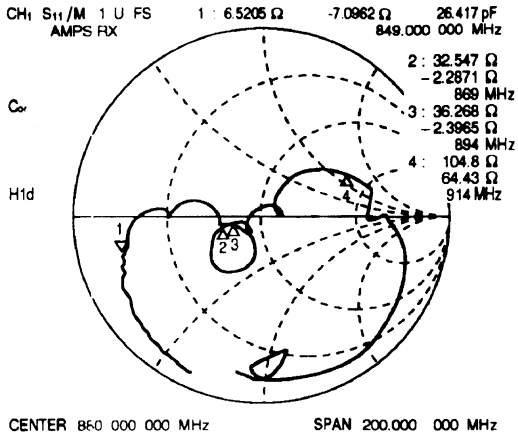


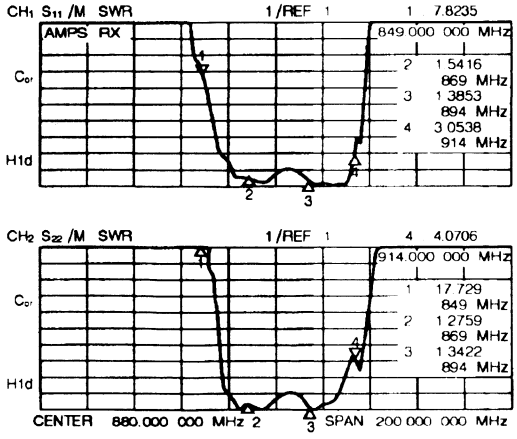


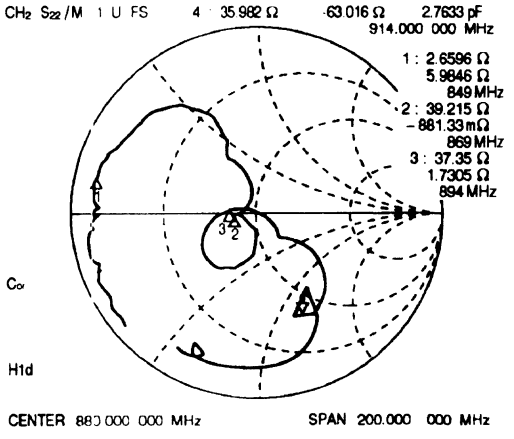
CHARACTERISTIC DATA EXAMPLES (HIGH ATTENUATION VERSION)

12. AMPS / ADC system (Rx) Part number : FAR–F5CC–881M50–L2AY



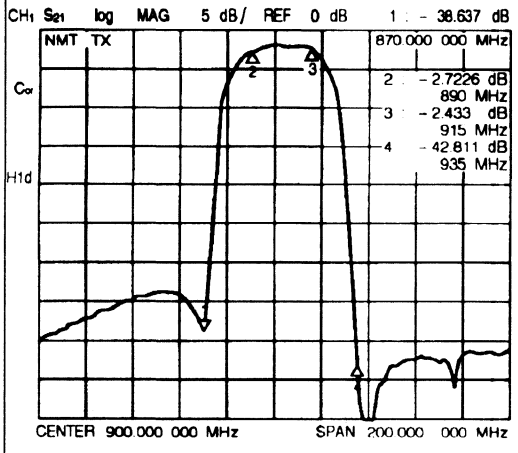


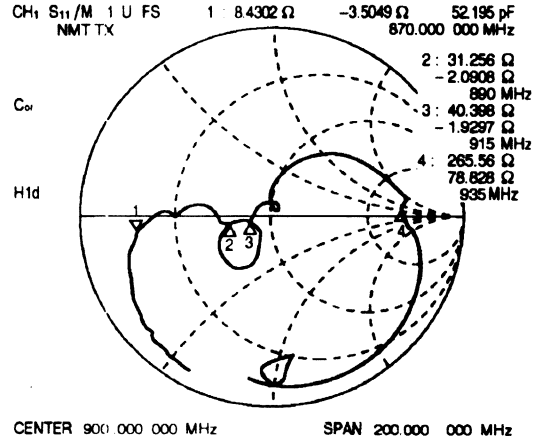


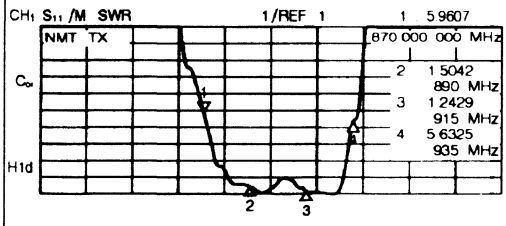


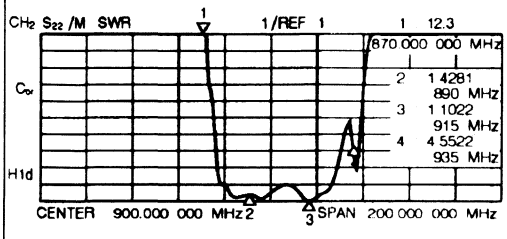
CHARACTERISTIC DATA EXAMPLES (HIGH ATTENUATION VERSION)

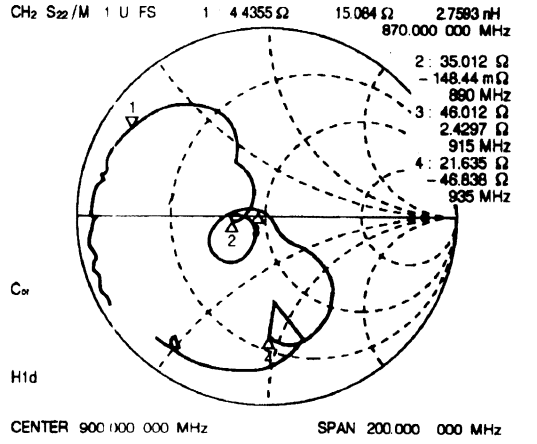
13. NMT / GSM system (Tx) Part number : FAR-F5CC-902M50-L2EZ





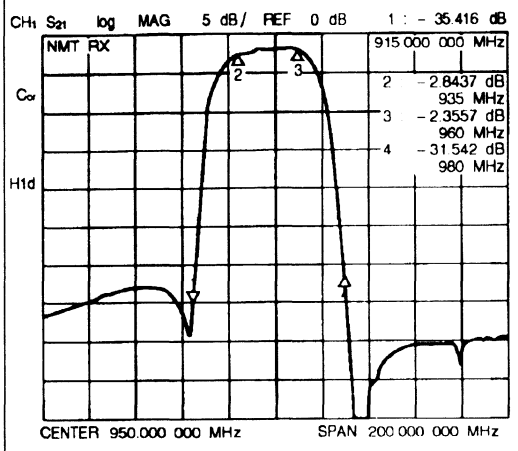


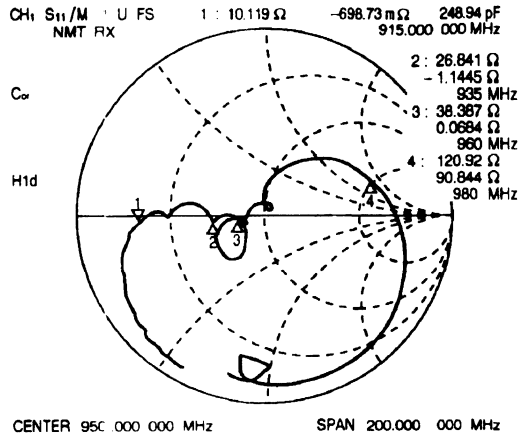


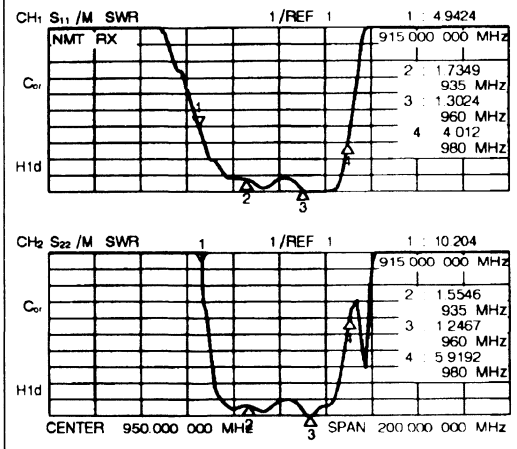


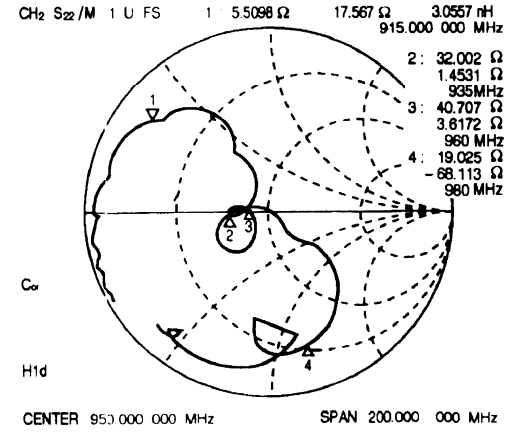
CHARACTERISTIC DATA EXAMPLES (HIGH ATTENUATION VERSION)

14. NMT / GSM system (Rx) Part number : FAR-F5CC-947M50-L2EY

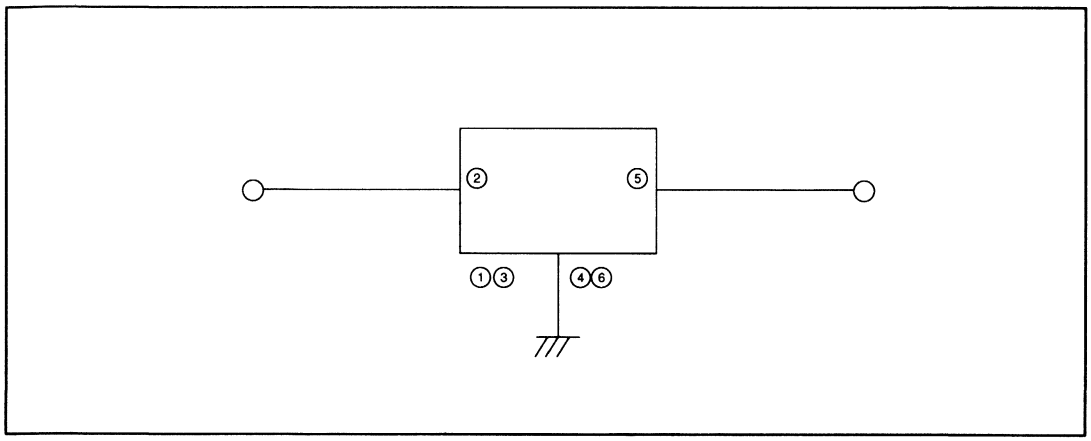








MEASURING CIRCUIT



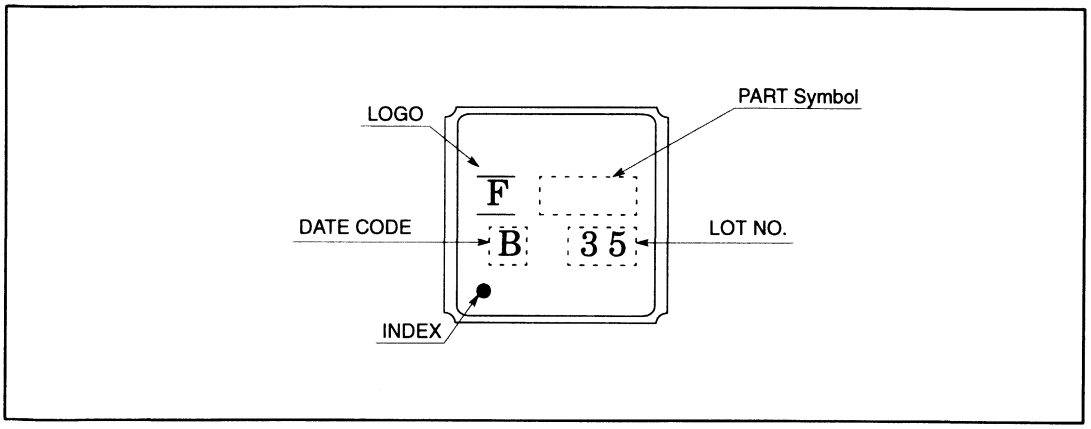
PART NUMBER DESIGNATION

[Designation example]

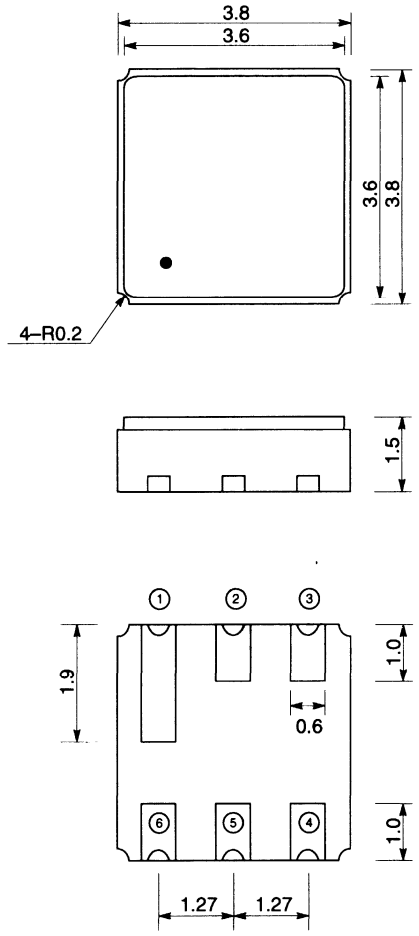
FAR-F5CC- □□□□□□ -L2 □□ -□
① ② ③

① Frequency designation	:	Specify the nominal frequency in six alphanumeric characters. Enter M (for MHz) at the decimal point. Refer to STANDARD FREQUENCIES.
② Serial number.	:	Specify a number from AA to ZZ.
③ Packaging (Reeled tape)	:	T → 1K pcs/reel R → 3K pcs/reel

MARKING



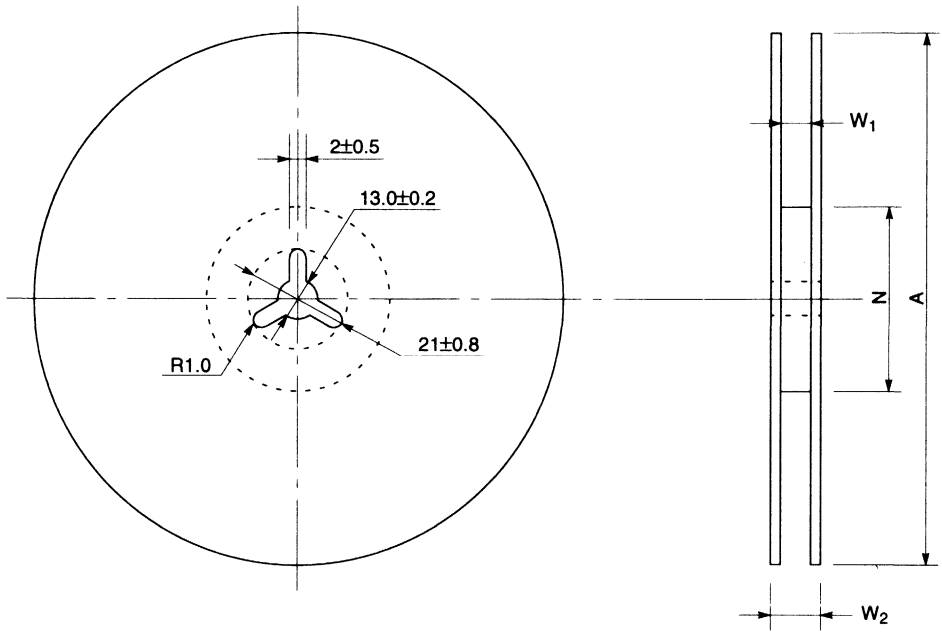
DIMENSIONS



Unit : mm

PACKING : Reel type

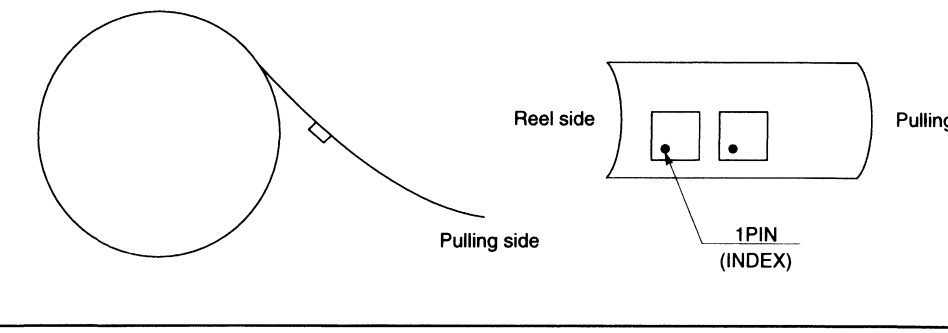
1. Reel dimension



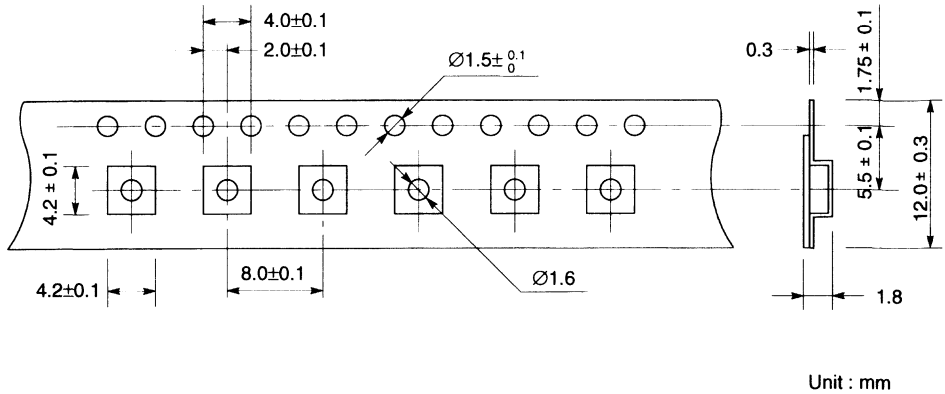
	A	N	W_1	W_2
–T	250	80	$12.4\pm{}^{2.0}_{0.0}$	18.4 or less
–R	330	80	$12.4\pm{}^{2.0}_{0.0}$	18.4 or less

Unit : mm

2. Packing style



3. Tape dimension



FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-23110-1E

ASSP for Mobile Communication Systems

Piezoelectric SAW BPF (1000 to 2500 MHz)

F6 Series (L2 Type)

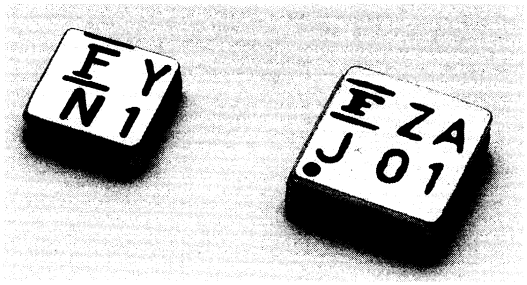
■ DESCRIPTION

The F6 series of SAW bandpass filters apply to the frequency range 1000 to 2500 MHz.
The SAW filters are fabricated on a lithium tantalate ($LiTaO_3$) substrate, producing filters with a wide frequency bandwidth, low insertion loss in passband and superior stability due to the high electromechanical coupling coefficient of the material.
Fujitsu's leading techniques for making filter pattern designs realized this high frequency filter.
The F6 series filters are housed in a small surface mount package. Moreover, the impedance in the passband is 50 ohms, and so applications require no external matching circuits.
The F6 series SAW filters are suitable for interstage RF filter in mobile communication systems in the submicrowave frequency band. Standard devices are available for PDC1.5 G, PCS, DCS1800 and 2.4 GHz Wireless LAN systems.

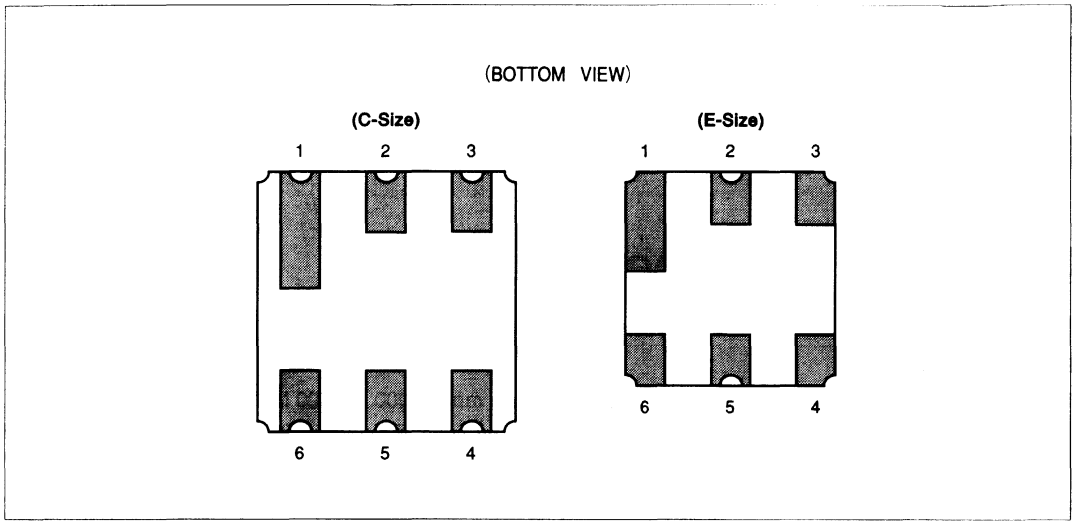
■ FEATURES

- Ultra compact and light package (3.8 mm × 3.0 mm ×)
- External matching circuits are not required.
- Surface mount package (SMT)
- Wide variety of standard devices for worldwide mobile communication systems
- Low insertion loss

■ PACKAGE



■ PIN ASSIGNMENT



■ PIN DESCRIPTIONS

Pin No.	Pin name	Description
1	GND	Ground Pin
2	IN	Input Pin
3	GND	Ground Pin
4	GND	Ground Pin
5	OUT	Output Pin
6	GND	Ground Pin

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Operating temperature	Ta	–30 to +85	°C
Storage temperature	T_{stg}	–40 to +100	°C
Frequency range		1000 to 2500	MHz
Maximum input level	P_{IN}	Refer to electrical characteristics	mW

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Operating temperature	Ta	–30 to +85*	°C

* : Standard Rating for 2.45 GHz Wireless LAN Systems is 0 to +60 °C.

■ STANDARD FREQUENCIES

Center freq. (MHz)	BW (MHz)	System	Part symbol	Part number	Package size
1441.0	24	PDC1.5 G (Tx)	ZA	FAR-F6CC-1G4410-L2ZA	C
1489.0	24	PDC1.5 G (Rx)	ZB	FAR-F6CC-1G4890-L2ZB	C
1619.0	24	PDC1.5 G (Lo)	ZN	FAR-F6CC-1G6190-L2ZN	C
1747.5	75	DCS1800 (Tx)	A	FAR-F6CE-1G7475-L2YA	E
1842.5	75	DCS1800 (Rx)	B	FAR-F6CE-1G8425-L2YB	E
1880.0	60	PCS (Tx)	C	FAR-F6CE-1G8800-L2XA	E
1960.0	60	PCS (Rx)	D	FAR-F6CE-1G9600-L2XB	E
2450.0	100	Wireless LAN	E	FAR-F6CE-2G4500-L2WA	E

■ ELECTRICAL CHARACTERISTICS (STANDARD VERSION)

1. PDC 1.5 G system (Tx)

Part number : FAR-F6CC-1G4410-L2ZA

Ta = –30 to 85 °C

Parameter	Symbol	Condition	Value			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	1429 to 1453 MHz	—	2.6	3.5	dB	
In-band deviation		1429 to 1453 MHz	—	1.0	1.8	dB	
Absolute stopband attenuation		DC to 1200 MHz	20	26	—	dB	
		1200 to 1260 MHz	25	30	—	dB	
		1260 to 1287 MHz	30	34	—	dB	
		1287 to 1380 MHz	25	29	—	dB	
		1477 to 1513 MHz	10	14	—	dB	
		1513 to 1607 MHz	33	39	—	dB	
		1607 to 1631 MHz	35	39	—	dB	
		1631 to 1900 MHz	30	38	—	dB	
		1900 to 2906 MHz	18	20	—	dB	
In-band VSWR		1429 to 1453 MHz	—	1.3	2.0	—	
Max. input power	P_{IN}	1429 to 1453 MHz	200			mW	

2. PDC 1.5 G system (Rx)

Part number : FAR-F6CC-1G4890-L2ZB

Ta = –30 to 85 °C

Parameter	Symbol	Condition	Value			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	1477 to 1501 MHz	—	2.9	3.2	dB	
In-band deviation		1477 to 1501 MHz	—	1.2	1.7	dB	
Absolute stopband attenuation		DC to 130 MHz	30	38	—	dB	
		130 to 958 MHz	20	26	—	dB	
		958 to 1216 MHz	25	27	—	dB	
		1216 to 1241 MHz	30	32	—	dB	
		1241 to 1429 MHz	26	28	—	dB	
		1429 to 1453 MHz	10	17	—	dB	
		1542 to 1566 MHz	20	40	—	dB	
		1566 to 1607 MHz	30	40	—	dB	
		1607 to 1631 MHz	35	40	—	dB	
		1631 to 1737 MHz	30	40	—	dB	
		1737 to 1761 MHz	35	40	—	dB	
		1761 to 1900 MHz	30	37	—	dB	
		1900 to 3000 MHz	15	20	—	dB	
In-band VSWR		1477 to 1501 MHz	—	1.4	2.0	—	
Max. input power	P_{IN}	1477 to 1501 MHz		200		mW	

3. PDC 1.5 G system (Lo)

Part number : FAR-F6CC-1G6190-L2ZN

Ta = –30 to 85 °C

Parameter	Symbol	Condition	Value			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	1607 to 1631 MHz	—	3.0	4.0	dB	
In-band deviation		1607 to 1631 MHz	—	1.5	2.0	dB	
Absolute stopband attenuation		DC to 130 MHz	30	38	—	dB	
		130 to 1501 MHz	25	28	—	dB	
		1737 to 1809 MHz	30	35	—	dB	
		1809 to 2500 MHz	20	29	—	dB	
		3214 MHz	15	25	—	dB	
In-band VSWR		1607 to 1631 MHz	—	1.6	2.0	—	
Max. input power	P_{IN}	1607 to 1631 MHz	200			mW	

4. DCS 1800 system (Tx)
Part number : FAR-F6CE-1G7475-L2YA

Ta = –30 to 85 °C

Parameter	Symbol	Condition	Value			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	1710 to 1785 MHz	—	3.5	4.5	dB	
In-band deviation		1710 to 1785 MHz	—	2.0	3.0	dB	
Absolute stopband attenuation		DC to 1500 MHz	15	17	—	dB	
		1500 to 1670 MHz	20	22	—	dB	
		1805 to 1880 MHz	5	10	—	dB	
		1880 to 2200 MHz	22	24	—	dB	
		3420 to 3570 MHz	25	27	—	dB	
		5130 to 5355 MHz	10	20	—	dB	
In-band VSWR		1710 to 1785 MHz	—	2.0	3.0	—	
Max. input power	P_{IN}	1710 to 1785 MHz	T.B.D.			mW	

5. DCS 1800 system (Rx)
Part number : FAR-F6CE-1G8425-L2YB

Ta = –30 to 85 °C

Parameter	Symbol	Condition	Value			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	1805 to 1880 MHz	—	3.9	4.8	dB	
In-band deviation		1805 to 1880 MHz	—	2.0	2.5	dB	
Absolute stopband attenuation		DC to 1500 MHz	21	23	—	dB	
		1600 to 1710 MHz	26	28	—	dB	
		1710 to 1785 MHz	8	24	—	dB	
		1920 to 2400 MHz	22	24	—	dB	
		3610 to 3760 MHz	22	25	—	dB	
In-band VSWR		1805 to 1880 MHz	—	2.0	3.0	—	
Max. input power	P_{IN}	1805 to 1880 MHz	T.B.D.			mW	

6. PCS system (Tx)

Part number : FAR-F6CE-1G8800-L2XA

Ta = –30 to 85 °C

Parameter	Symbol	Condition	Value			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	1850 to 1910 MHz	—	3.5	4.5	dB	
In-band deviation		1850 to 1910 MHz	—	1.5	2.5	dB	
Absolute stopband attenuation		DC to 1500 MHz	22	24	—	dB	
		1500 to 1800 MHz	25	28	—	dB	
		1930 to 1990 MHz	5	8	—	dB	
		3700 to 3820 MHz	20	24	—	dB	
		5550 to 5730 MHz	4	5	—	dB	
In-band VSWR		1850 to 1910 MHz	—	1.8	2.5	—	
Max. input power	P_{IN}	1850 to 1910 MHz	T.B.D.			mW	

7. PCS system (Rx)

Part number : FAR-F6CE-1G9600-L2XB

Ta = –30 to 85 °C

Parameter	Symbol	Condition	Value			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	1930 to 1990 MHz	—	4.0	4.8	dB	
In-band deviation		1930 to 1990 MHz	—	2.0	2.8	dB	
Absolute stopband attenuation		DC to 1500 MHz	22	24	—	dB	
		1500 to 1850 MHz	25	28	—	dB	
		1850 to 1910 MHz	10	25	—	dB	
		3920 to 4040 MHz	20	23	—	dB	
In-band VSWR		1930 to 1990 MHz	—	1.8	2.5	—	
Max. input power	P_{IN}	1930 to 1990 MHz	T.B.D.			mW	

8. Wireless-LAN system

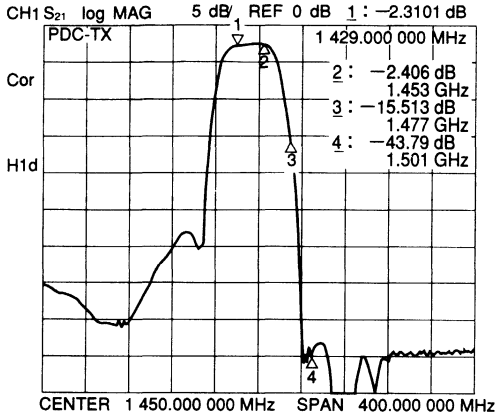
Part number : FAR-F6CE-2G4500-L2WA

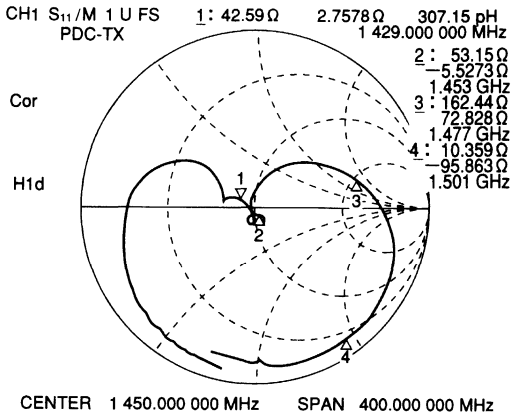
Ta = 0 to 60 °C

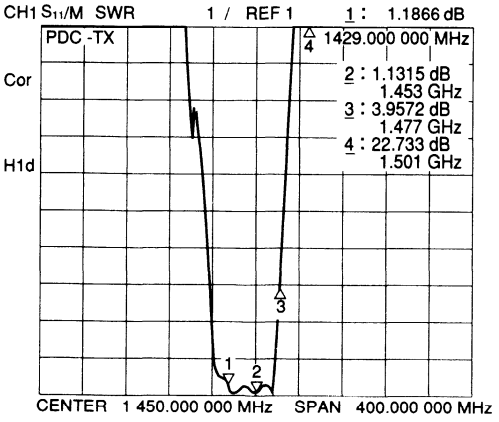
Parameter	Symbol	Condition	Value			Unit	Remarks
			Min.	Typ.	Max.		
Insertion loss	IL	2400 to 2500 MHz	—	4.5	5.5	dB	
In-band deviation		2400 to 2500 MHz	—	2.3	3.5	dB	
Absolute stopband attenuation		DC to 1700 MHz	20	25	—	dB	
		1800 to 2200 MHz	25	28	—	dB	
		2700 to 3100 MHz	30	34	—	dB	
		4800 to 5000 MHz	15	18	—	dB	
In-band VSWR		2400 to 2500 MHz	—	2.0	3.0	—	
Max. input power	P_{IN}	2400 to 2500 MHz		1		mW	

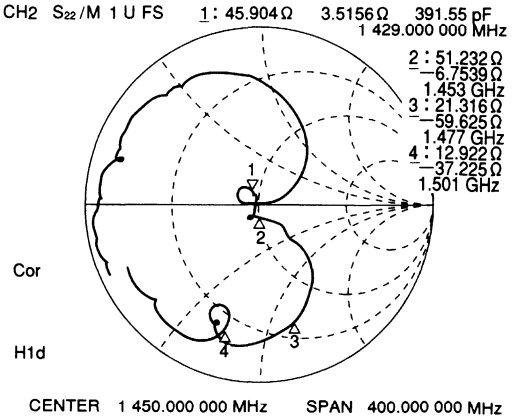
■ TYPICAL CHARACTERISTICS (STANDARD VERSION)

1. PDC 1.5 G system (Tx)
Part number : FAR-F6CC-1G4410-L2ZA









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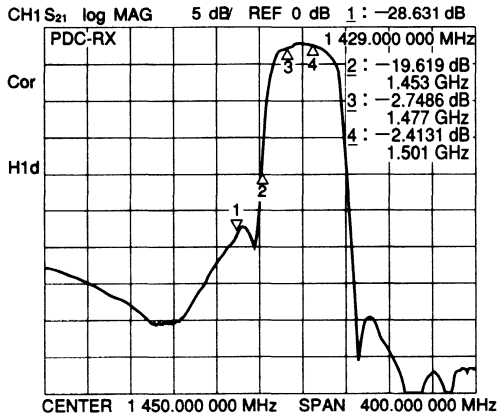
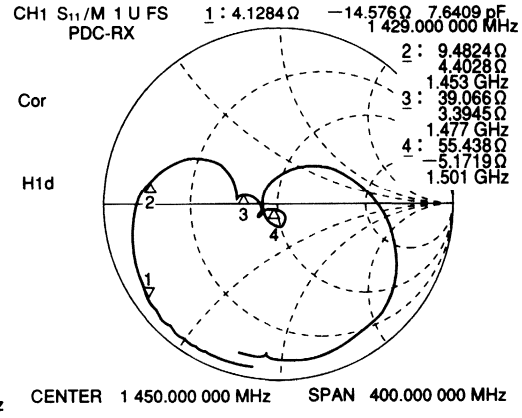
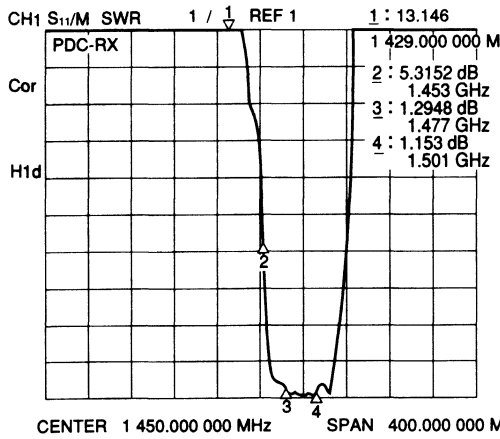
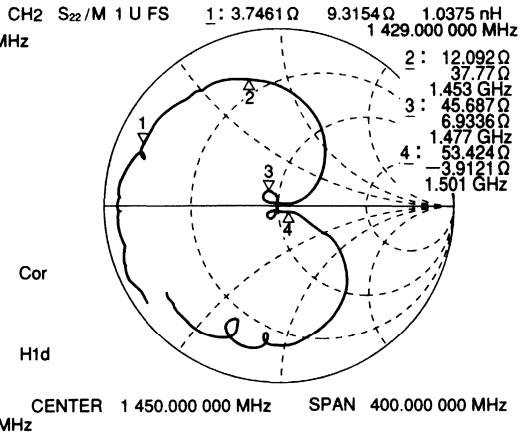
2. PDC 1.5 G system (Rx)
Part number : FAR-F6CC-1G4890-L2ZB









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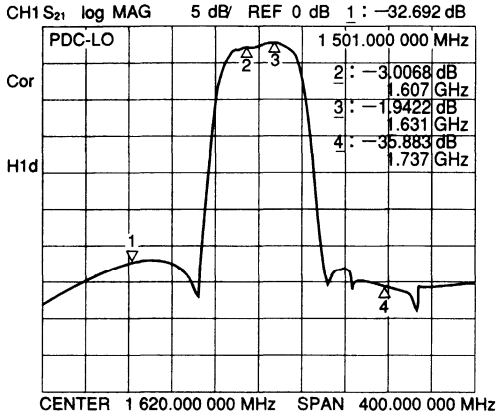
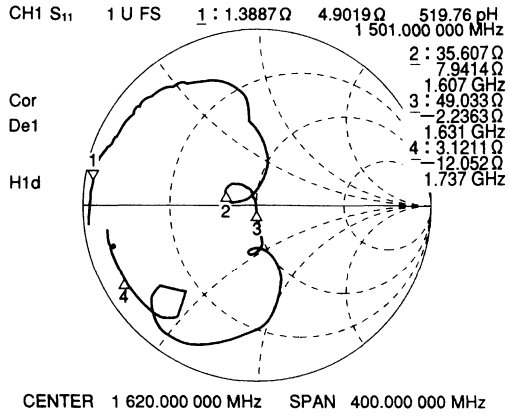
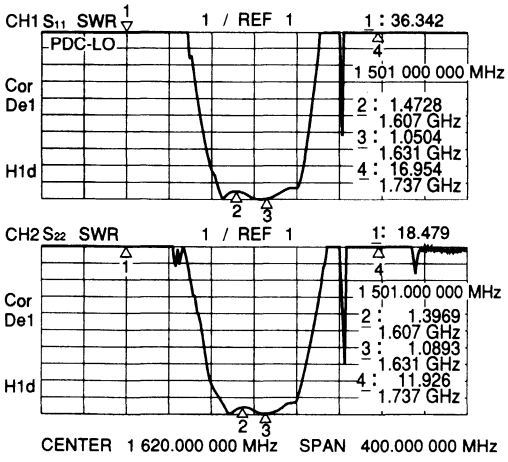
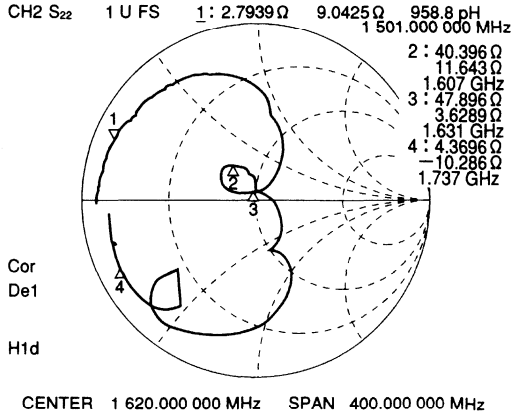
3. PDC 1.5 G system (Lo)
Part number : FAR-F6CC-1G6190-L2ZN









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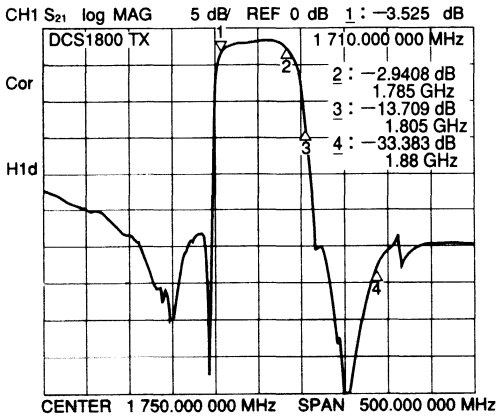
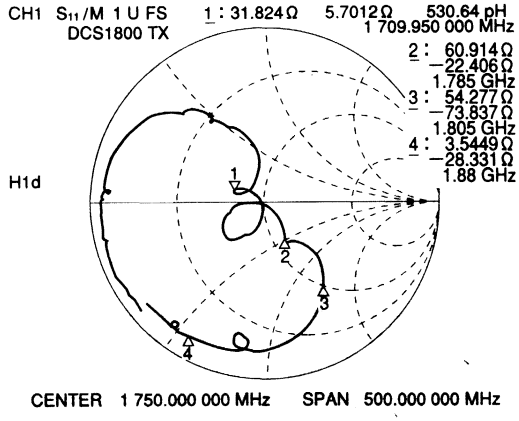
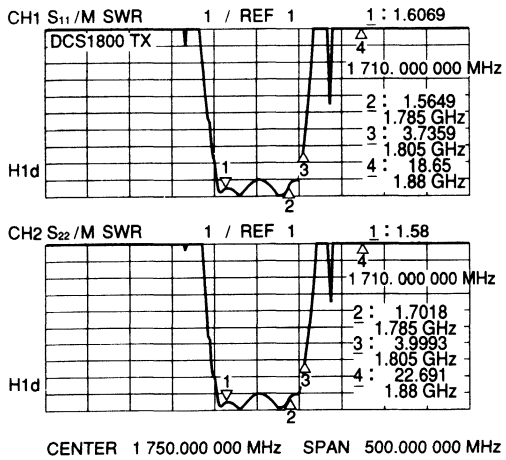
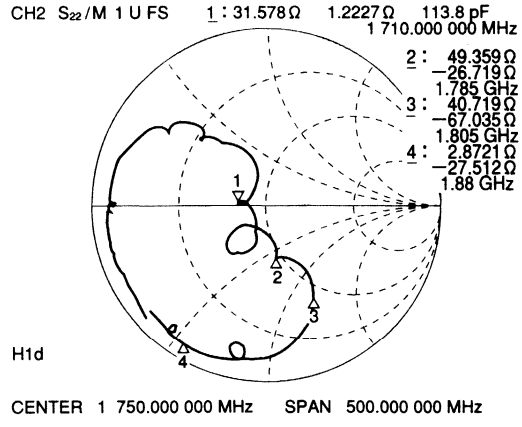
4. DCS 1800 system (Tx)
Part number : FAR-F6CE-1G7475-L2YA









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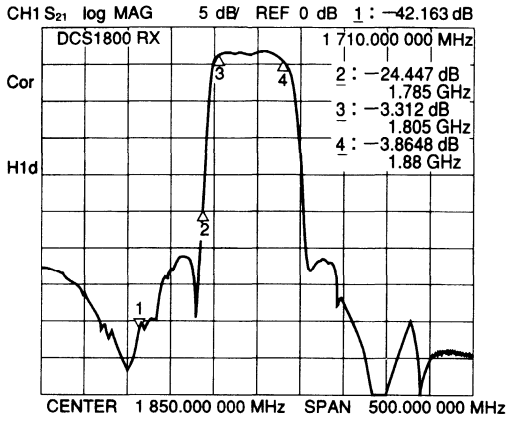
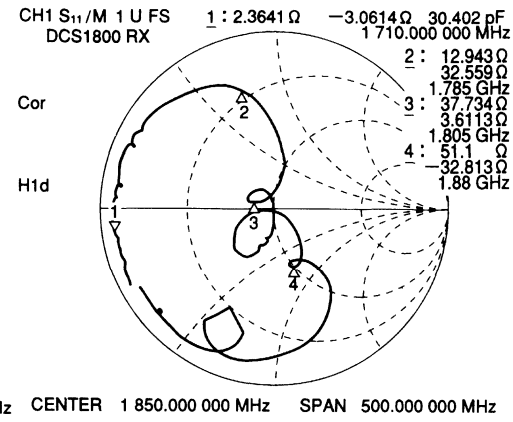
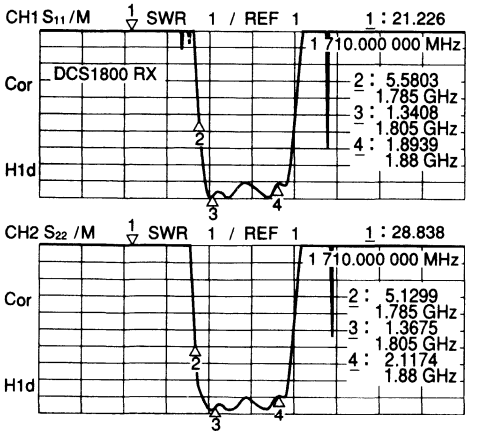
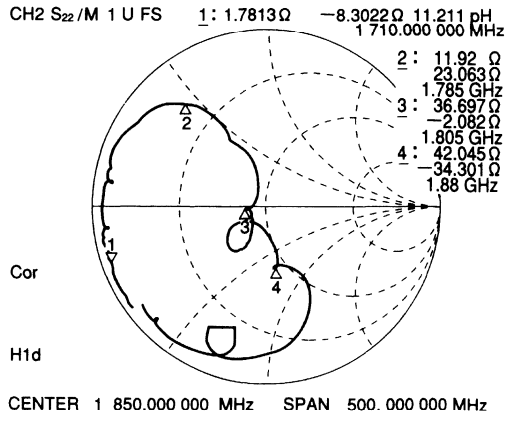
5. DCS 1800 system (Rx)
Part number : FAR-F6CE-1G8425-L2YB









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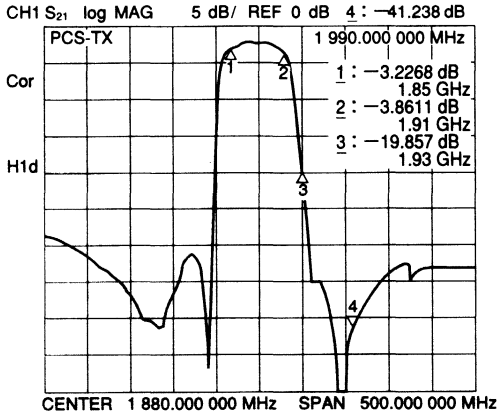
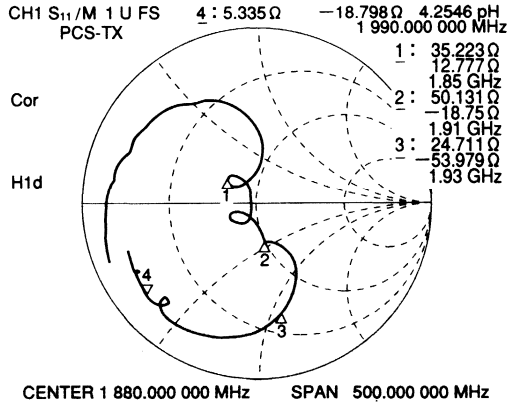
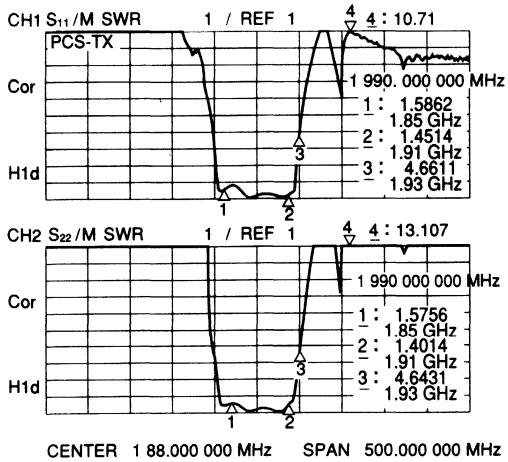
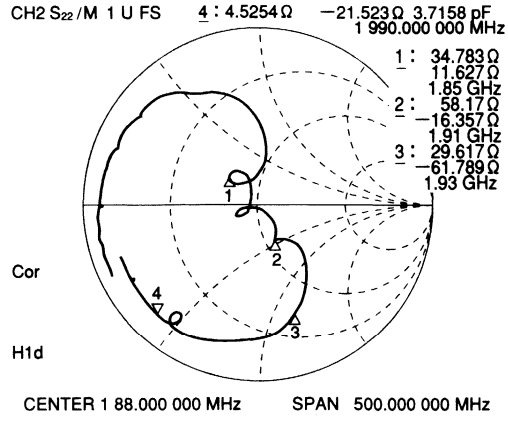
6. PCS system (Tx) **Preliminary**

Part number : FAR-F6CE-1G8800-L2XA









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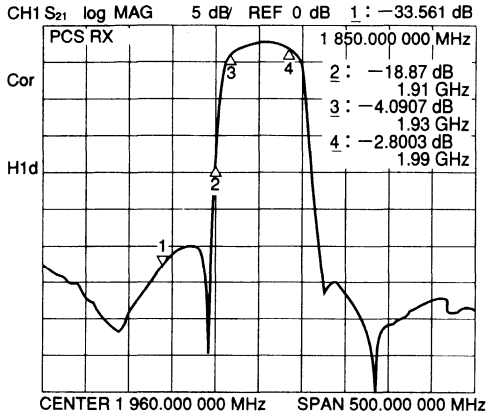
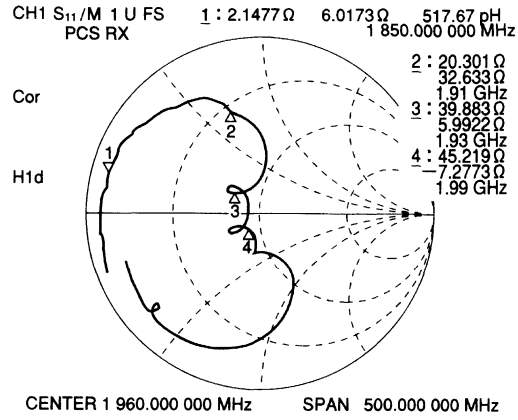
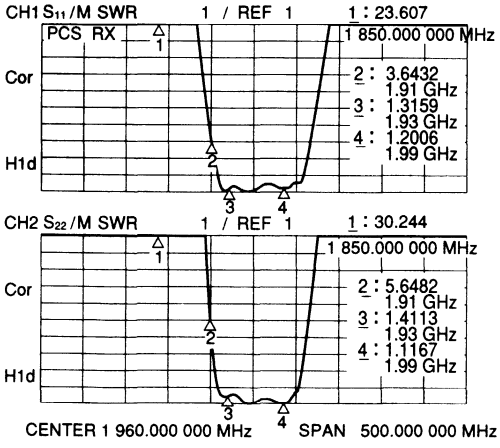
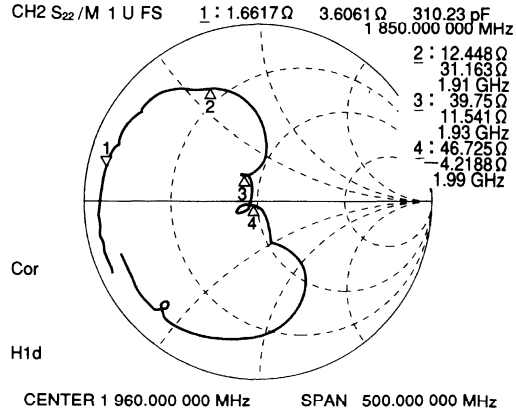
7. PCS system (Rx) **Preliminary**
Part number : FAR-F6CE-1G9600-L2XB









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8. Wireless-LAN system **Preliminary**
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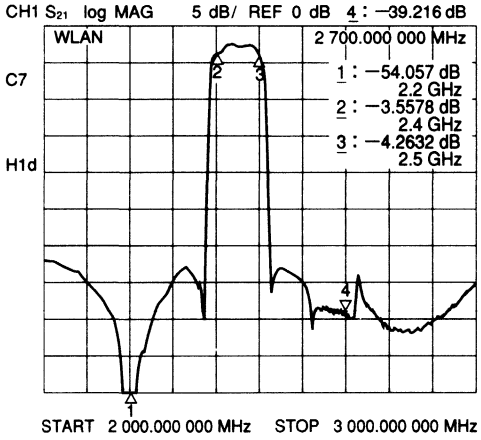
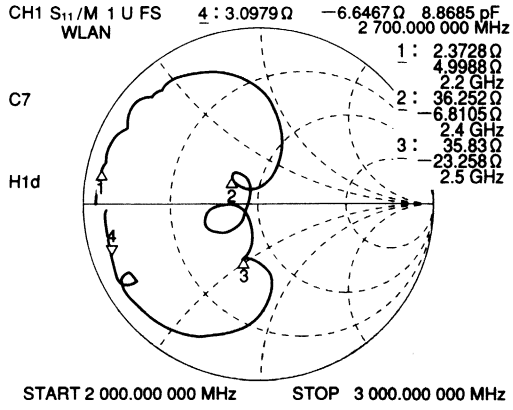
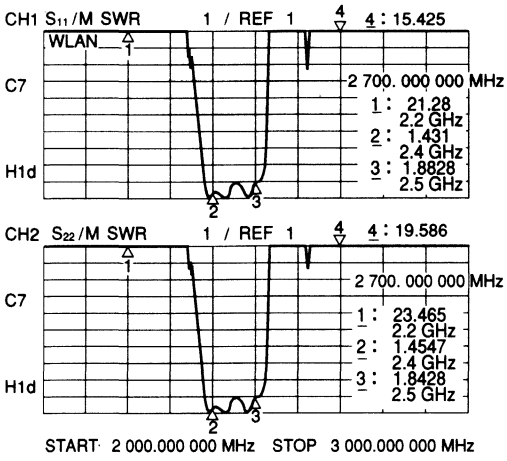
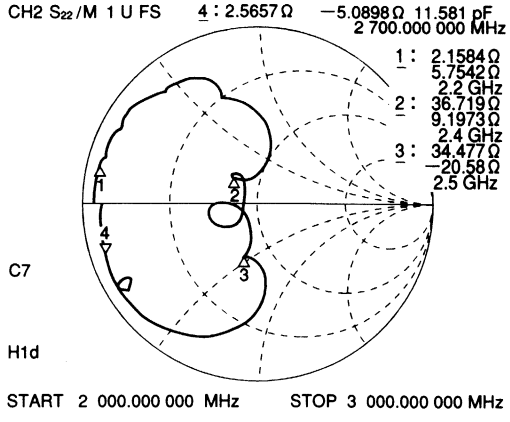
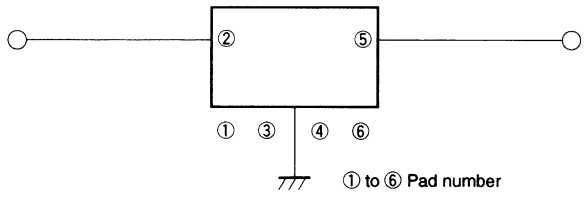








■ MEASURING CIRCUIT



■ PART NUMBER DESIGNATION

[Designation example]

FAR – F6C□ – □□□□□□ – L2□□ – □

① ② ③ ④

① Package designation: C: 3.8 mm□ × 1.6 mm

E: 3.0 mm□ × 1.2 mm

Refer to "■ standard frequencies"

② Frequency designation: Specify the nominal frequency in six alphanumeric characters. Enter G(for GHz) at the decimal point. Refer to standard frequencies.

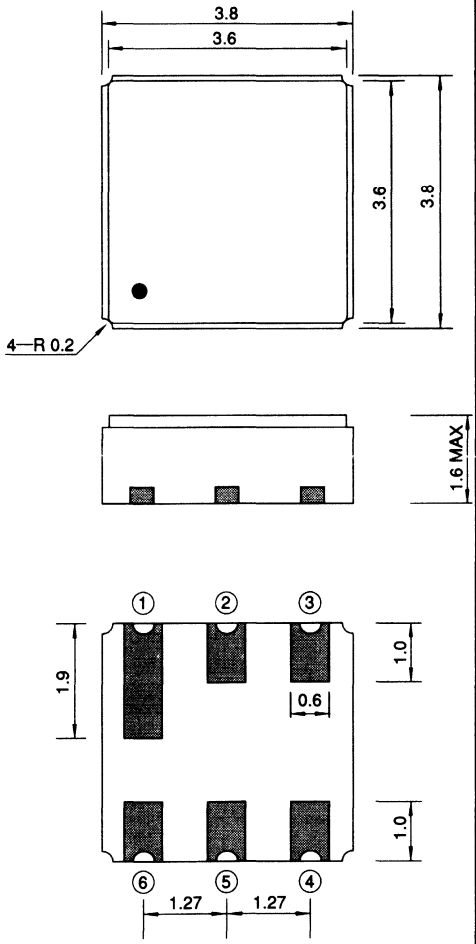
[Example] 1.4410 GHz → 1 G 4410

③ Serial number: Specify a characters from WA to ZZ. Refer to standard frequencies.

④ Packing: (Reeled tape) T : 1 K pcs/reel
R : 3 K pcs/reel

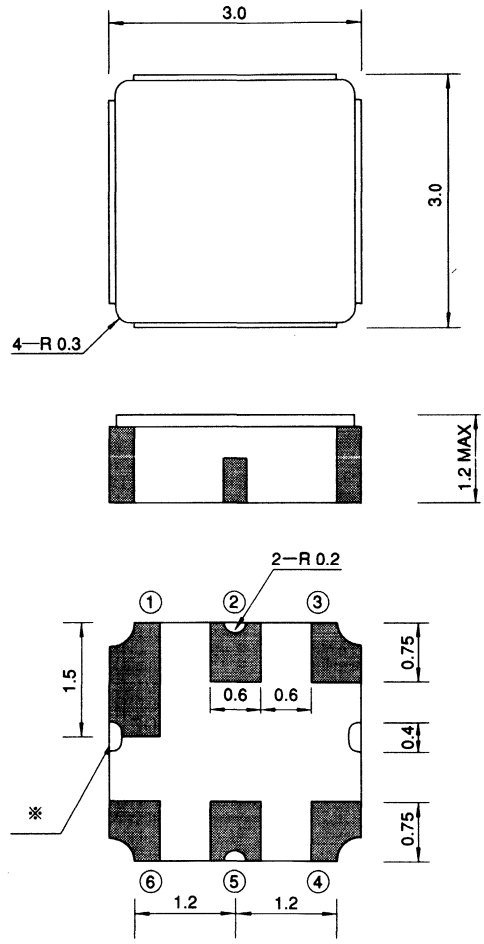
■ PACKAGE DIMENSIONS

(C-SIZE)



Dimensions in mm.

(E-SIZE)

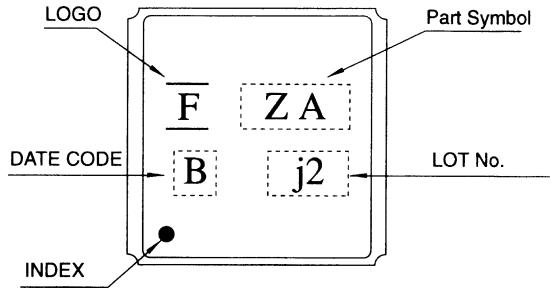


Dimensions in mm.

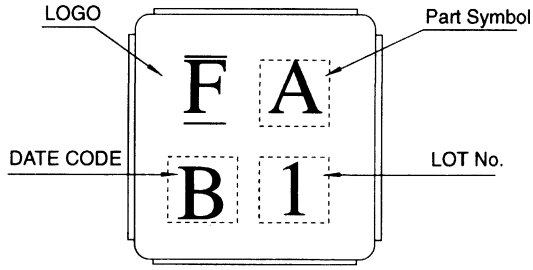
*There are some package types don't have castration.

■ MARKING

(C-SIZE)

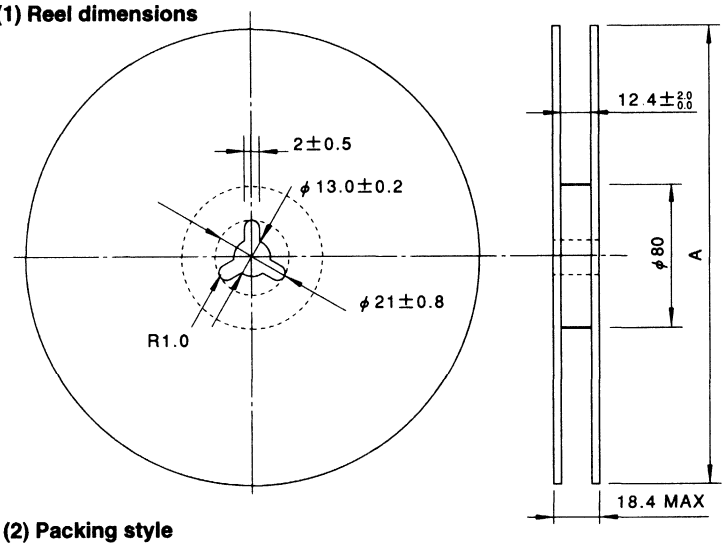


(E-SIZE)



■ PACKING : Reel type

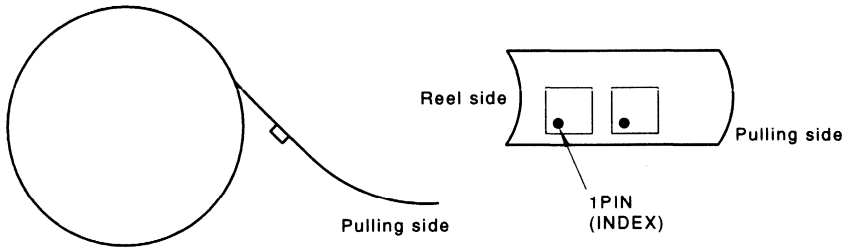
(1) Reel dimensions



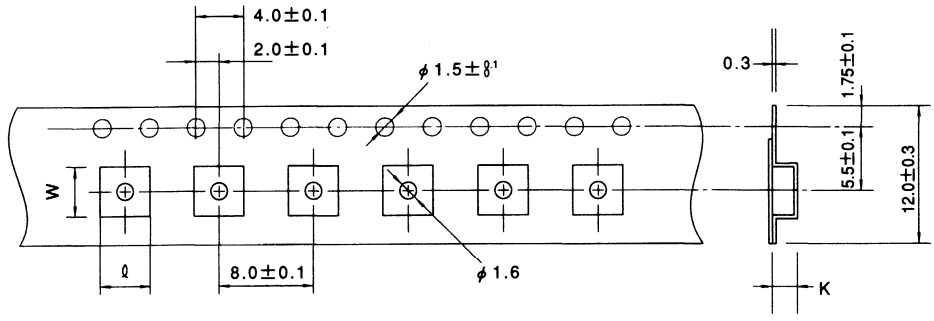
Type	A	Volume
–T	250	1 Kpcs
–R	330	3 Kpcs

Dimensions in mm.

(2) Packing style



(3) Tape dimensions



Package	ℓ	W	K
C	4.2 ± 0.1	4.2 ± 0.1	1.8
E	3.4 ± 0.1	3.4 ± 0.1	1.5

Dimensions in mm.

MEMO

5 PCM Transmission Products

FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-20100-3E

ASSP

PIEZO-ELECTRIC DEVICE

F1/F2/F3 SERIES

TIMING EXTRACTION BANDPASS FILTER (1.5 TO 100MHz)

■ OVERVIEW

The F1,F2, and F3 Series were developed as timing extraction filters for primary, secondary, and tertiary digital communication devices.

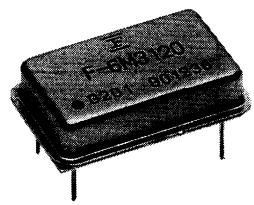
This new all-solid-state bandpass filter (BPF) uses a piezoelectric with a large electromechanical coefficient (lithium tantalate: $LiTaO_3$). The filter has a wide bandwidth, and is very stable.

■ FEATURES

- Wide frequency range 1.5 to 100MHz
- Wide fractional bandwidth (%): 0.1 to 2.5
- Low insertion loss: 6dB or less
- Excellent temperature characteristics: 1.5 to 35MHz: ±400ppm or less (0 to 60°C)
  36 to 100MHz: –30ppm/°C (0 to 60°C)
- Small frequency deviation Δf_o <±500ppm eliminating the need for adjustment
- Highly reliable hermetically sealed package
- Compatible with small 14-pin DIP IC

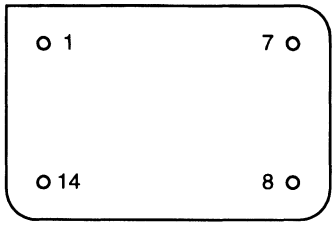
■ PACKAGE

14-PIN DIP SIZE METAL CASE



■ PIN ASSIGNMENT

(BOTTOM VIEW)



Pin No.	Pin name	Description
1	IN	Input pin
7	GND	Ground pin
8	NC	No connection
14	OUT	Output pin

■ MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Operating temperature	T_a	–20 to 80	°C
Storage temperature	T_{stg}	–40 to 80	°C
Insulation resistance	IR	100 (100V DC)	MΩ
Frequency range		1.5 to 100	MHz

■ RECOMMENDED OPERATING CONDITIONS

Item	Symbol	Rating	Unit
Operating temperature	T_a	0 to 70	°C

■ STANDARD FREQUENCY

Series	Standard frequency	Application	Remarks
F1	1.544 MHz	For the U.S. and Japan (primary group)	
	2.048 MHz	For Europe (primary group)	
	3.088 MHz	For the U.S. and Japan (primary group)	1.544 x 2
	3.152 MHz	For the U.S. and Japan (primary group)	
	4.096 MHz	For Europe (primary group)	2.048 x 2
	6.312 MHz	For the U.S. and Japan (secondary group)	
	8.192 MHz	For the U.S. and Japan (secondary group)	
	8.448 MHz	For Europe (secondary group)	
	12.624 MHz	For the U.S. and Japan (secondary group)	6.312 x 2
	16.384 MHz	For the U.S. and Japan (secondary group)	8.192 x 2
F2	16.896 MHz	For Europe (secondary group)	8.448 x 2
	32.064 MHz	For Japan (tertiary group)	
	34.368 MHz	For Europe (tertiary group)	
F3	44.736 MHz	For the U.S. (tertiary group)	

■ ELECTRICAL CHARACTERISTICS

F1 Series

Item	Symbol	Condition	Rating			Unit	Remarks
			Minimum	Typical	Maximum		
Frequency deviation	Δf_o		–500	—	+500	ppm	f_o standard
Load Q	Q		1000	—	40		
Insertion loss	IL			—	6	dB	
Stop band attenuation	A_{OUT}	f_o±10 MHz	20	—	—	dB	
Frequency stability with temperature	Δf (Ta)		–400	—	+400	ppm	25°C standard, Ta= 0 to 70°C

F2 Series

Item	Symbol	Condition	Rating			Unit	Remarks
			Minimum	Typical	Maximum		
Frequency deviation	Δf_o		–500	—	+500	ppm	f_o standard
Load Q	Q		1000	—	40		
Insertion loss	IL			—	6	dB	
Stop band attenuation	A_{OUT}	f_o±10 MHz	20	—	—	dB	
Frequency stability with temperature	Δf (Ta)		–400	—	+400	ppm	25°C standard, Ta= 0 to 70°C

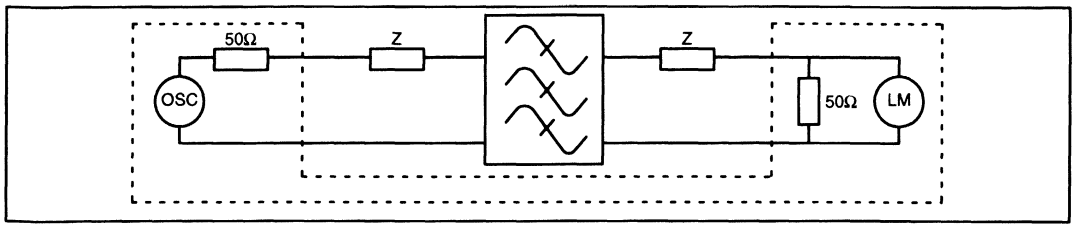
F3 Series

Item	Symbol	Condition	Rating			Unit	Remarks
			Minimum	Typical	Maximum		
Frequency deviation	Δf_o		–500	—	+500	ppm	f_o standard
Load Q	Q		200	—	50		
Insertion loss	IL			—	6	dB	
Stop band attenuation	A_{OUT}	f_o±10 MHz	20	—	—	dB	
Frequency stability with temperature	Δf (Ta)		–1350	—	750	ppm	25°C standard, Ta= 0 to 70°C

■ ELECTRICAL CHARACTERISTICS

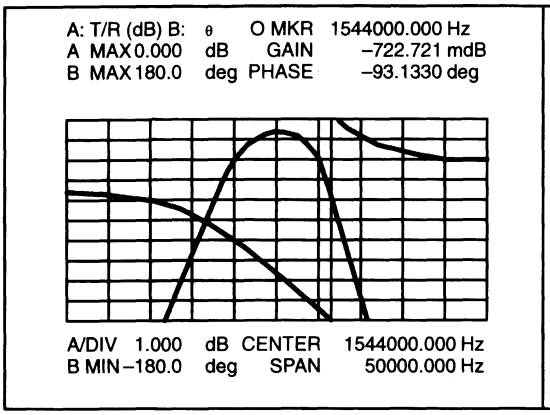
No.	Standard frequency (MHz)	Part number	Specification			
			Load Q	Insertion loss, IL (dB)	Phase rotation θ (degree)	Terminating impedance Z (Ω)
1	1.544	FAR-F1DA-1M5440-G201	110 ±20	3 or less	−90±20	790
2	1.544	FAR-F1DA-1M5440-G202	110 ±20	3 or less	−90±20	1000
3	1.544	FAR-F1DA-1M5440-G203	60 ±10	3 or less	−95±10	2035//20pF
4	1.544	FAR-F1DA-1M5440-G205	110 ±20	3 or less	−90±20	2000
5	2.048	FAR-F1DA-2M0480-G201	40 ±10	3 or less	−90±10	2035
6	2.048	FAR-F1DA-2M0480-G202	100 ±20	3 or less	−90±20	1000
7	3.088	FAR-F1DA-3M0880-G201	150 ±20	3 or less	−90±20	640
8	3.152	FAR-F1DA-3M1520-G201	85 ±15	3 or less	−90±15	1285
9	4.096	FAR-F1DA-4M0960-G201	110 ±20	3 or less	−90±20	750
10	6.312	FAR-F1DA-6M3120-G201	110 ±20	3 or less	−90±20	985
11	6.312	FAR-F1DA-6M3120-G202	110 ±20	3 or less	−90±20	1000
12	8.192	FAR-F1DA-8M1920-G201	100 ±20	3 or less	−90±20	980
13	8.448	FAR-F1DA-8M4480-G201	110 ±20	3 or less	−90±20	980
14	12.624	FAR-F1DA-12M624-G201	100 ±20	3 or less	−90±20	590
15	16.384	FAR-F1DA-16M384-G201	100 ±20	3 or less	−90±20	410
16	16.896	FAR-F1DA-16M896-G201	100 ±20	3 or less	−90±20	390
17	32.064	FAR-F2DA-32M064-G201	100 ±10	3 or less	−90±15	100
18	34.368	FAR-F2DA-34M368-G201	100 ±10	3 or less	−90±15	100
19	44.736	FAR-F3DA-44M736-G201	65 ±15	6 or less	38±10	105

■ TEST CIRCUIT

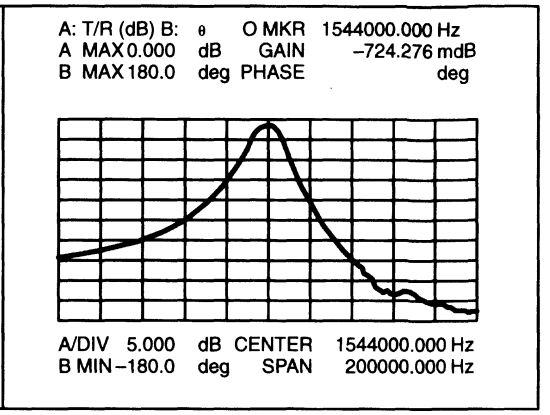


■ CHARACTERISTICS SAMPLE

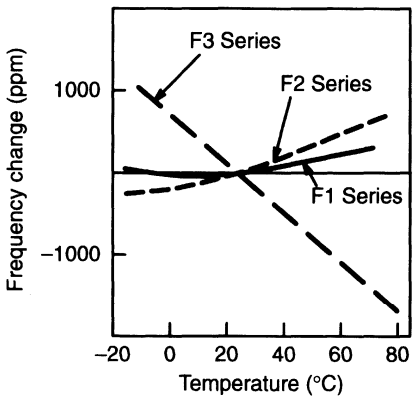
Pass band characteristic



Stop band characteristic



Temperature characteristic



■ PART NUMBERING SYSTEM

[Example]

FAR-F1DA-□□□□□□-G□□□

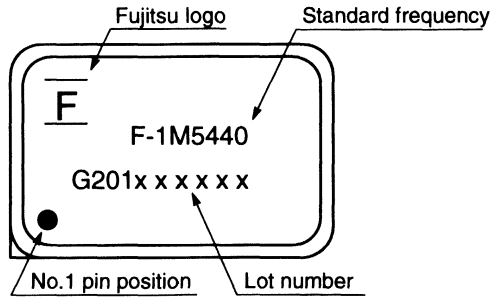
① ② ③

① Series designation

② Frequency designation : The standard frequency is designated in six alphanumeric characters. M is used to designate the decimal point in MHz. Refer to "ELECTRIC CHARACTERISTICS" in detail
Example: 1.544MHz: 1M5440

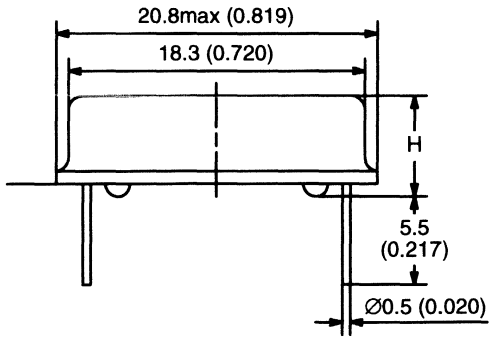
③ Serial number : The serial number is assigned from 201 to 999 (201 is normal).

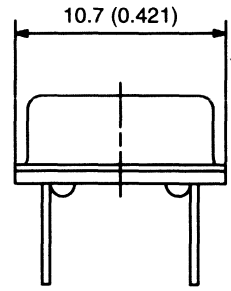
■ MARKING

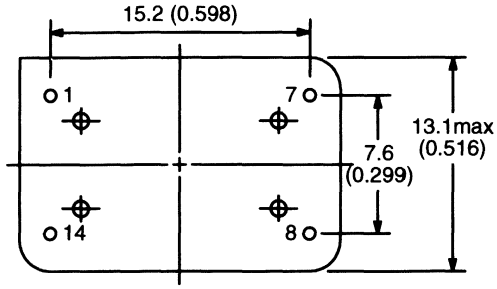


■ DIMENSIONS

Unit: mm (in.)







Series	H
F1 <3MHz	8.5 (0.335)
F1 ≥3MHz	5.8 (0.228)
F2	5.8 (0.228)
F3	5.8 (0.228)

MEMO

FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-20101-1E

ASSP

PIEZO-ELECTRIC DEVICE

F4 SERIES

TIMING EXTRACTION FILTER, 50 to 300 MHz

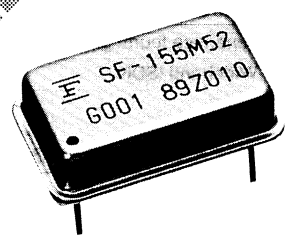
■ DESCRIPTION

The F4 series are timing extraction filter used in the high-grade digital transmission equipment like wide-band ISDN. The F4 series uses a single lithium tantalate piezoelectric crystal ($L_iT_aO_3$) that has large electromechanical coupling coefficient, and a unique SAW resonator. That provides wide bandwidths, insertion loss, and exceptional stability in VHF band until 300 MHz.

■ FEATURES

- Wide frequency range: 50 to 300 MHz
- Wide band width: 0.3 to 1.0%
- Low insertion loss: 6 dB or less
- Excellent temperature characteristics:
  ±200 ppm or less (0 to 60°C)
- No adjustment is required due to small frequency deviation:
  $\Delta fo < \pm 500$ ppm
- High reliable hermetically sealed package
- Small type, and compatible with 14-pin DIP IC

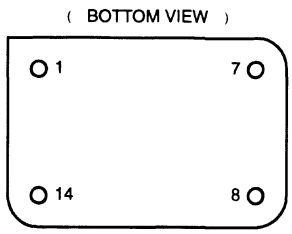
■ PACKAGE



14-pin DIP size metal case

■ PIN ASSIGNMENT

Pin number	Pin name	Description
1	IN	Input pin
7	GND	Ground pin
8	NC	No connection
14	OUT	Output pin



■ MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Operating temperature	Ta	–20 to 80	°C
Storage temperature	Tstg	–30 to 80	°C
Insulation resistance	IR	100 (100V DC)	MΩ
Frequency range		50 to 300	MHz

■ RECOMMENDED OPERATING CONDITIONS

Item	Symbol	Rating	Unit
Operating temperature	Ta	0 to 70	°C

■ STANDARD FREQUENCIES

Frequency	Application	Part number
51.84 MHz	Wide band ISDN	FAR-F4DA-51M840-G201
97.728 MHz	Japanese fourth group	FAR-F4DA-97M728-G201
155.52 MHz	Wideband ISDN	FAR-F4DA-155M52-G201

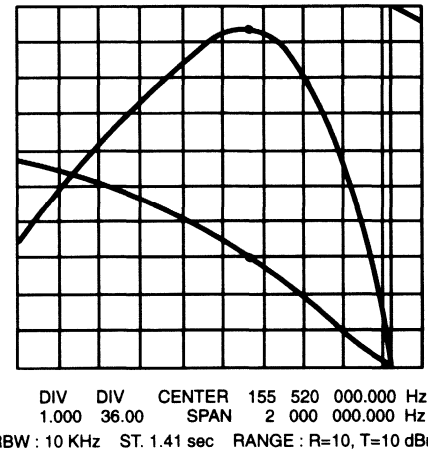
■ ELECTRICAL CHARACTERISTICS

Item	Symbol	Condition	Rated value			Unit	Remarks
			Minimum	Typical	Maximum		
Frequency deviation	Δf_O		–500	–	+500	ppm	f_0 standard
Load Q	Q		100	–	333		
Insertion loss	IL			–	6	dB	
Stop band attenuation	A_{OUT}	$f_O \pm 10$ MHz	15	–	–	dB	
Frequency temperature stability	Δf (Ta)		–300	–	+300	ppm	25°C standard Ta = 0 to 70°C
Terminate impedance	Z		10	–	50	Ω	

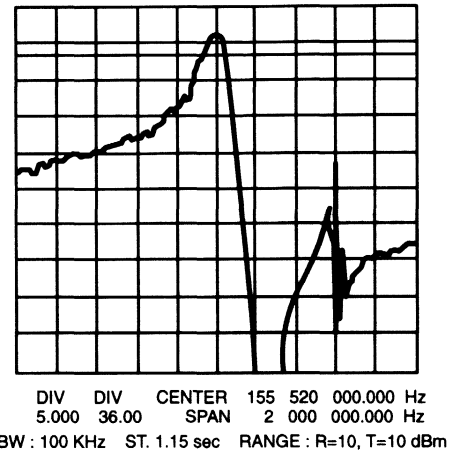
■ CHARACTERISTICS EXAMPLE

155.52 MHz example

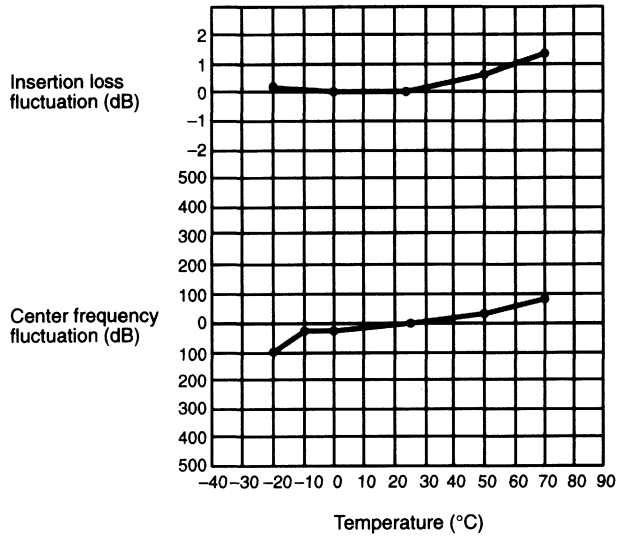
Pass band characteristic



Stop band characteristic



Temperature characteristic



■ PART NUMBERING SYSTEM

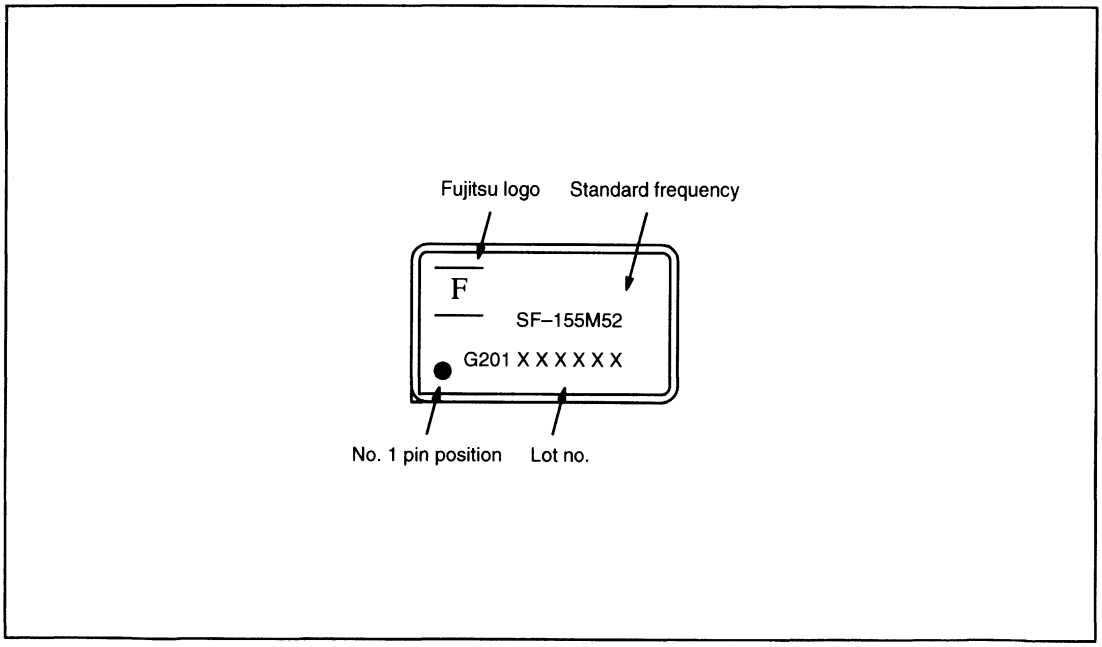
[Example]
FAR-F4DA-□□□□□□-G□□□
u l

u Frequency designation : Designate the standard frequency in six characters.
M indicates the decimal point in MHz.

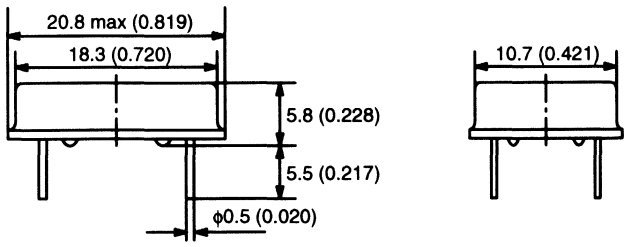
Frequency	Designation
51.84 MHz	51M840
97.728 MHz	97M728
115.52 MHz	115M52

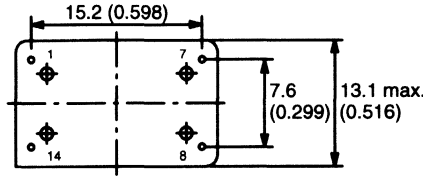
l Serial number : Specify 201 to 999 (201 is normal).

■ MARKING



■ DIMENSIONS



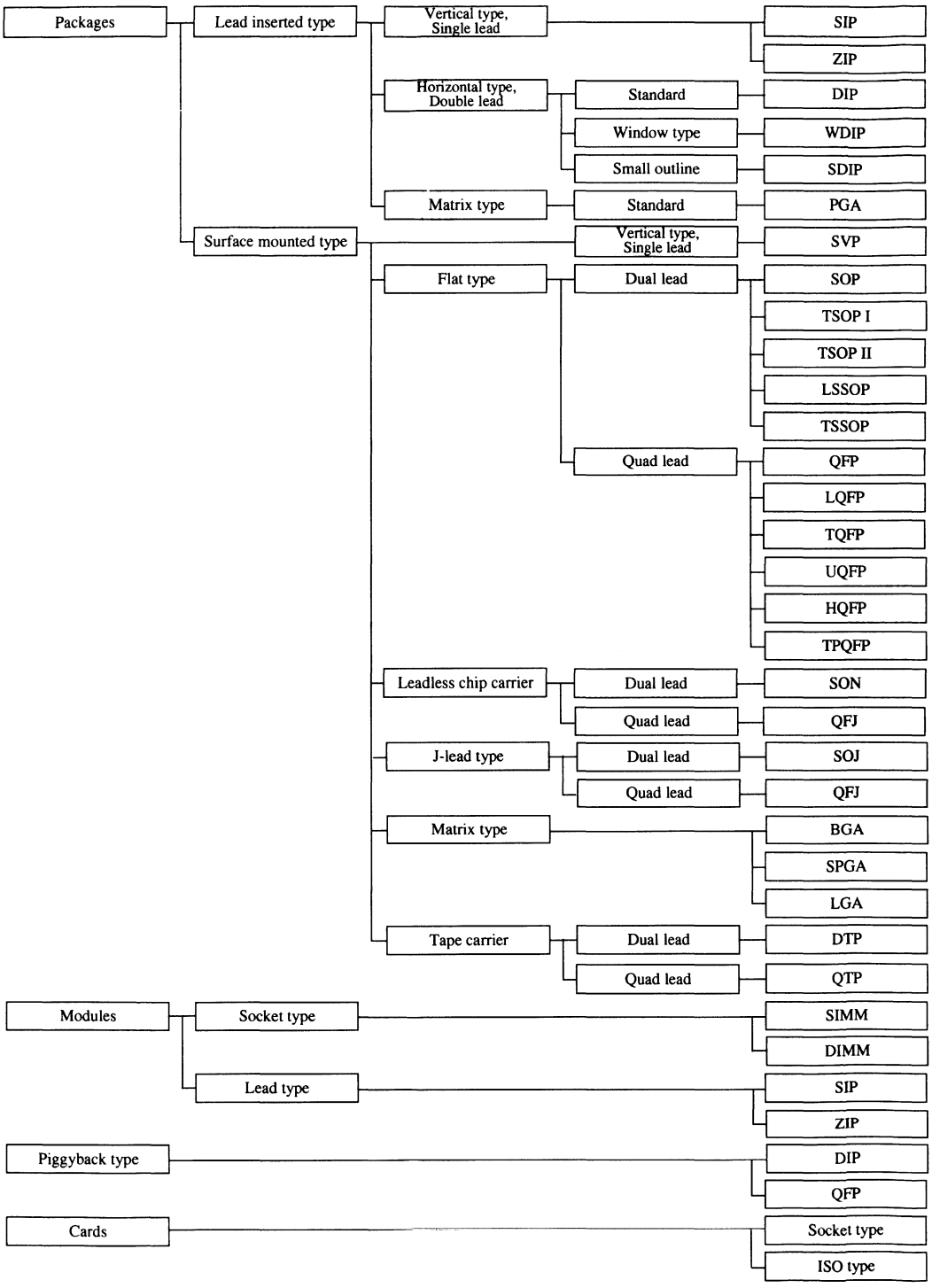


Unit: mm (in.)

MEMO

6 Package Dimensions

Package Line-up



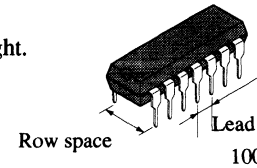
Package Line-up

Name of package	Description	Lead pitch *1 (mil)	Row space*1 (mil)
DIP	Dual In-line Package	100	300/400/600/900
SH-DIP*3	Shrink Dual In-line Package	70	—
SK-DIP*3	Skinny Dual In-line Package	100	300
SL-DIP*3	Slim Dual In-line Package	100	400
SIP	Single In-line Package	100	—
ZIP	Zig-Zag In-line Package	50 (100)	100
SZIP	Shrink Zig-Zag In-line Package	35	70
PGA	Pin Grid Array Package	50/100	—
SVP	Surface Vertical Package	0.50mm/0.65mm	—
SOP	Small Outline Package (straight lead) Small Outline L-Leaded Package(gullwing type, EIAJ*2)	50	—
SOL*3	Small Outline L-Leaded Package (JEDEC*2)	50	—
SSOP	Shrink Small Outline L-Leaded Package	0.65mm/0.80mm/ 1.00mm	—
TSOP (I)	Thin Small Outline L-Leaded Package (I)	0.50mm/0.55mm/ 0.60mm	—
TSOP (II)	Thin Small Outline L-Leaded Package (II)	0.50mm/0.80mm/ 1.00mm/1.27mm/	—
SON	Small Outline Non-Leaded Package	0.50mm/1.00mm	—
QFP	Quad Flat Package(straight lead) Quad Flat L-Leaded Package	0.40mm/0.50mm/ 0.65mm/0.80mm/ 1.00mm	—
LQFP*3	Low Profile Shrink Quad Flat L-Leaded Package	0.40mm/0.50mm	—
TQFP	Thin Quad Flat L-Leaded Package	0.40mm/0.50mm	—
TPQ	Test Pad QFP	0.30mm	—
LCC*3	Leadless Chip Carrier	40/50	—
QFN	Quad Flat Non-Leaded Package		
PCLP*3	Printed Circuit-board Leadless Package	0.50mm/0.65mm	—
QFJ	Quad Flat J-Leaded Package	50	—
SOJ	Small Outline J-Leaded Package	50	—
BGA	Ball Grid Array	1.5mm/1.27mm/1.0mm	—
DTP	Dual Tape Carrier Package	—	—
QTP	Quad Tape Carrier Package	—	—
SIMM	Single Inline Memory Module	50/100	—
DIMM	Dual Inline Memory Module	50	—

*1 : These columns indicate the dimensions shown at right.

*2 : Joint Electron Device Engineering Council

*3 : Package name used by Fujitsu

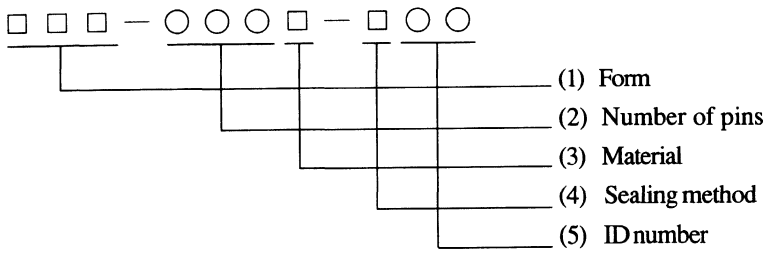


100 mil = 2.54 mm

Package Codes

Distinctions among package forms, number of pins, material, sealing method, etc., as well as classification between package and modules are shown in the package code as follows.

Packages (excluding TCP)



(1) Form : Indicates the form of package. (three letters)
DIP : Indicates a DIP-type package (includes SH, SK, and SL) .
SIP : Indicates an SIP-type package.
ZIP : Indicates a ZIP-type package.
PGA : Indicates a PGA-type package.
FPT : Indicates a flat-type package.
LCC : Indicates an LCC-, QFJ-, or SOJ-type package.

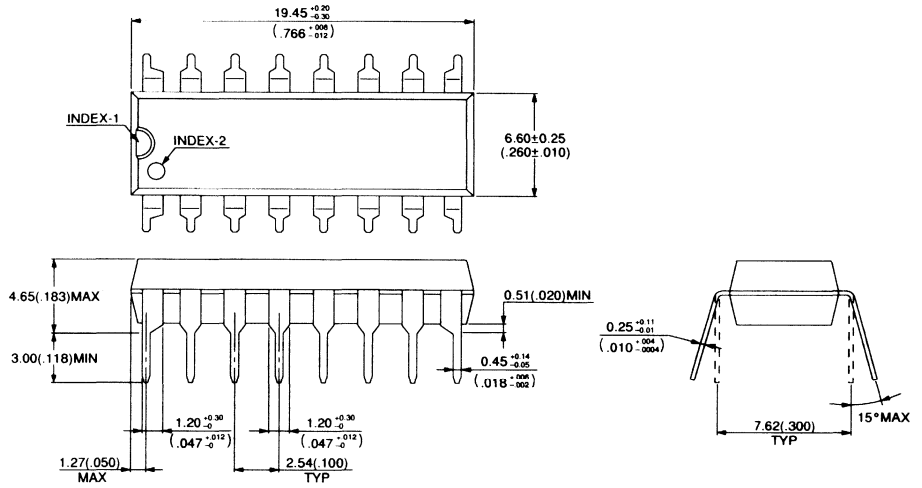
(2) Number of pins : Indicates the number of pins.

(3) Material : Indicates the package material. (one letter)
P : Plastic
C : Ceramic

(4) Sealing method : Indicates the package sealing method. (one letter)
M: Plastic mold
A : Metal seal
F : Frit seal
C : Cerdip

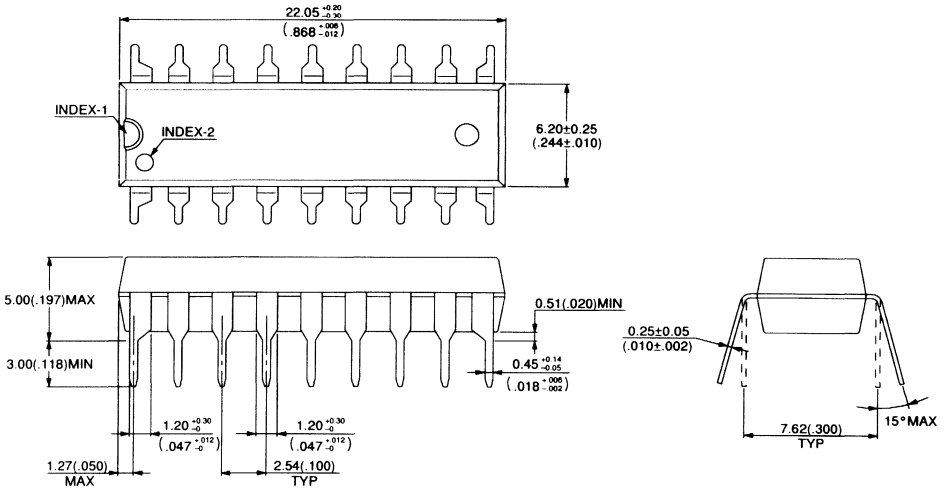
(5) ID number : An ID number within the form (two digits)

16-pin plastic DIP
(DIP-16P-M03)



Dimensions in mm (inches).

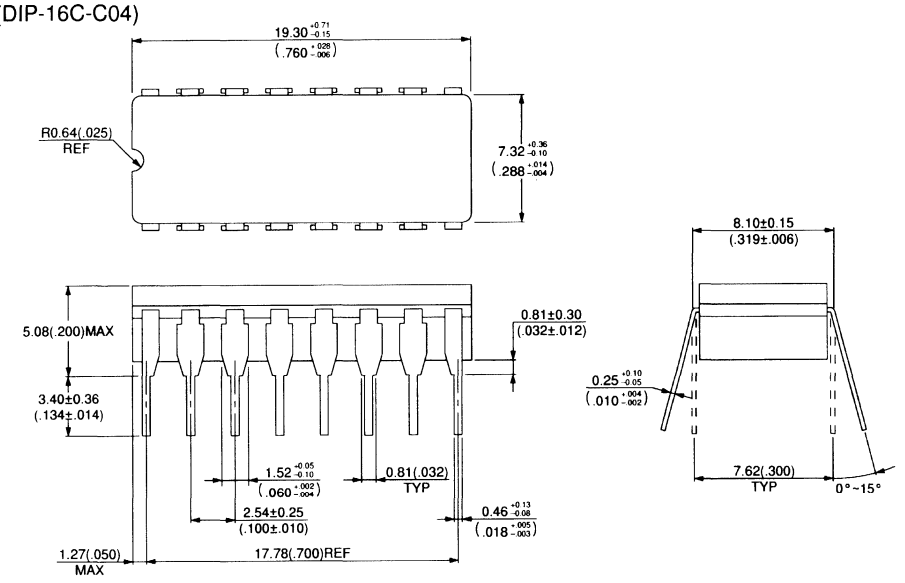
18-pin plastic DIP
(DIP-18P-M02)



Dimensions in mm (inches).

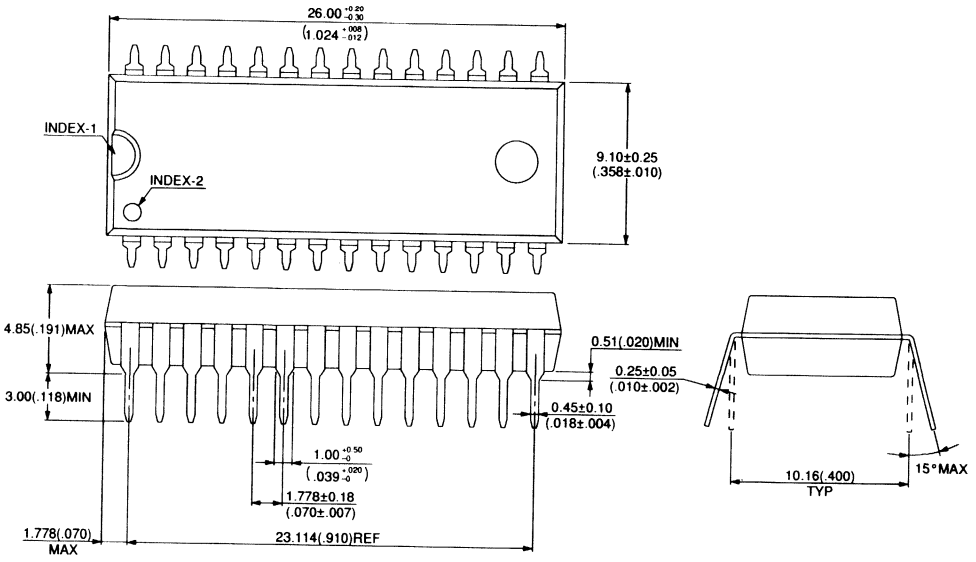
Dimensions

16-pin plastic DIP
(DIP-16C-C04)



Dimensions in mm (inches).

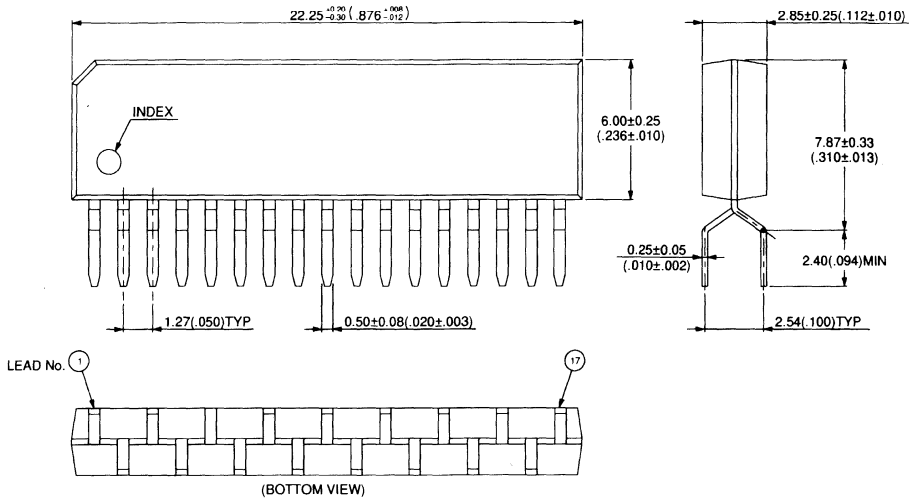
28-pin plastic SH- DIP
(DIP-28P-M03)



Dimensions in mm (inches).

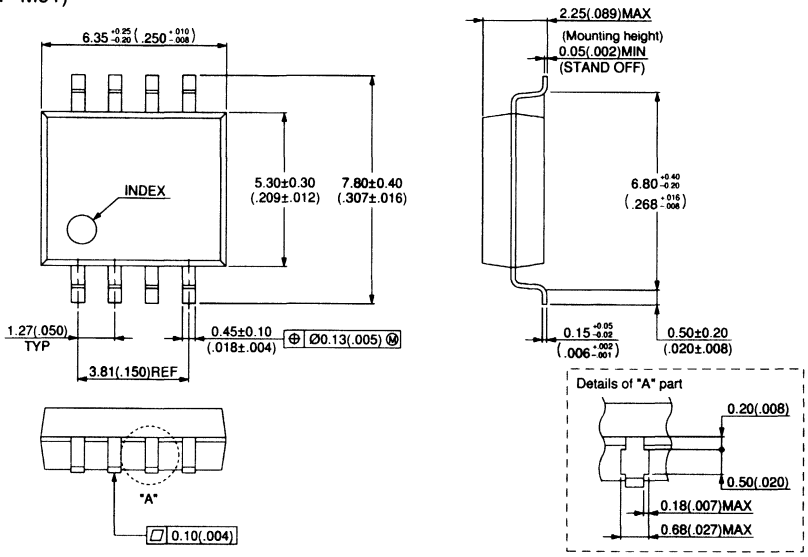
Dimensions

17-pin plastic ZIP
(ZIP-17P-M01)



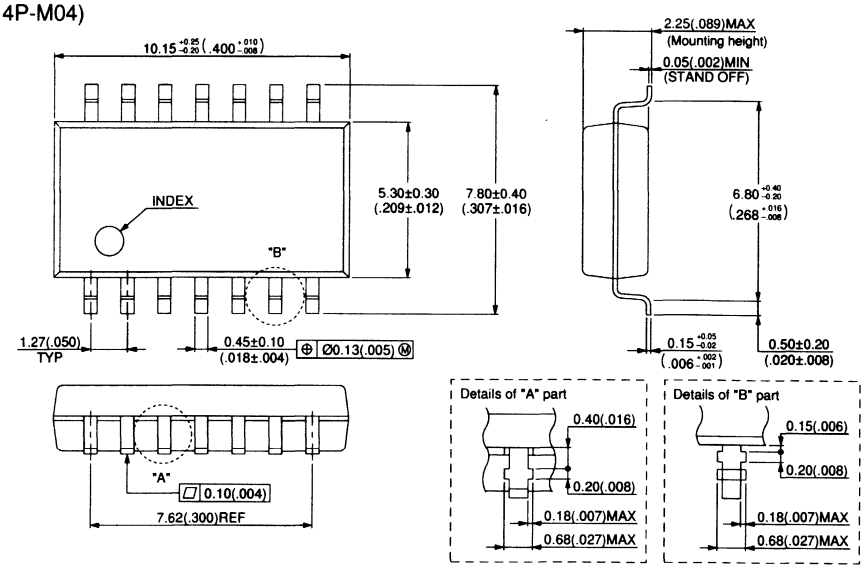
Dimensions in mm (inches).

8-pin plastic SOP
(FPT-8P-M01)



Dimensions in mm (inches) .

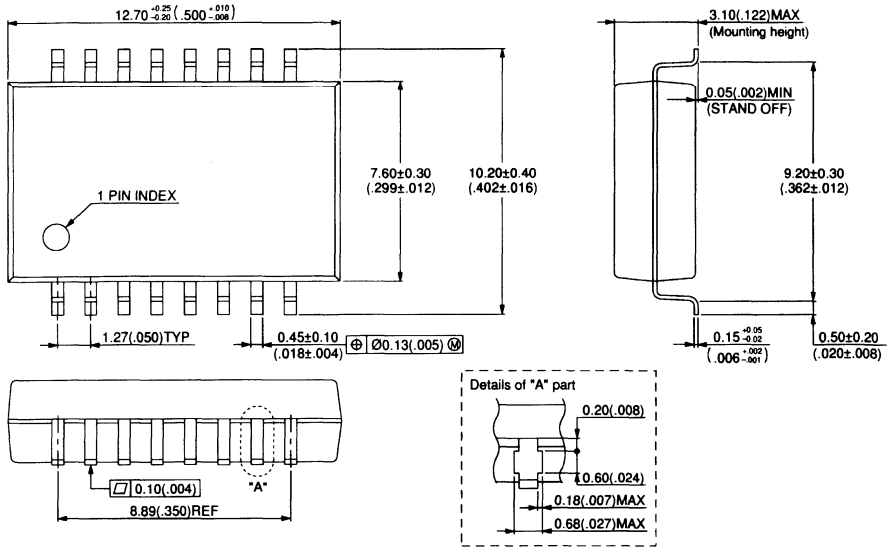
14-pin plastic SOP
(FPT-14P-M04)



Dimensions in mm (inches) .

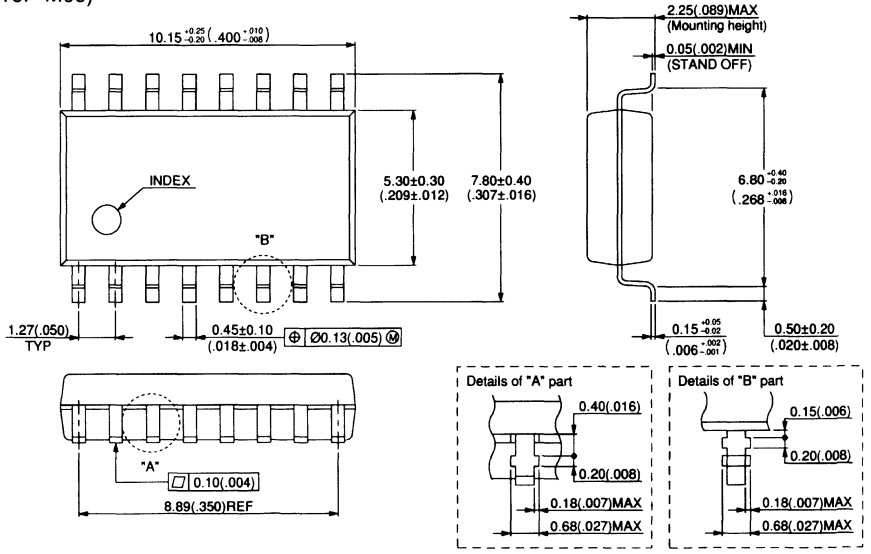
Dimensions

16-pin plastic SOP
(FPT-16P-M03)



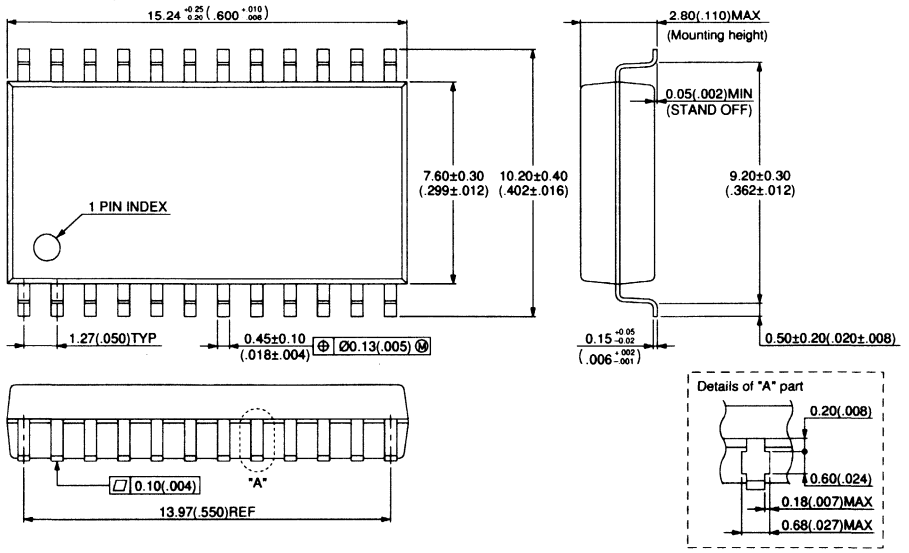
Dimensions in mm (inches).

16-pin plastic SOP
(FPT-16P-M06)



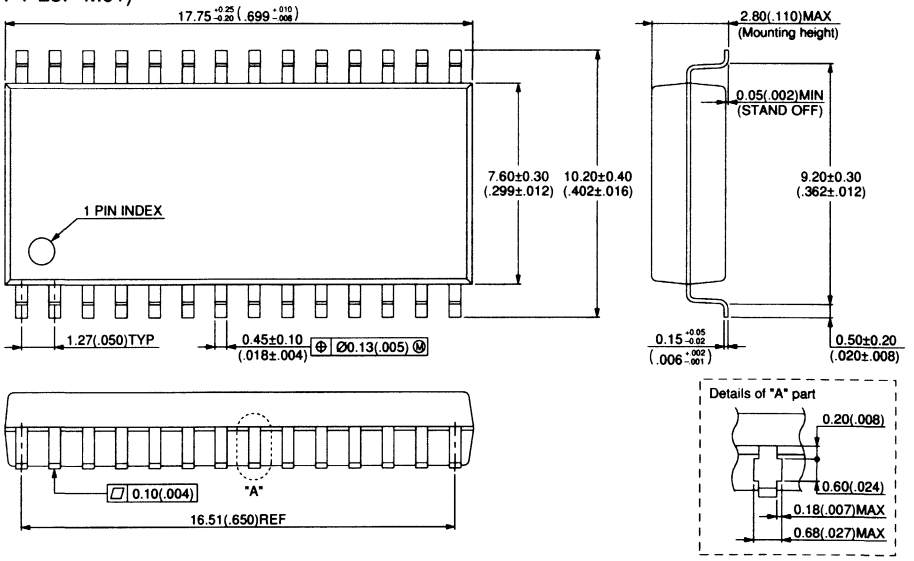
Dimensions in mm (inches).

24-pin plastic SOP
(FPT-24P-M02)



Dimensions in mm (inches).

28-pin plastic SOP
(FPT-28P-M01)

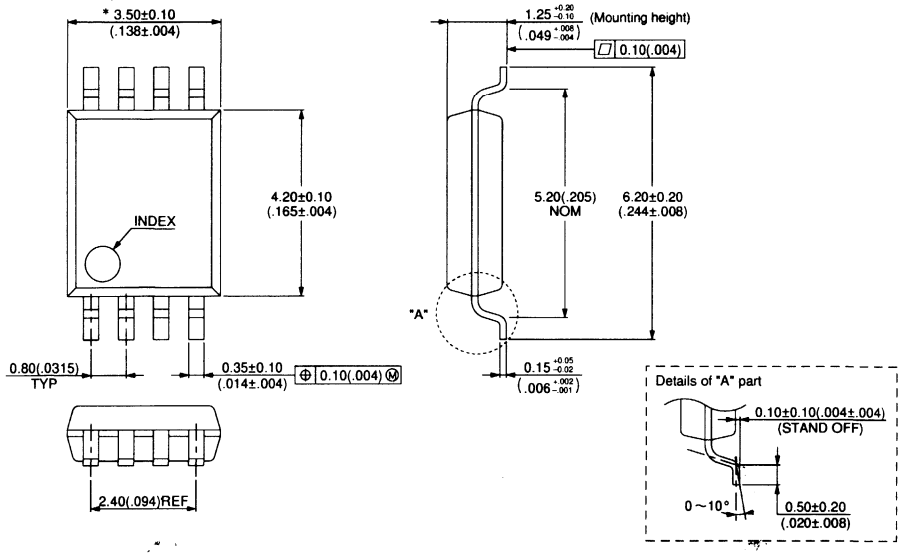


Dimensions in mm (inches).

Dimensions

8-pin plastic SSOP
(FPT-8P-M03)

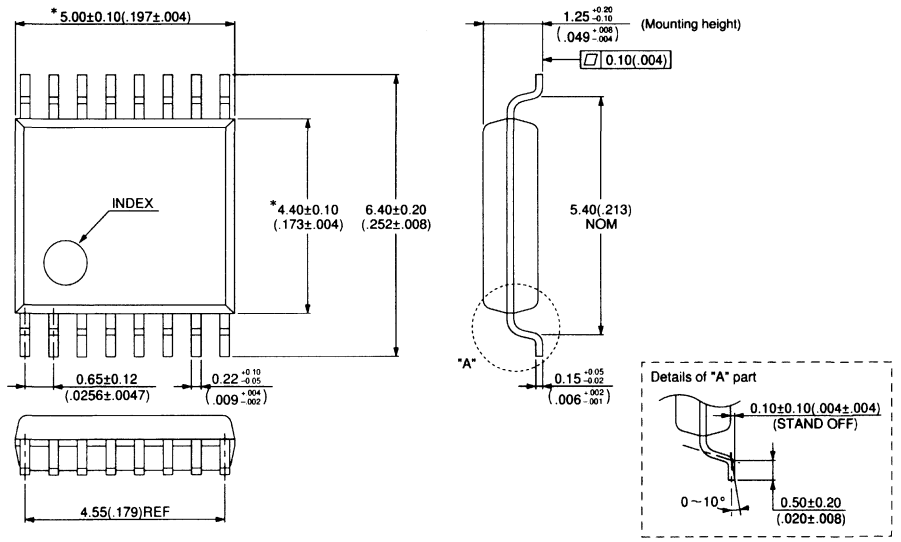
*:This dimension does not include resin protrusion.



Dimensions in mm (inches).

16-pin plastic SSOP
(FPT-16P-M05)

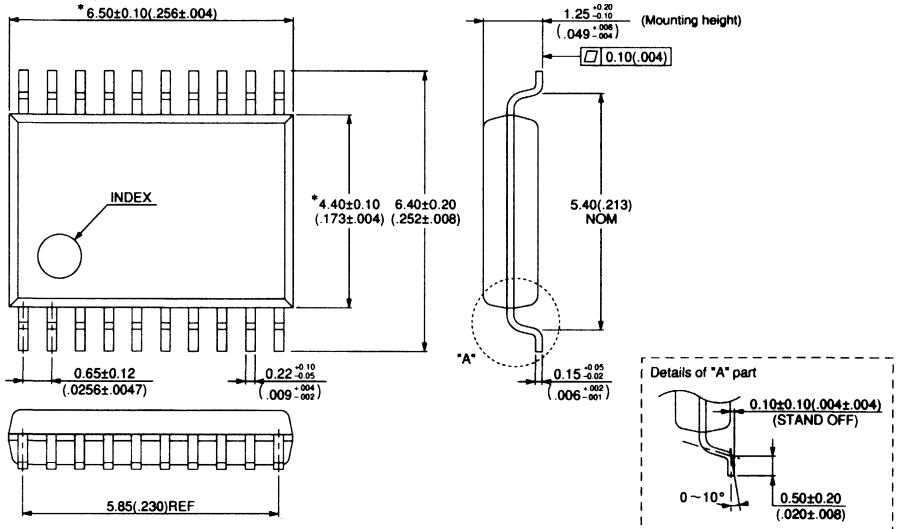
*:This dimension does not include resin protrusion.



Dimensions in mm (inches).

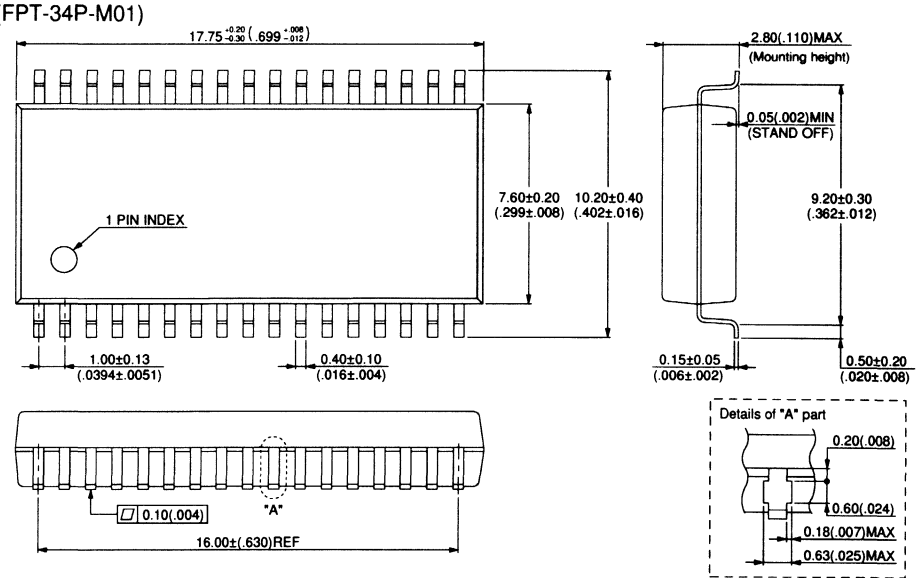
20-pin plastic SSOP
(FPT-20P-M03)

*:This dimension does not include resin protrusion.



Dimensions in mm (inches).

34-pin plastic SSOP
(FPT-34P-M01)

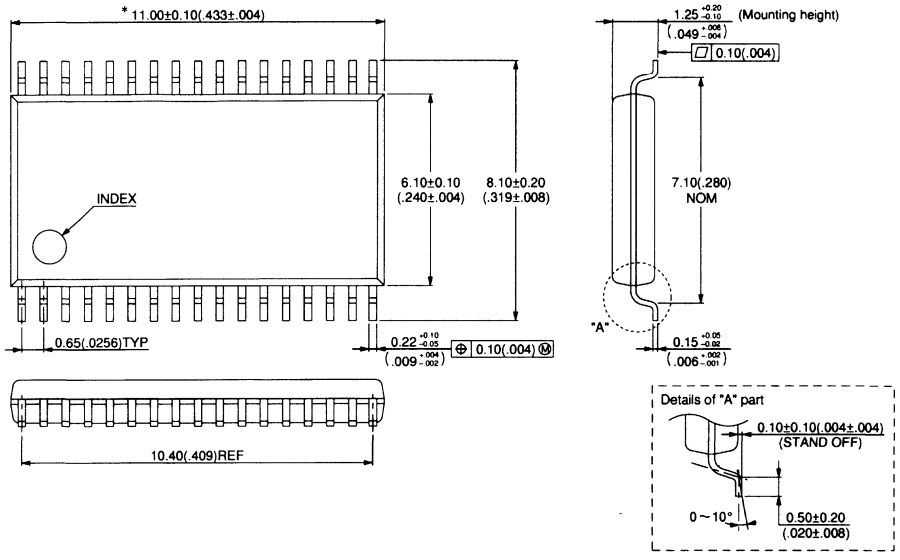


Dimensions in mm (inches).

Dimensions

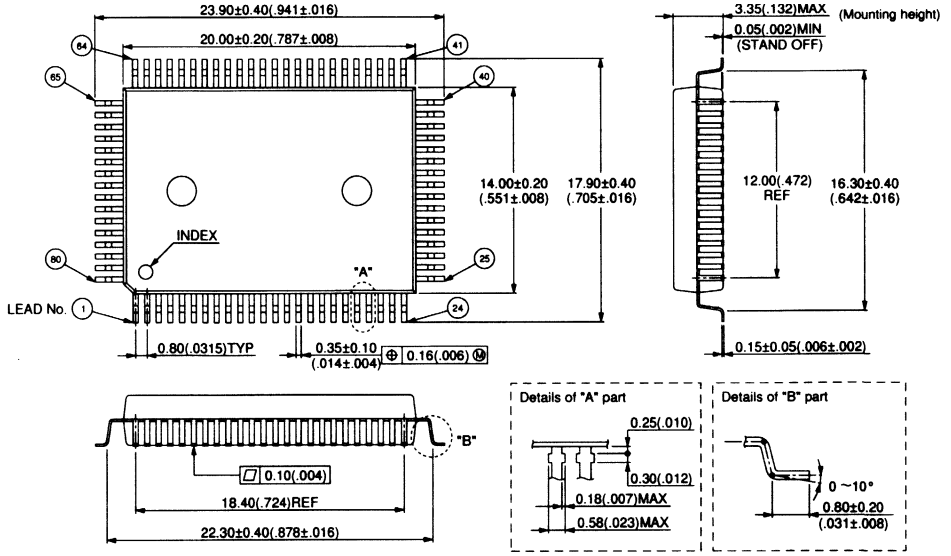
34-pin plastic SSOP
(FPT-34P-M03)

*:This dimension does not include resin protrusion.



Dimensions in mm (inches) .

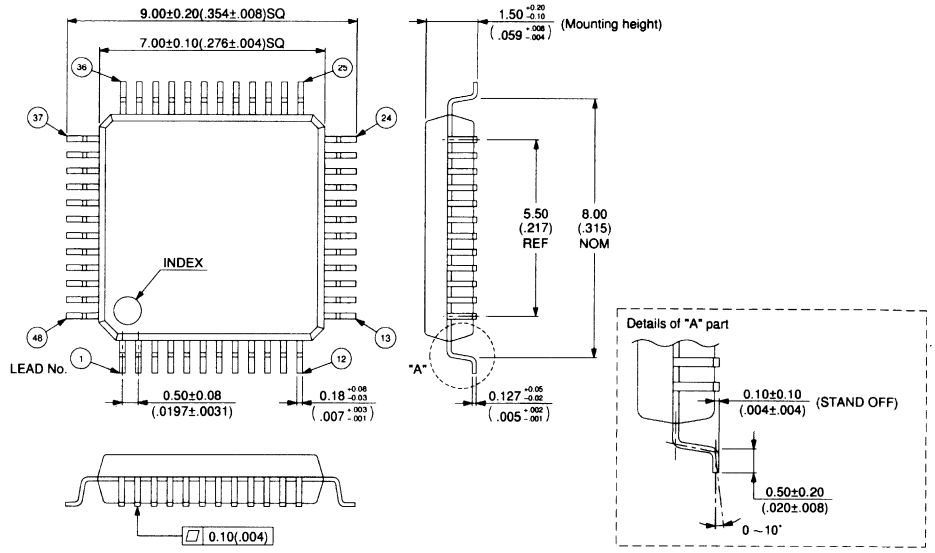
80-pin plastic QFP
(FPT-80P-M06)



Dimensions in mm (inches) .

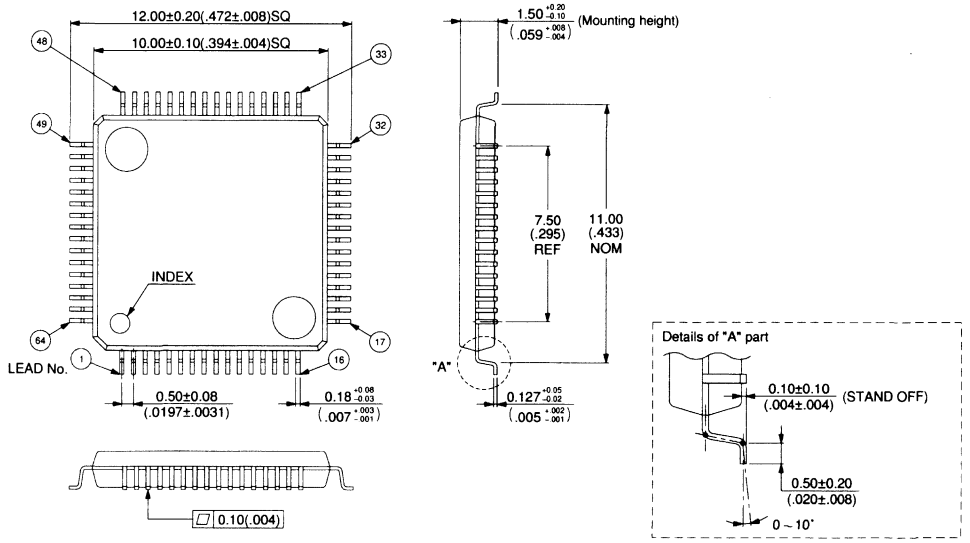
Dimensions

48-pin plastic LQFP
(FPT-48P-M05)



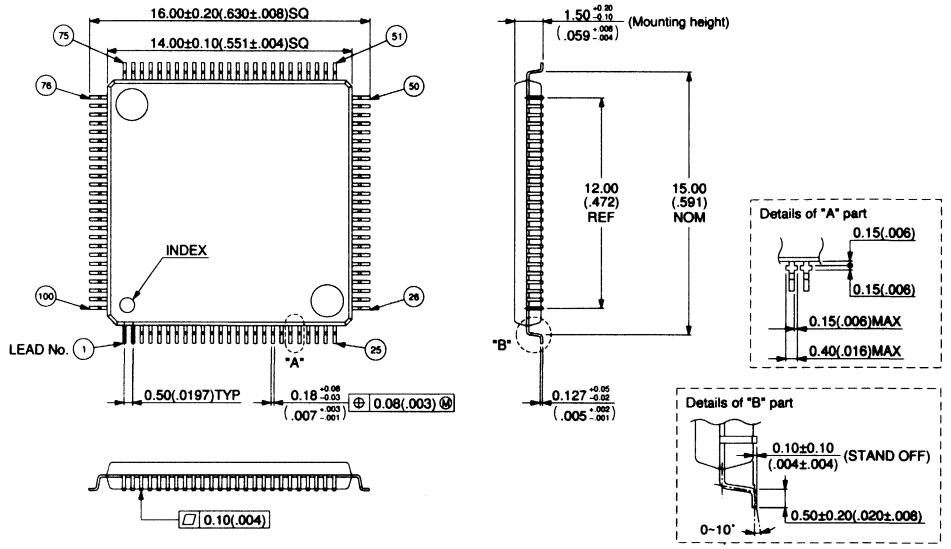
Dimensions in mm (inches).

64-pin plastic LQFP
(FPT-64P-M03)



Dimensions in mm (inches).

100-pin plastic LQFP
(FPT-100P-M05)



Dimensions in mm (inches) .

MEMO

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